4K X2804C 512 x 8 Bit

5 Volt, Byte Alterable E²PROM

FEATURES

- **90ns Access Time**
- **Simple Byte and Page Write**
  - **—Single 5V Supply**
    - **—No External High Voltages or V_{PP} Control Circuits**
  - **—Self-Timed**
    - **—No Erase Before Write**
    - **—No Complex Programming Algorithms**
    - **—No Overerase Problem**
- **High Performance Advanced NMOS Technology**
- **Fast Write Cycle Times**
  - **—16 Byte Page Write Operation**
  - **—Byte or Page Write Cycle: 5ms Typical**
  - **—Complete Memory Rewrite: 640ms Typical**
  - **—Effective Byte Write Cycle Time: 300µs Typical**
- **$\overline{DATA}$ Polling**
  - **—Allows User to Minimize Write Cycle Time**
- **JEDEC Approved Byte-Wide Pinout**
- **High Reliability**
  - **—Endurance: 10,000 Cycles**
  - **—Data Retention: 100 Years**

DESCRIPTION

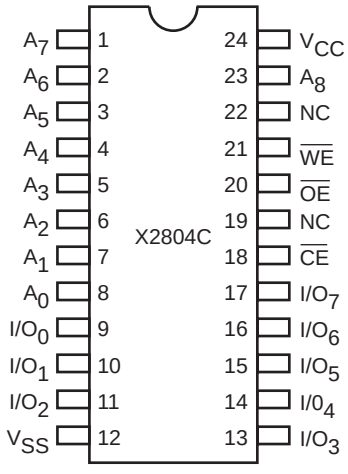
The Xicor X2804C is a 512 x 8 E²PROM, fabricated with an advanced, high performance N-channel floating gate MOS technology. Like all Xicor Programmable nonvolatile memories it is a 5V only device. The X2804C features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

The X2804C supports a 16-byte page write operation, typically providing a 300µs/byte write cycle, enabling the entire memory to be written in less than 640ms. The X2804C also features $\overline{DATA}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

PIN CONFIGURATION

PLASTIC DIP



6612 FHD F02.1

PIN DESCRIPTIONS

Addresses (A_0–A_8)

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

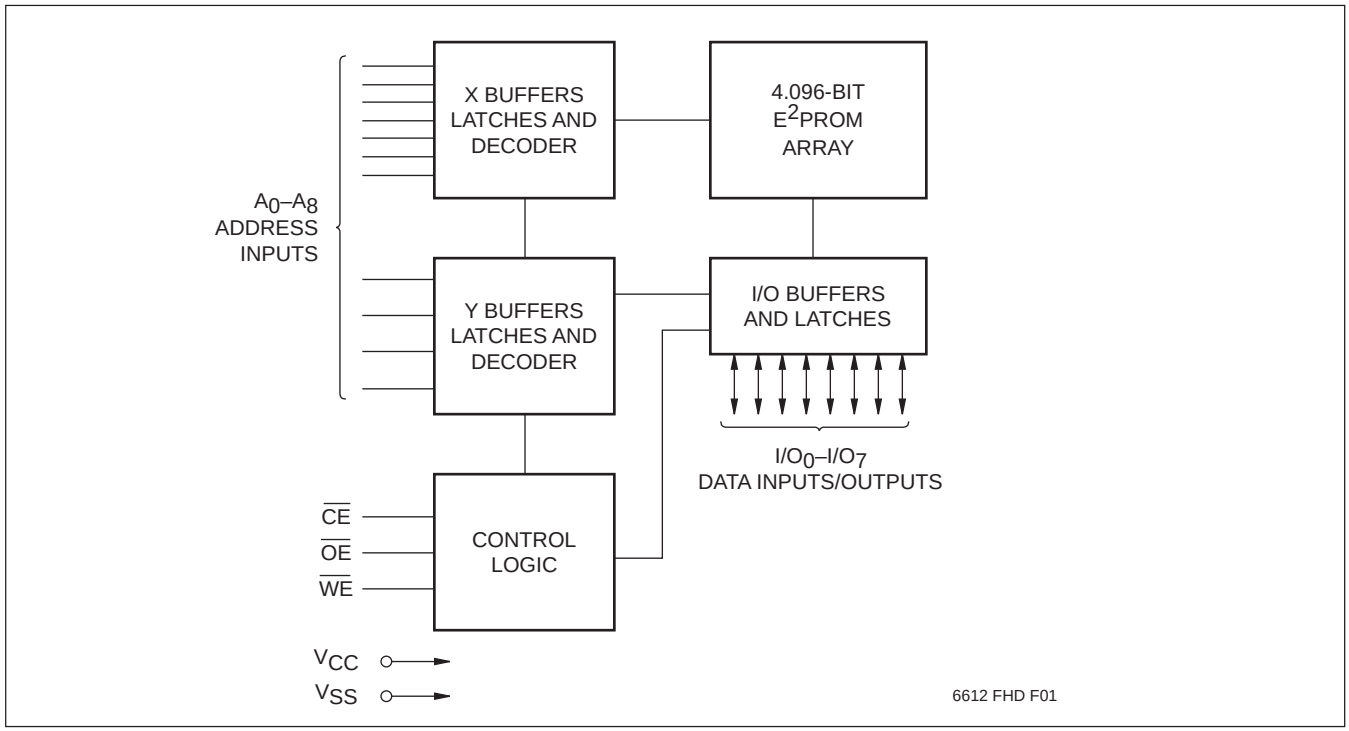
The Output Enable input controls the data output buffers and is used to initiate read operations.

PIN NAMES

Symbol	Description
A_0–A_8	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

6612 PGM T01

FUNCTIONAL DIAGRAM



DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW and $\overline{WE}$ HIGH. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X2804C supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5ms.

Page Write Operation

The page write feature of the X2804C allows the entire memory to be typically written in 450ms. Page write allows two to sixteen bytes of data to be consecutively written to the X2804C prior to the commencement of the internal programming cycle. Although the host system may read data from any other device in the system to transfer to the X2804C, the destination page address of the X2804C should be the same on each subsequent strobe of the $\overline{WE}$ and $\overline{CE}$ inputs. That is, A_4 through A_{10} must be the same for each transfer of data to the X2804C during a page write cycle.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to fifteen bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 20µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 20µs, the internal automatic programming cycle will commence. There is no page write window limitation. The page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 20µs.

$\overline{DATA}$ Polling

The X2804C features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X2804C, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

WRITE PROTECTION

There are three features that protect the nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse which is typically less than 10ns will not initiate a write cycle.
- V_{CC} Sense—All functions are inhibited when V_{CC} is ≤3V, typically.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH during power-up and power-down, will inhibit inadvertent writes. Write cycle timing specifications must be observed concurrently.

ENDURANCE

Xicor E²PROMs are designed and tested for applications requiring extended endurance.

SYSTEM CONSIDERATIONS

Because the X2804C is frequently used in large memory arrays, it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit, it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X2804C has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1µF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7µF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias
- X2804C ..... –10°C to +85°C
- X2804CI ..... –65°C to +135°C

Storage Temperature ..... –65°C to +150°C

Voltage on any Pin with
- Respect to V_{SS} ..... –1V to +7V

D.C. Output Current 5mA

Lead Temperature (Soldering, 10 seconds)..... 300°C

***COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C

6612 PGM T02.2

Supply Voltage	Limits
X2804C	5V ±10%

6612 PGM T03

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active)		70	110	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL} All I/O’s = Open Other Inputs = V_{CC}
I_{SB}	V_{CC} Current (Standby)		35	50	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O’s = Open Other Inputs = V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(2)	Input LOW Voltage	–1		0.8	V	
V_{IH}(2)	Input HIGH Voltage	2		V_{CC} +1	V	
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –400µA

6612 PGM T02.1

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage and are not tested.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Unit
Minimum Endurance	10,000		Cycles/Byte
Data Retention	100		Years

6612 PGM T03

POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(3)	Power-Up to Read Operation	1	ms
t_{PUW}(3)	Power-Up to Write Operation	5	ms

6612 PGM T04

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance	6	pF	V_{IN} = 0V

6612 PGM T05.1

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V

3852 PGM T06.1

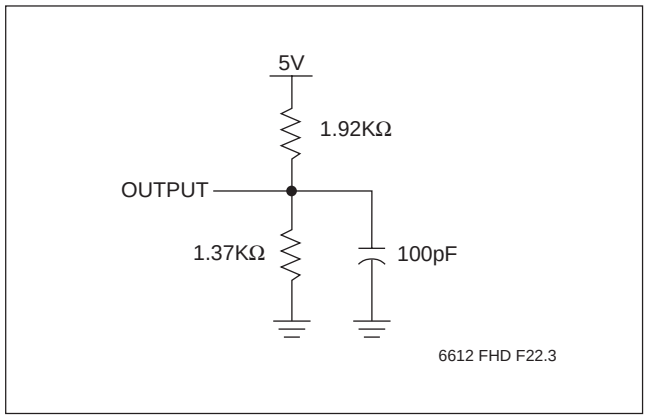
MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

6612 PGM T07

Note: (3) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUITS



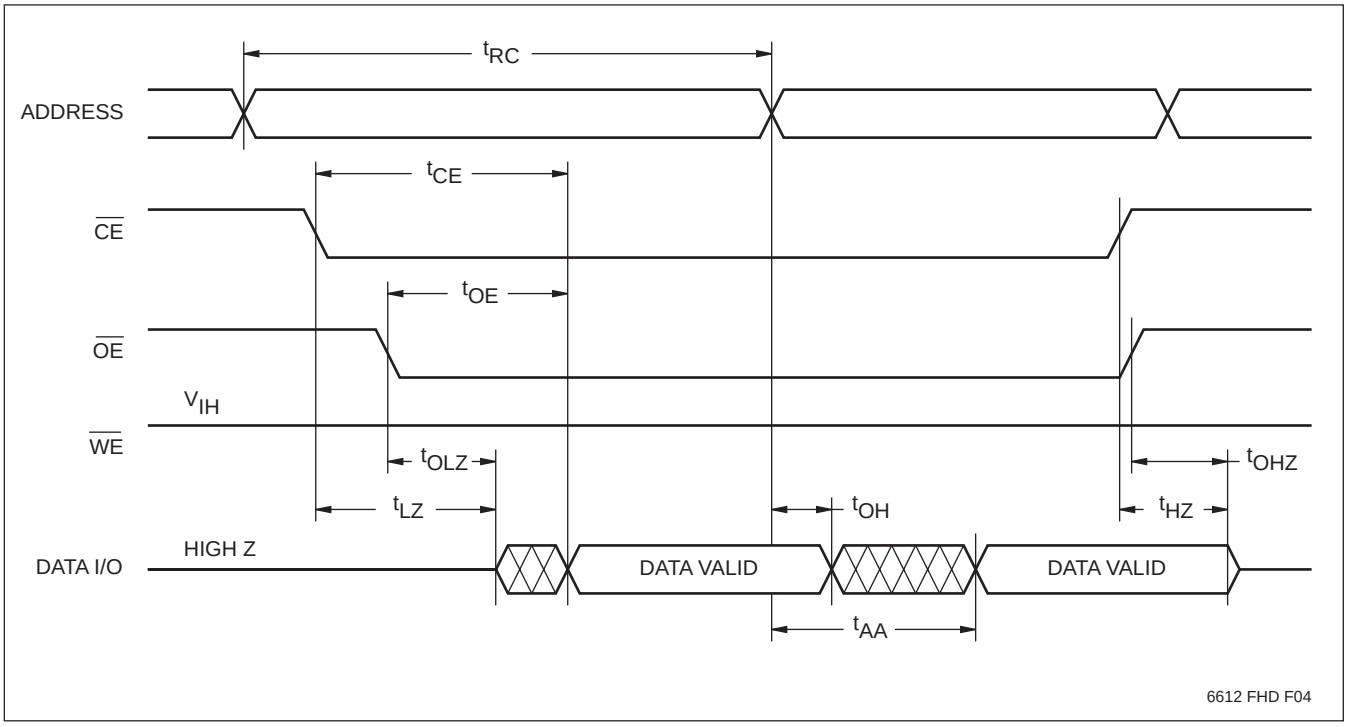
A.C. CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Read Cycle Limits

Symbol	Parameter	X2804C-90		X2804C-15		X2804C-20		X2804C-25		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	90		150		200		250		ns
t_{CE}	Chip Enable Access Time		90		150		200		250	ns
t_{AA}	Address Access Time		90		150		200		250	ns
t_{OE}	Output Enable Access Time		60		80		100		100	ns
t_{LZ}(4)	$\overline{CE}$ LOW to Active Output	0		0		0		0		ns
t_{OLZ}(4)	$\overline{OE}$ LOW to Active Output	0		0		0		0		ns
t_{HZ}(4)	$\overline{CE}$ HIGH to High Z Output		50		60		60		60	ns
t_{OHZ}(4)	$\overline{OE}$ HIGH to High Z Output		50		60		60		60	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

6612 PGM T10.1

Read Cycle



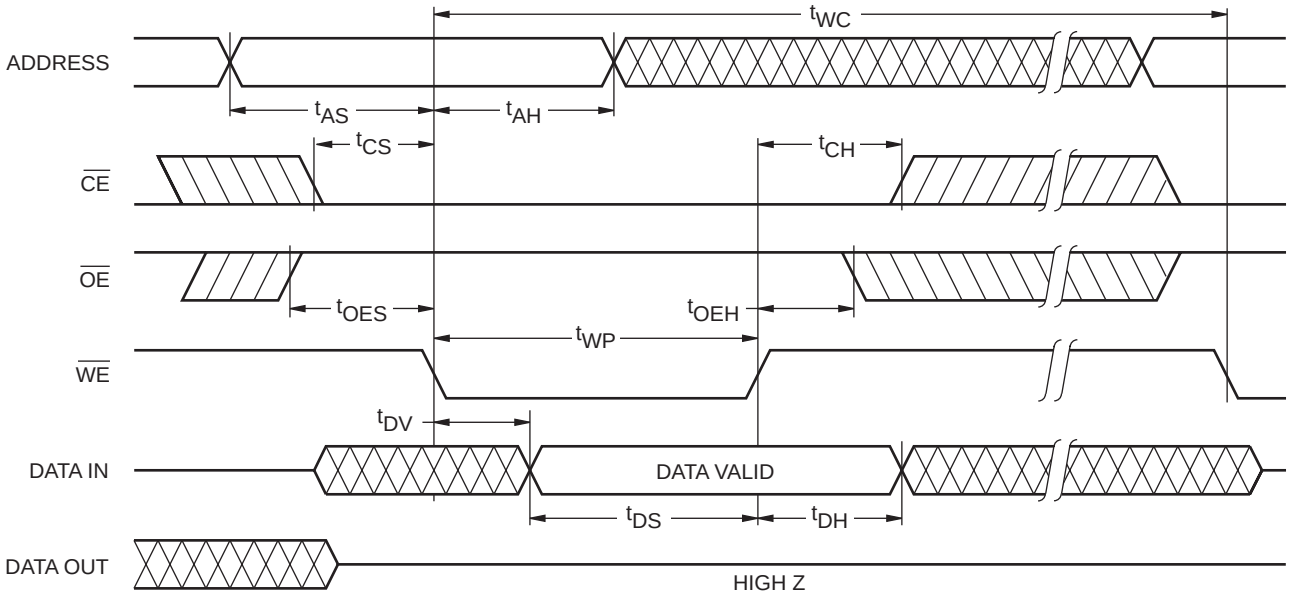
Notes: (4) t_{LZ} min., t_{HZ}, t_{OLZ}, and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

Write Cycle Limits

Symbol	Parameter	X2804C-90		X2804C-15,-20,-25		Units
		Min.	Max.	Min.	Max.	
t_{WC}(5)	Write Cycle Time		10		10	ms
t_{AS}	Address Setup Time	5		5		ns
t_{AH}	Address Hold Time	80		100		ns
t_{CS}	Write Setup Time	0		0		ns
t_{CH}	Write Hold Time	0		0		ns
t_{CW}	$\overline{CE}$ Pulse Width	80		100		ns
t_{OES}	$\overline{OE}$ HIGH Setup Time	10		10		ns
t_{OEH}	$\overline{OE}$ HIGH Hold Time	5		10		ns
t_{WP}	$\overline{WE}$ Pulse Width	80		100		ns
t_{WPH}	$\overline{WE}$ HIGH Recovery	50		50		ns
t_{DV}	Data Valid		100		100	µs
t_{DS}	Data Setup	35		50		ns
t_{DH}	Data Hold	5		10		ns
t_{DW}	Delay to Next Write	10		10		µs
t_{BLC}	Byte Load Cycle	1	100	1	100	µs

6612 PGM T09.1

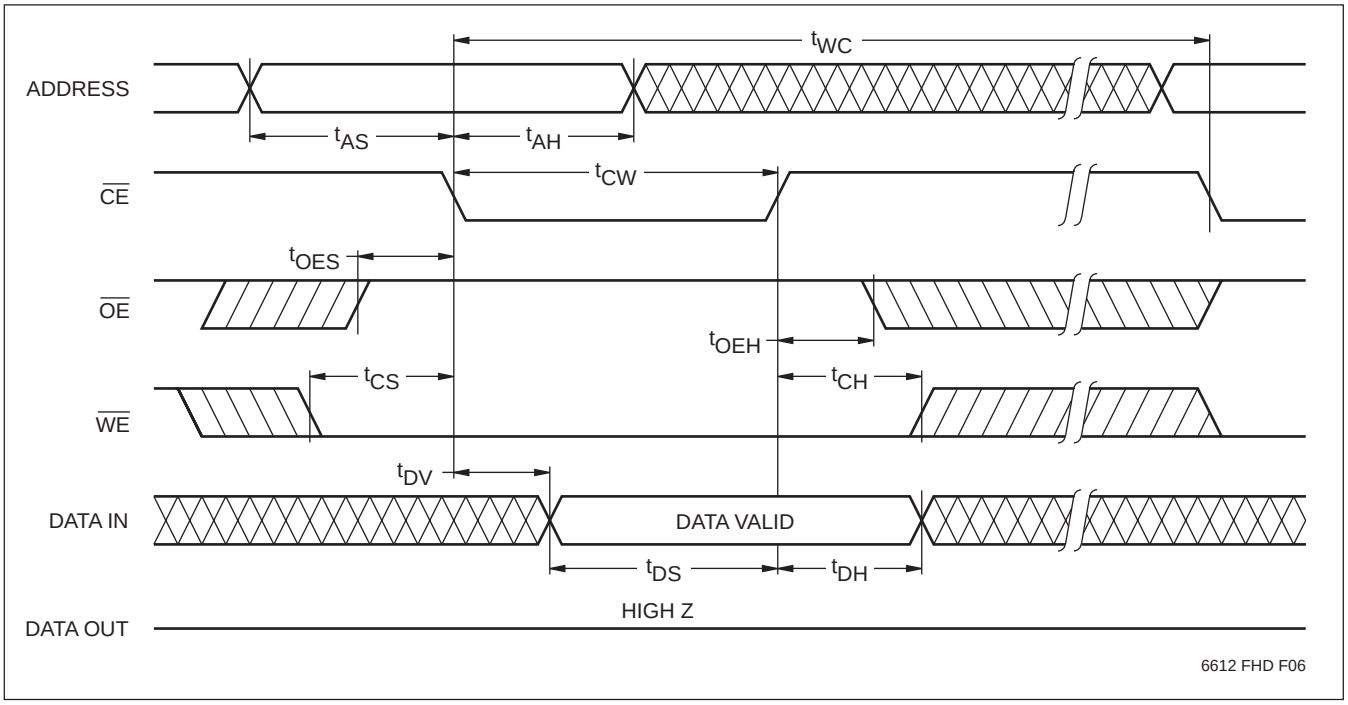
$\overline{WE}$ Controlled Write Cycle



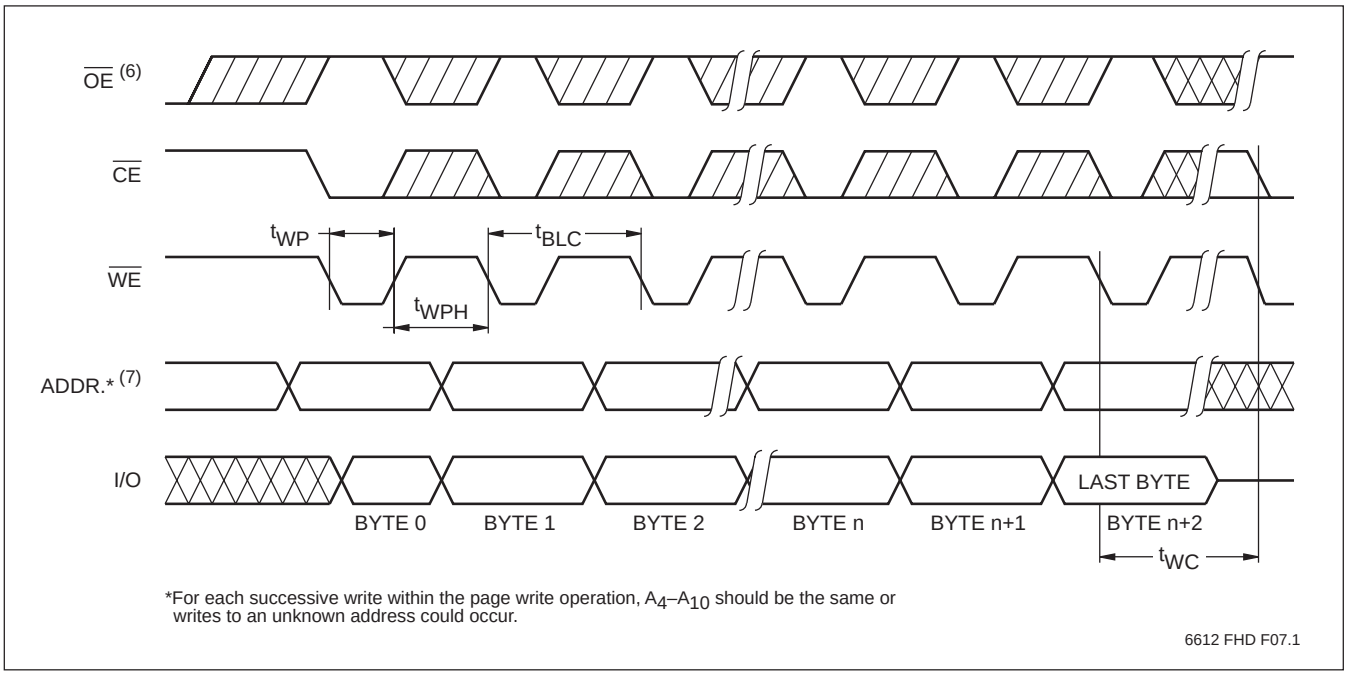
6612 FHD F05

Notes: (5) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation. For faster t_{WC}, please refer to X28C16 and X28HC16 product data sheets.

$\overline{CE}$ Controlled Write Cycle



Page Mode Write Cycle

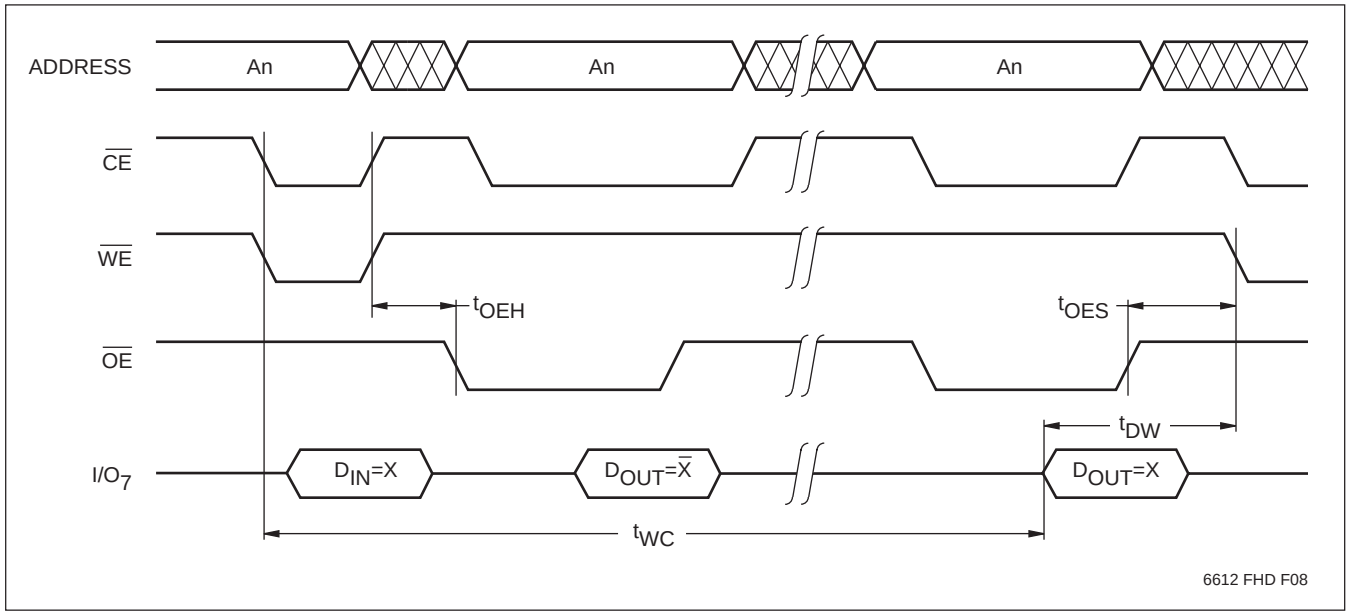


*For each successive write within the page write operation, A_4–A_{10} should be the same or writes to an unknown address could occur.

Notes: (6) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(7) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram[10]

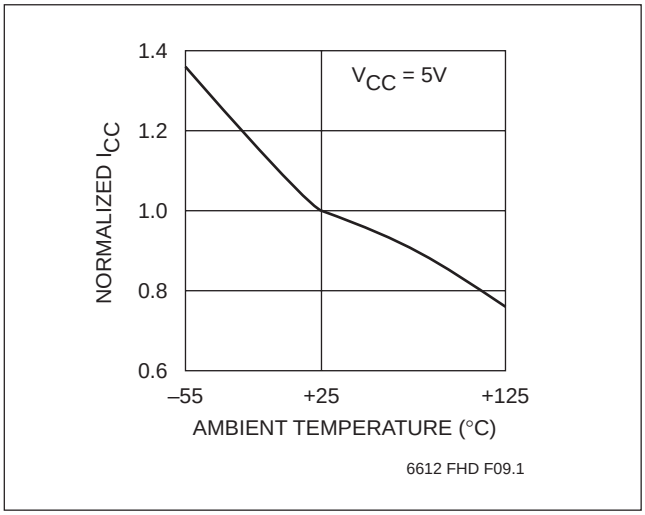


Note: (10) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

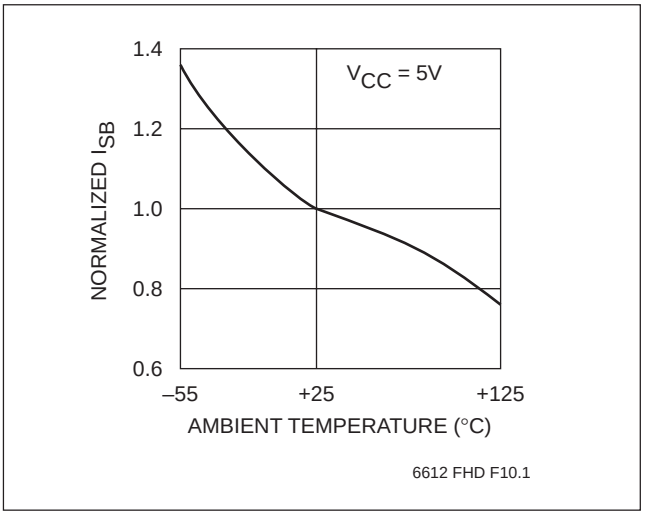
SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

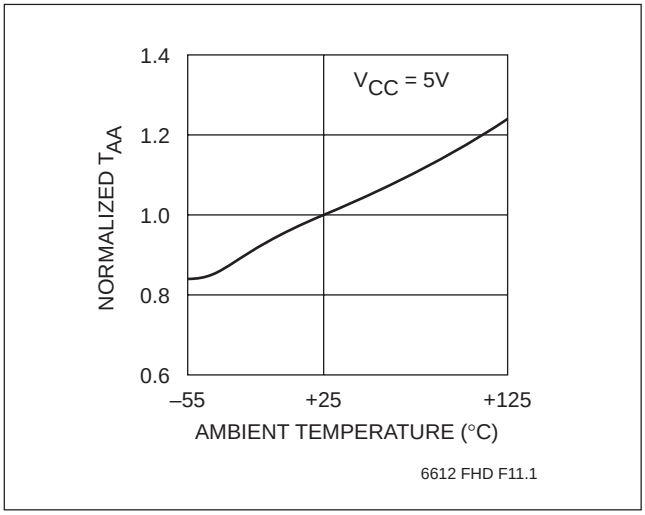
Normalized Active Supply Current vs. Ambient Temperature



Normalized Standby Supply Current vs. Ambient Temperature

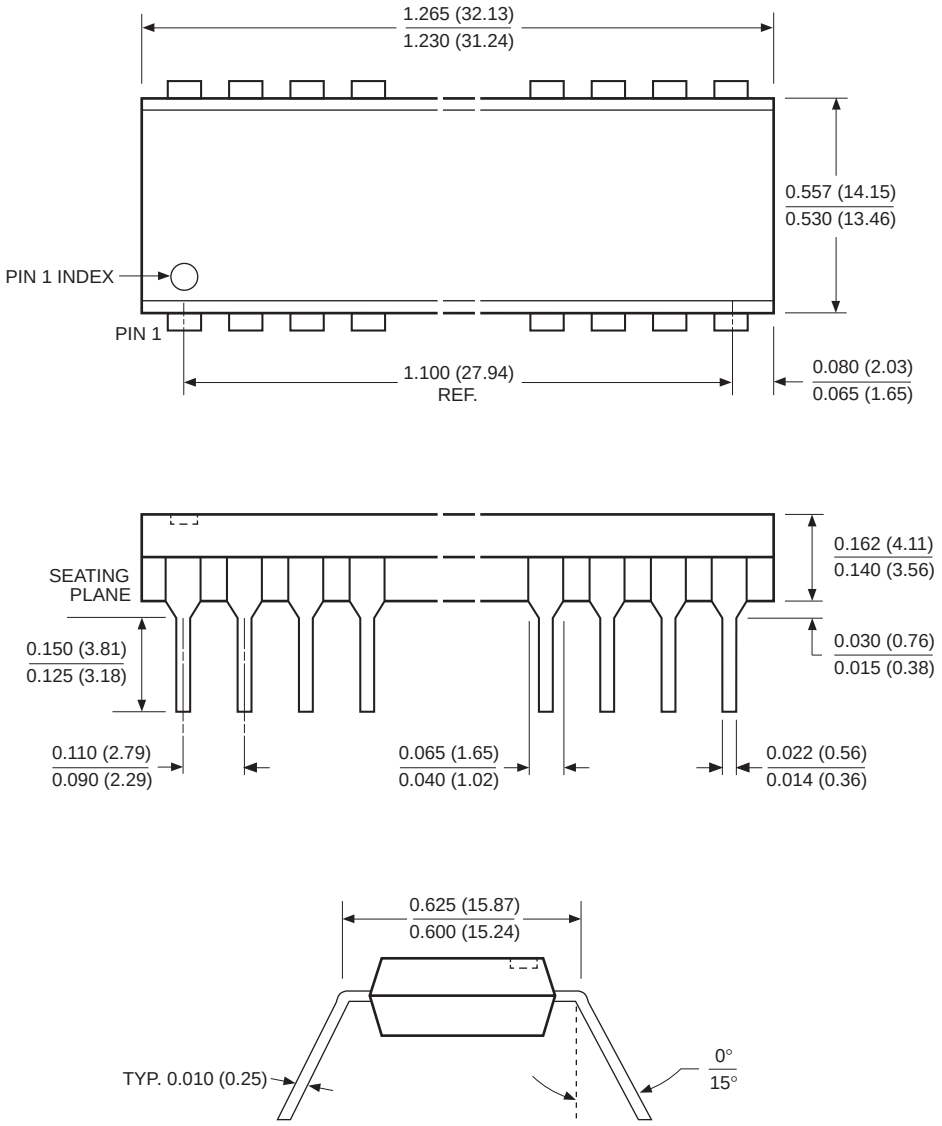


Normalized Access Time vs. Ambient Temperature



PACKAGING INFORMATION

24-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

3926 FHD F03

ORDERING INFORMATION