NEC

MOS INTEGRATED CIRCUIT

μPD78P054

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD78P054 is a product in the μPD78054 subseries within the 78K/0 series, in which the on-chip mask ROM of the μPD78054 is replaced with one-time PROM or EPROM.

As the μPD78P054 is user-programmable, it is ideal for evaluation in system development, short-run and multiple-device production, and early start-up.

Caution The μPD78P054KK-T does not maintain planned reliability when used in your device's mass-produced products. Please use only experimentally or for evaluating function during trail manufacture.

Details are given in the following User's Manual, which should be read without fail when carrying out design work.

μPD78054, 78054Y Subseries User's Manual: U11747E
78K/0 Series User's Manual-Instruction : U12326E

FEATURES

- Pin compatible with mask ROM products (except the V_{PP} pin)
- Internal PROM : 32K bytes[Note]
  - μPD78P054KK-T : Reprogrammable (ideal for system evaluation)
  - μPD78P054GC, 78P054GK : Programmable once only (ideal for limited production)
- Internal high-speed RAM : 1024 bytes[Note]
- Buffer RAM : 32 bytes
- Operable in the same supply voltage as mask ROM products (V_{DD} = 2.0 to 6.0 V)
- Corresponding to QTOP™ microcontrollers

Note *Internal PROM and internal high-speed RAM capacities can be changed by memory size switching* register (IMS).

Remarks 1. For the differences between PROM product and mask ROM product, refer to **1. DEFERENCES BETWEEN μPD78P054 AND MASK ROM PRODUCTS**.

2. A QTOP *microcontroller is the general name for a single-chip microcontroller with one-time* PROM for which program writing, marking, screening, and verifying are completely supported by NEC.

In this document, "PROM" is used in parts common to one-time PROM products and EPROM products.

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The mark ★ shows major revised points.

ORDERING INFORMATION

	Part Number	Package	On-Chip ROM	Quantity Grade
	μPD78P054GC-3B9	80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm)	One-time PROM	Standard
★	μPD78P054GC-8BT[Note]	80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm)	One-time PROM	Standard
	μPD78P054GK-BE9	80-pin plastic TQFP(fine pitch) (12 × 12 mm)	One-time PROM	Standard
	μPD78P054KK-T	80-pin ceramic WQFN	EPROM	Unapplicable (For functional evaluation)

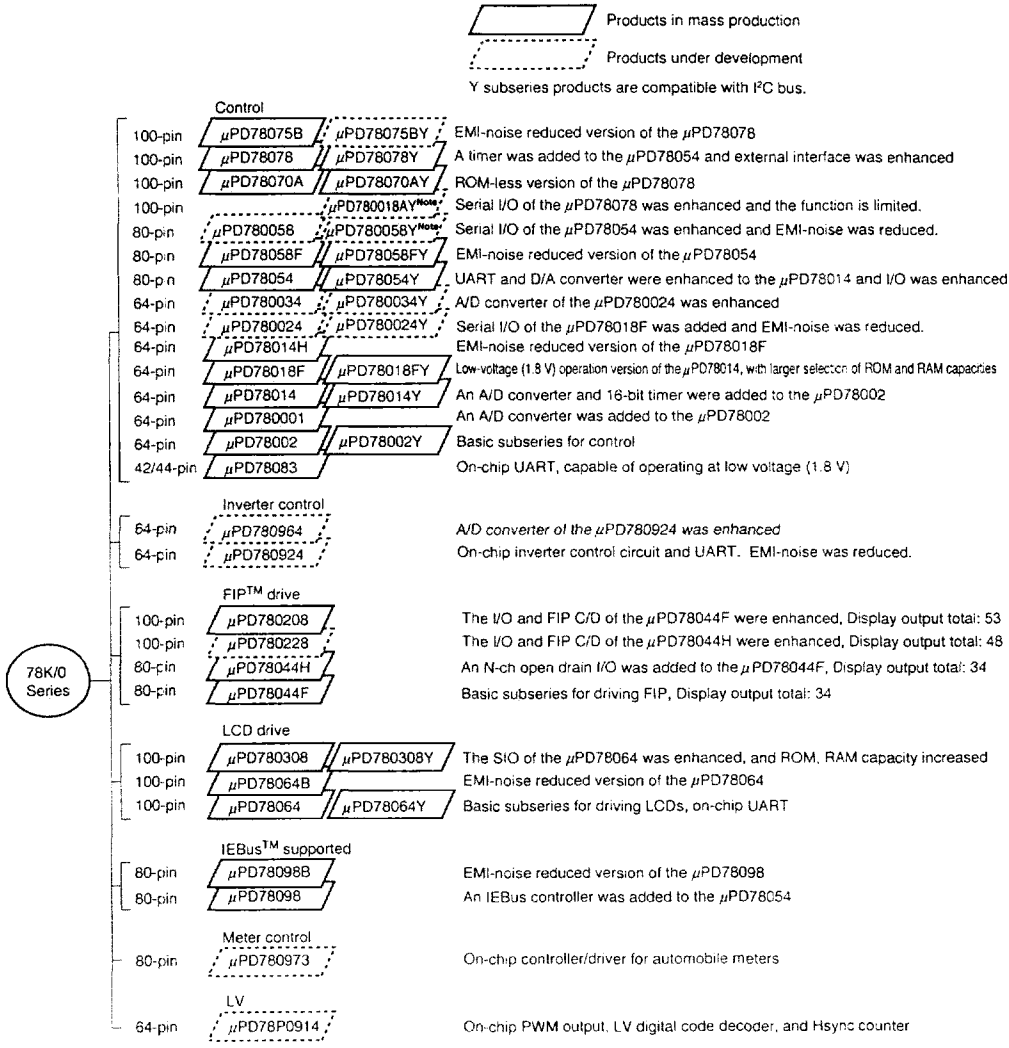
Note Under development

★ **Caution Two types of package of the μPD78P054GC are available (refer to 10. PACKAGE DRAWINGS). For the suppliable packages, consult NEC sales personnel.**

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

★ 78K/0 SERIES DEVELOPMENT

The following shows the products organized according to usage. The names in the parallelograms are subseries names.



Note Under planning

The following lists the main functional differences between subseries products.

Subseries Name \ Function		ROM Capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-bit	16-bit	Watch	WDT							
Control	μPD78075B	32K-40K	4ch	1ch	1ch	1ch	8ch	–	2ch	3ch (UART: 1ch)	88	1.8 V	○
	μPD78078	48K-60K											
	μPD78070A	–									61	2.7 V	
	μPD780058	24K-60K	2ch						2ch	3ch (time division UART: 1ch)	68	1.8 V	
	μPD78058F	48K-60K								3ch (UART: 1ch)	69	2.7 V	
	μPD78054	16K-60K										2.0 V	
	μPD780034	8K-32K					–	8ch	–	3ch (UART: 1ch, time division 3-wire: 1ch)	51	1.8 V	
	μPD780024						8ch	–					
	μPD78014H									2ch	53	1.8 V	
	μPD78018F	8K-60K											
	μPD78014	8K-32K										2.7 V	
	μPD780001	8K		–	–					1ch	39		–
	μPD78002	8K-16K			1ch		–				53		○
	μPD78083				–		8ch			1ch (UART: 1ch)	33	1.8 V	–
Inverter control	μPD780964	8K-32K	3ch	**Note**	–	1ch	–	8ch	–	2ch (UART: 2ch)	47	2.7 V	○
	μPD780924						8ch	–					
FIP drive	μPD780208	32K-60K	2ch	1ch	1ch	1ch	8ch	–	–	2ch	74	2.7 V	–
	μPD780228	48K-60K	3ch	–	–					1ch	72	4.5 V	
	μPD78044H	32K-48K	2ch	1ch	1ch						68	2.7 V	
	μPD78044F	16K-40K								2ch			
LCD drive	μPD780308	48K-60K	2ch	1ch	1ch	1ch	8ch	–	–	3ch (time division UART: 1ch)	57	2.0 V	–
	μPD78064B	32K								2ch (UART: 1ch)			
	μPD78064	16K-32K											
IEBus supported	μPD78098B	40K-60K	2ch	1ch	1ch	1ch	8ch	–	2ch	3ch (UART: 1ch)	69	2.7 V	○
	μPD78098	32K-60K											
Meter control	μPD780973	24K-32K	3ch	1ch	1ch	1ch	5ch	–	–	2ch (UART: 1ch)	56	4.5 V	–
LV	μPD78P0914	32K	6ch	–	–	1ch	8ch	–	–	2ch	54	4.5 V	○

Note 10-bit timer: 1 channel

FUNCTION DESCRIPTION

Item		Function
Internal memory		• PROM : 32K bytes[Note 1] • RAM High-speed RAM : 1024 bytes[Note 1] Buffer RAM : 32 bytes
Memory space		64K bytes
General register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Instruction cycles		Instruction execution time variable function is built in.
When main system clock is selected		0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs/12.8 μs (when operating at 5.0 MHz)
When subsystem clock is selected		122 μs (when operating at 32.768 kHz)
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD correction, etc.
I/O ports		Total : 69 • CMOS input : 2 • CMOS input/output : 63 • N-ch open-drain input/output : 4
A/D converter		• 8-bit resolution × 8 ch
D/A converter		• 8-bit resolution × 2 ch
Serial interface		• 3-wire serial I/O/SBI/2-wire serial I/O mode selectable : 1 ch • 3-wire serial I/O mode : 1 ch (with on-chip max. 32-byte auto transmitting/receiving function) • 3-wire serial I/O/UART mode selectable : 1 ch
Timer		• 16-bit timer/event counter : 1 ch • 8-bit timer/event counter : 2 ch • Watch timer : 1 ch • Watchdog timer : 1 ch
Timer output		3 pins (14-bit PWM output enable: 1 pin)
Clock output		19.5 kHz, 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, and 5.0 MHz (At main system clock: 5.0 MHz) 32.768 kHz (At subsystem clock: 32.768 kHz)
Buzzer output		1.2 kHz, 2.4 kHz, 4.9 kHz and 9.8 kHz (At main system clock: 5.0 MHz)
Vectored interrupt sources	Maskable	Internal: 13, external: 7
	Non-maskable	Internal: 1
	Software	1
Test input		Internal: 1, external: 1
Supply voltage		V_{DD} = 2.0 to 6.0 V
Operating ambient temperature		T_A = −40 to 85 °C
Packages		• 80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm) • 80-pin plastic QFP[Note 2] (14 × 14 mm, resin thickness 1.4 mm) • 80-pin plastic TQFP (fine pitch) (12 × 12 mm) • 80-pin ceramic WQFN

★

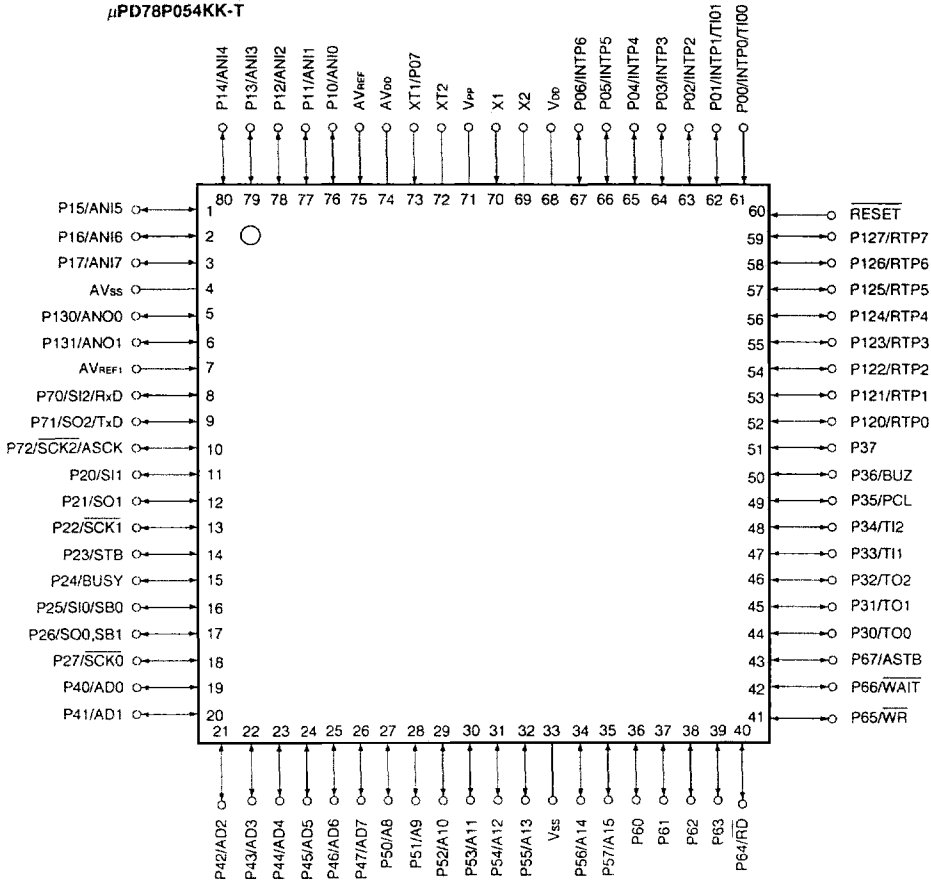
Notes 1. Internal PROM/internal high-speed RAM capacity can be changed by memory size switching register (IMS).

2. Under development

PIN CONFIGURATION (TOP VIEW)

(1) Normal Operating Mode

- 80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm)
  μPD78P054GC-3B9
- ★ 80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm)
  μPD78P054GC-8BT[Note]
- 80-pin plastic TQFP (fine pitch) (12 × 12 mm)
  μPD78P054GK-BE9
- 80-pin ceramic WQFN
  μPD78P054KK-T



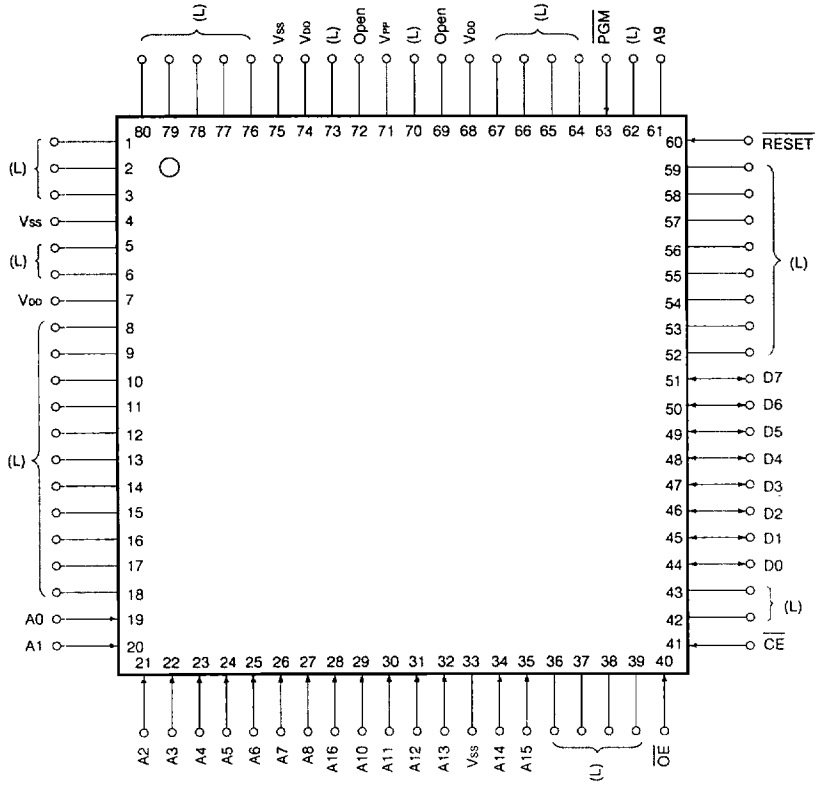
Note Under development

Cautions 1. Connect V_{PP} pin to V_{SS} directly.
2. Connect AV_{DD} pin to V_{DD}.
3. Connect AVss pin to V_{SS}.

A8-A15	:	Address Bus
AD0-AD7	:	Address/ Data Bus
ANI0-ANI7	:	Analog Input
ANO0-ANO1	:	Analog Output
ASCK	:	Asynchronous Serial Clock
ASTB	:	Address Strobe
AV_{DD}	:	Analog Power Supply
AV_{REF0}, AV_{REF1}	:	Analog Reference Voltage
AV_{SS}	:	Analog Ground
BUSY	:	Busy
BUZ	:	Buzzer Clock
INTP0-INTP6	:	Interrupt From Peripherals
P00-P07	:	Port 0
P10-P17	:	Port 1
P20-P27	:	Port 2
P30-P37	:	Port 3
P40-P47	:	Port 4
P50-P57	:	Port 5
P60-P67	:	Port 6
P70-P72	:	Port 7
P120-P127	:	Port 12
P130, P131	:	Port 13
PCL	:	Programmable Clock
$\overline{RD}$	:	Read Strobe
$\overline{RESET}$	:	Reset
RTP0-RTP7	:	Real-Time Output Port
RxD	:	Receive Data
SB0, SB1	:	Serial Bus
$\overline{SCK0}$-$\overline{SCK2}$	:	Serial Clock
SI0-SI2	:	Serial Input
SO0-SO2	:	Serial Output
STB	:	Strobe
TI00, TI01	:	Timer Input
TI1,TI2	:	Timer Input
TO0-TO2	:	Timer Output
TxD	:	Transmit Data
V_{DD}	:	Power Supply
V_{PP}	:	Programming Power Supply
V_{SS}	:	Ground
$\overline{WAIT}$	:	Wait
$\overline{WR}$	:	Write Strobe
X1, X2	:	Crystal (Main System Clock)
XT1, XT2	:	Crystal (Subsystem Clock)

(2) PROM Programming Mode

- 80-pin plastic QFP (14 × 14 mm, resin thickness 2.7 mm)
  μPD78P054GC-3B9
★ - 80-pin plastic QFP (14 × 14 mm, resin thickness 1.4 mm)
  μPD78P054GC-8BT[Note]
- 80-pin plastic TQFP (fine pitch) (12 × 12 mm)
  μPD78P054GK-BE9
- 80-pin ceramic WQFN
  μPD78P054KK-T

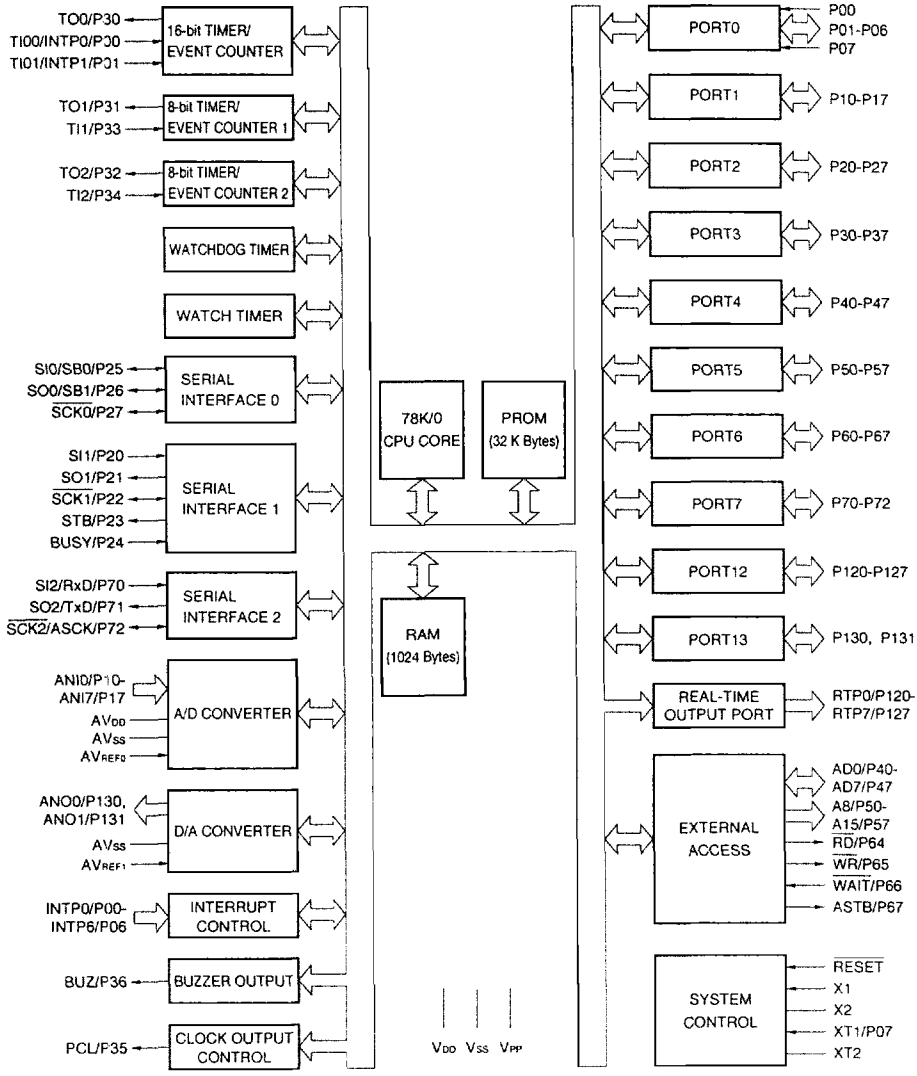


Note Under development

Cautions 1. (L) : Individually connect to Vss via a pull-down resistor.
2. Vss : Connect to GND.
3. $\overline{\text{RESET}}$: Set to low level.
4. Open : No connection

A0 to A16	: Address Bus	$\overline{RESET}$	: Reset
$\overline{CE}$	: Chip Enable	V_{DD}	: Power Supply
D0 to D7	: Data Bus	V_{PP}	: Programming Power Supply
$\overline{OE}$	: Output Enable	V_{SS}	: Ground
$\overline{PGM}$	: Program		

★ BLOCK DIAGRAM



1. DIFFERENCES BETWEEN μPD78P054 AND MASK ROM PRODUCTS

The μPD78P054 is a single-chip microcontroller with an on-chip one-time writable PROM or with an on-chip EPROM which has program write, erasure and rewrite capability.

It is possible to make all the functions except for PROM specification, and mask option of P60 to P63 pins, to the same as those of mask ROM products by setting the memory size switching register (IMS).

Differences between the PROM product (μPD78P054) and mask ROM products (μPD78052, 78053, 78054) are shown in Table 1-1.

Table 1-1. Differences between μPD78P054 and Mask ROM Products

	Item	μPD78P054	Mask ROM Products
★	*Internal ROM structure*	*One-time PROM/EPROM*	*Mask ROM*
★	Internal ROM capacity	32 KB	μPD78052: 16 KB μPD78053: 24 KB μPD78054: 32 KB
★	Changing internal ROM capacity by memory size switching register	Can be changed[Note]	Cannot be changed
	IC pin	No	Yes
	V_{PP} pin	Yes	No
	On-chip pull-up resistor by mask option for pins P60-P63	No	Yes
★	Electrical specification	Refer to data sheet for each product.	

Note The internal PROM becomes to 32K bytes and the internal high-speed RAM becomes 1024 bytes by the $\overline{\text{RESET}}$ input.

★ **Caution Noise resistance and noise radiation are different in PROM version and mask ROM versions. If using a mask ROM version instead of the PROM version for processes between prototype development and full production, be sure to fully evaluate the CS of the mask ROM version (not ES).**

2. PIN FUNCTION TABLE

2.1 PINS IN NORMAL OPERATING MODE

(1) Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Dual-Function Pin
P00	Input	Port 0 8-bit input/output port	Input only	Input	INTP0/TI00
P01	I/O		Input/output is specifiable bit-wise. When used as the input port, it is possible to use a pull-up resistor by software.	Input	INTP1/TI01
P02					INTP2
P03					INTP3
P04					INTP4
P05					INTP5
P06					INTP6
P07[Note1]	Input		Input only	Input	XT1
P10-P17	I/O	Port 1 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to use a pull-up resistor by software[Note2].		Input	ANI0-ANI7
P20	I/O	Port 2 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to use a pull-up resistor by software.		Input	SI1
P21					SO1
P22					$\overline{SCK1}$
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					$\overline{SCK0}$
P30	I/O	Port 3 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to use a pull-up resistor by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—

Notes 1. When P07/XT1 pins are used as the input ports, set the processor clock control register (PCC) bit 6(FRC) to 1. (Be sure not to use the on-chip feedback resistor of the subsystem clock oscillation circuit.)

2. When P10/ANI0 to P17/ANI7 pins are used as the analog inputs for A/D converter, an on-chip pull-up resistor becomes automatically unused.

(1) Port Pins (2/2)

Pin Name	I/O	Function		After Reset	Dual-Function Pin
P40-P47	I/O	Port 4 8-bit input/output port Input/output is specifiable as 8-bit unit. When used as the input port, it is possible to use a pull-up resistor by software. Set test input flag(KRIF) to 1 by falling edge detection.		Input	AD0 to AD7
P50-P57	I/O	Port 5 8-bit input/output port It is possible to directly drive LED. Input/output is specifiable bit-wise. When used as the input port, it is possible to use a pull-up resistor by software.		Input	A8 to A15
P60	I/O	Port 6 3-bit input/output port Input/output is specifiable bit-wise.	N-ch open-drain input/output port. It is possible to directly drive LED.	Input	—
P61					
P62					
P63					
P64			When used as the input port, it is possible to use a pull-up resistor by software.	Input	$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB
P70	I/O	Port 7 3-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to use a pull-up resistor by software.		Input	SI2/RxD
P71					SO2/TxD
P72					$\overline{SCK2}$/ASCK
P120-P127	I/O	Port 12 8-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to use a pull-up resistor by software.		Input	RTP0 to RTP7
P130, P131	I/O	Port 13 2-bit input/output port Input/output is specifiable bit-wise. When used as the input port, it is possible to use a pull-up resistor by software.		Input	ANO0, ANO1

(2) Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Dual-Function Pin
INTP0	Input	External interrupt request inputs, with specifiable valid edges (rising edge, falling edge, and both rising and falling edges).	Input	P00/TI00
INTP1				P01/TI01
INTP2				P02
INTP3				P03
INTP4				P04
INTP5				P05
INTP6				P06
SI0	Input	Serial data input of the serial interface	Input	P25/SB0
SI1				P20
SI2				P70/RxD
SO0	Output	Serial data output of the serial interface	Input	P26/SB1
SO1				P21
SO2				P71/TxD
SB0	I/O	Serial data input/output of the serial interface	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	I/O	Serial clock input/output of the serial interface	Input	P27
$\overline{SCK1}$				P22
$\overline{SCK2}$				P72/ASCK
STB	Output	Automatic transmitting/receiving strobe output of the serial interface	Input	P23
BUSY	Input	Automatic transmitting/receiving busy input of the serial interface	Input	P24
RxD	Input	Serial data input for asynchronous serial interface	Input	P70/SI2
TxD	Output	Serial data output for asynchronous serial interface	Input	P71/SO2
ASCK	Input	Serial clock input for asynchronous serial interface	Input	P72/$\overline{SCK2}$
TI00	Input	External count clock input to 16-bit timer (TM0)	Input	P00/INTP0
TI01		Capture trigger signal input to capture register (CR00)		P01/INTP1
TI1		External count clock input to 8-bit timer (TM1)		P33
TI2		External count clock input to 8-bit timer (TM2)		P34
TO0	Output	16-bit timer (TM0) output (dual-function as 14-bit PWM output)	Input	P30
TO1		8-bit timer (TM1) output		P31
TO2		8-bit timer (TM2) output		P32
PCL	Output	Clock output (for trimming main system clock and subsystem clock)	Input	P35
BUZ	Output	Buzzer output	Input	P36
RTP0-RTP7	Output	Real-time output port which outputs data in synchronization with trigger.	Input	P120-P127
AD0-AD7	I/O	Low order address/data bus when expanding memory to the outside.	Input	P40-P47
A8-A15	Output	High order address bus when expanding memory to the outside.	Input	P50-P57

(2) Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Dual-Function Pin
$\overline{RD}$	Output	Strobe signal output for the external memory read operation	Input	P64
$\overline{WR}$		Strobe signal output for the external memory write operation	Input	P65
$\overline{WAIT}$	Input	Wait insertion when accessing external memory	Input	P66
ASTB	Output	Strobe output to externally latches address information which is output to ports 4 and 5 for accessing external memory.	Input	P67
ANI0-ANI7	Input	Analog input of A/D converter	Input	P10-P17
ANO0, ANO1	Output	Analog output of D/A converter	Input	P130, P131
AV_{REF0}	Input	Reference voltage input of A/D converter	—	—
AV_{REF1}	Input	Reference voltage input of D/A converter	—	—
AV_{DD}	—	*Analog power supply of A/D converter. Connect to* V_{DD}	—	—
★ AV_{SS}	—	Ground potential of A/D, D/A converter. Connect to Vss	—	—
$\overline{RESET}$	Input	System reset input	—	—
X1	Input	Main system clock oscillation crystal connection	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection	Input	P07
XT2	—		—	—
V_{DD}	—	*Positive power supply*	—	—
V_{PP}	—	High-voltage applied during program write/verification. Connected to Vss directly in normal operating mode	—	—
V_{SS}	—	Ground potential	—	—

2.2 PINS IN PROM PROGRAMMING MODE

Pin Name	I/O	Function
$\overline{RESET}$	Input	PROM programming mode setting When +5 V or +12.5 V is applied to the V_{PP} pin and a low level signal is applied to the $\overline{RESET}$ pin, this chip is set in the PROM programming mode.
V_{PP}	Input	PROM programming mode setting and high-voltage applied during program write/verification
A0-A16	Input	Address bus
D0-D7	Input/output	Data bus
$\overline{CE}$	Input	PROM enable input/program pulse input
$\overline{OE}$	Input	Read strobe input to PROM
$\overline{PGM}$	Input	Program/program inhibit input in PROM programing mode.
V_{DD}	—	Positive power supply
V_{SS}	—	Ground potential

2.3 PIN INPUT/OUTPUT CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

Types of input/output circuits of the pins and recommended connection of unused pins are shown in Table 2-1. For the configuration of each type of input/output circuit, refer to **Figure 2-1**.

Table 2-1. Type of Input/Output Circuit of Each Pin (1/2)

Pin Name	I/O Circuit Type	I/O	Recommended Connecting Method when Unused
P00/INTP0/TI00	2	Input	Connect to V_{SS}.
P01/INTP1/TI01	8-A	I/O	Independently connected to V_{SS} through resistor.
P02/INTP2			
P03/INTP3			
P04/INTP4			
P05/INTP5			
P06/INTP6			
★ P07/XT1	16	Input	Connect to V_{DD}.
P10/ANI0-P17/ANI7	11	I/O	Independently connected to V_{DD} or V_{SS} through resistor.
P20/SI1	8-A		
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/$\overline{SCK0}$			
P30/TO0	5-A		
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0-P47/AD7	5-E		Independently connected to V_{DD} through resistor.
P50/A8-P57/A15	5-A		Independently connected to V_{DD} or V_{SS} through resistor.
P60-P63	13-D		Independently connected to V_{DD} through resistor.
P64/$\overline{RD}$	5-A		Independently connected to V_{DD} or V_{SS}.
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			

Table 2-1. Type of Input/Output Circuit of Each Pin (2/2)

Input/Output	I/O Circuit Type	I/O	Recommended Connecting Method when Unused
P70/SI2/RxD	8-A	I/O	Independently connected to V_{DD} or V_{SS}.
P71/SO2/TxD	5-A		
P72/$\overline{SCK2}$/ASCK	8-A		
P120/RTP0-P127/RTP7	5-A		
P130/ANO0, P131/ANO1	12-A		Independently connected to Vss through resistor.
$\overline{RESET}$	2	Input	—
XT2	16	—	Leave open
AV_{REF0}	—		Connect to V_{SS}
AV_{REF1}			Connect to V_{DD}
AV_{DD}			
AV_{SS}			Connect to V_{SS}
★ V_{PP}			Connect to V_{SS} directly

Figure 2-1. List of Pin Input/Output Circuits (1/2)

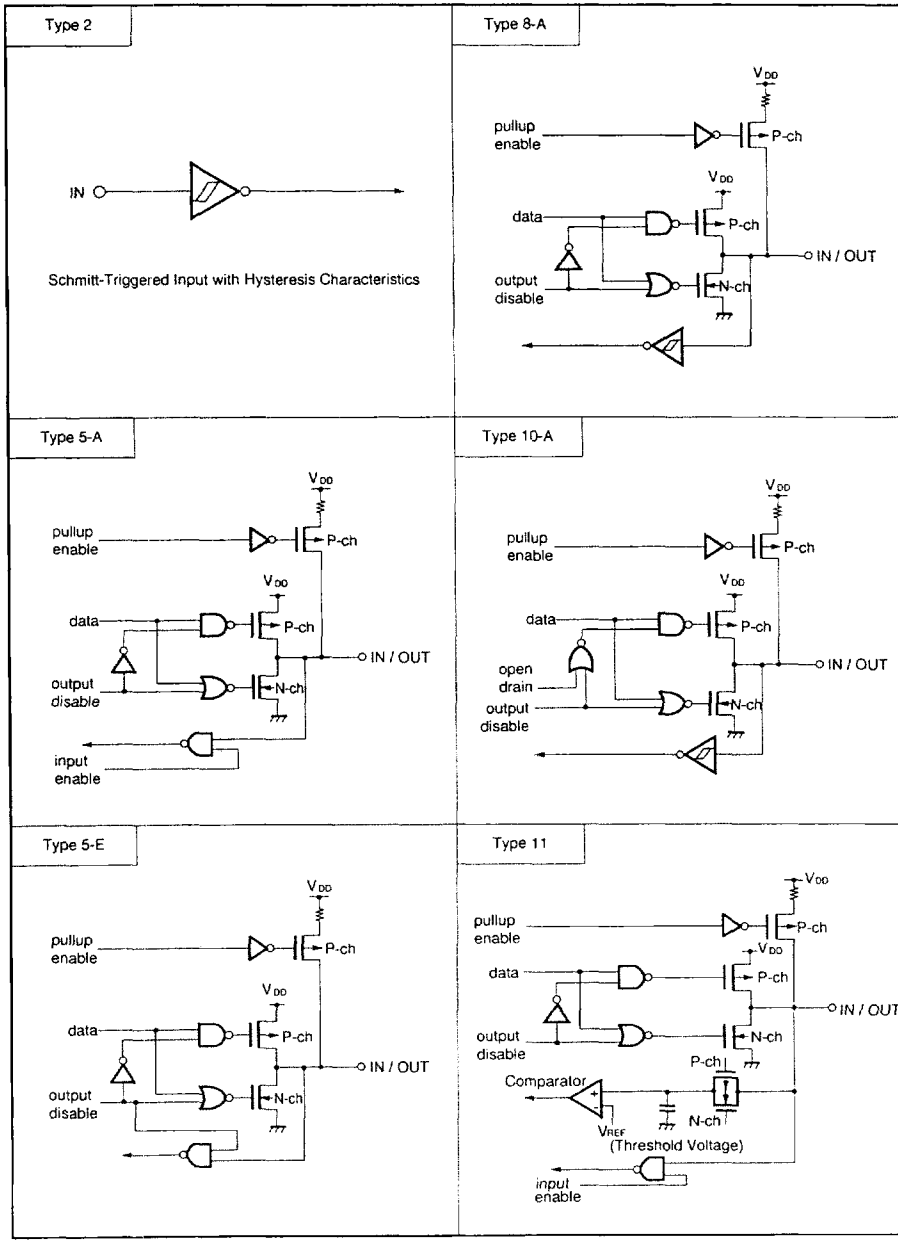
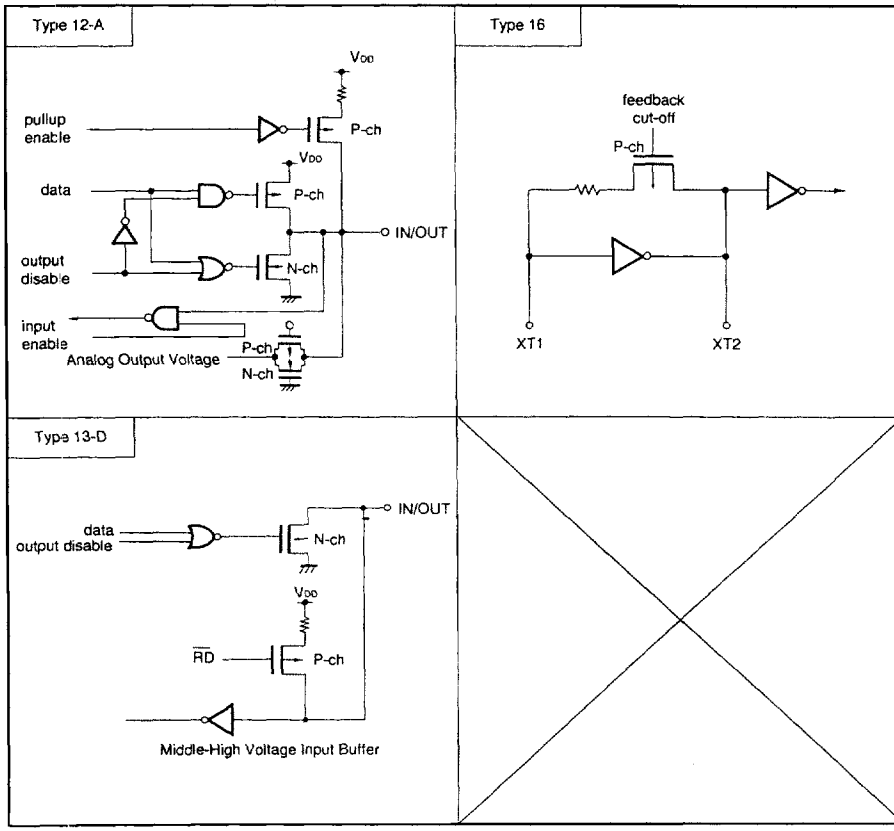


Figure 2-1. List of Pin Input/Output Circuits (2/2)



3. MEMORY SIZE SWITCHING REGISTER (IMS)

This is a register to disable use of part of internal memories by software. By setting this memory size switching register (IMS), it is possible to get the same memory mapping as that of mask ROM product having different internal memories (ROM, RAM).

The IMS is set up by the 8-bit memory manipulation instruction.

C8H will result by the $\overline{\text{RESET}}$ input.

Figure 3-1. Memory Size Switching Register Format

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	C8H	R/W

ROM3	ROM2	ROM1	ROM0	Selection of Internal ROM Capacity
0	1	0	0	16K bytes
0	1	1	0	24K bytes
1	0	0	0	32K bytes
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Selection of Internal High-Speed RAM Capacity
0	1	0	512 bytes
1	1	0	1024 bytes
Other than above			Setting prohibited

Table 3-1 shows the setting values of IMS which makes the memory mapping the same as that of the various mask ROM products.

Table 3-1. Memory Size Switching Register Setting Values

Target Mask ROM Product	IMS Setting Value
μPD78052	44H
μPD78053	C6H
μPD78054	C8H

4. PROM PROGRAMMING

The μPD78P054 has an on-chip 32-Kbyte PROM as a program memory. For programming, set the PROM programming mode by the V_{PP} and $\overline{RESET}$ pins. For connecting unused pins, refer to **PIN CONFIGURATION (TOP VIEW) (2) PROM Programming Mode**.

Caution Program writing should be performed in the address range 0000H to 7FFFH (the last address, 7FFFH, should be specified). Writing cannot be performed with a PROM programmer that cannot specify the write addresses.

4.1 OPERATING MODES

When +5 V or +12.5 V is applied to the V_{PP} pin and a low level signal is applied to the $\overline{RESET}$ pin, the PROM programming mode is set. This mode will become the operating mode as shown in Table 4-1 when the $\overline{CE}$, $\overline{OE}$ and $\overline{PGM}$ pins are set as shown.

Further, when the read mode is set, it is possible to read the contents of the PROM.

Table 4-1. Operating Modes of PROM Programming

Pin / Operating Mode	$\overline{RESET}$	V_{PP}	V_{DD}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	D0 to D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High-impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				×	H	H	High-impedance
				×	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	×	High-impedance
Standby				H	×	×	High-impedance

×: L or H

(1) Read mode

Read mode is set if $\overline{CE}$ = L, $\overline{OE}$ = L is set.

(2) Output disable mode

Data output becomes high-impedance, and is in the output disable mode, if $\overline{OE}$ = H is set.

Therefore, it allows data to be read from any device by controlling the $\overline{OE}$ pin, if multiple μPD78P054s are connected to the data bus.

(3) Standby mode

Standby mode is set if $\overline{CE}$ = H is set.

In this mode, data outputs become high-impedance irrespective of the $\overline{OE}$ status.

(4) Page data latch mode

Page data latch mode is set if $\overline{CE}$ = H, $\overline{PGM}$ = H, $\overline{OE}$ = L are set at the beginning of page write mode.

In this mode, 1 page 4-byte data is latched in an internal address/data latch circuit.

(5) Page write mode

After 1 page 4 bytes of addresses and data are latched in the page data latch mode, a page write is executed by applying a 0.1 ms program pulse (active low) to the $\overline{PGM}$ pin with $\overline{CE}$ = H, $\overline{OE}$ = H. Then, program verification can be performed, if $\overline{CE}$ = L, $\overline{OE}$ = L are set.

If programming is not performed by a one-time program pulse, X (X ≤ 10) write and verification operations should be executed repeatedly.

(6) Byte write mode

Byte write is executed when a 0.1 ms program pulse (active low) is applied to the $\overline{PGM}$ pin with $\overline{CE}$ = L, $\overline{OE}$ = H. Then, program verification can be performed if $\overline{OE}$ = L is set.

If programming is not performed by a one-time program pulse, X (X ≤ 10) write and verification operations should be executed repeatedly.

(7) Program verify mode

Program verify mode is set if $\overline{CE}$ = L, $\overline{PGM}$ = H, $\overline{OE}$ = L are set.

In this mode, check if a write operation is performed correctly, after the write.

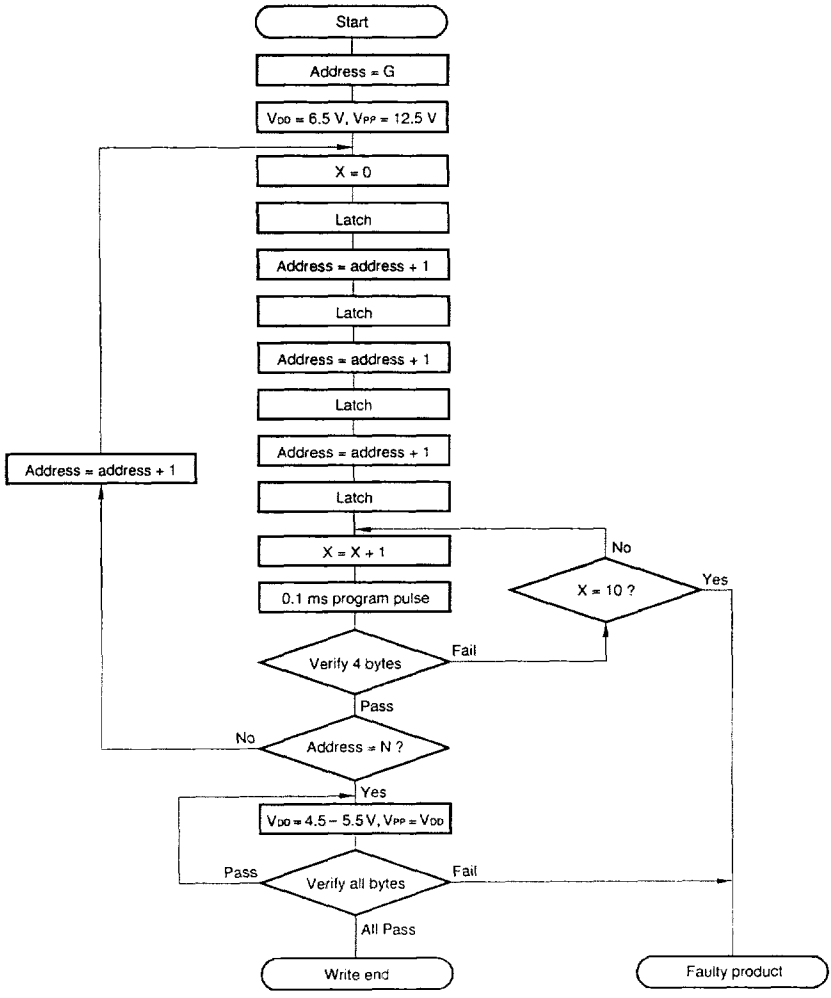
(8) Program inhibit mode

Program inhibit mode is used when the $\overline{OE}$ pin, V_{PP} pin and D0 to D7 pins of multiple μPD78P054s are connected in parallel and a write is performed to one of those devices.

When a write operation is performed, the page write mode or byte write mode described above is used. At this time, a write is not performed to a device which has the $\overline{PGM}$ pin driven high.

4.2 PROM WRITE PROCEDURE

Figure 4-1. Page Program Mode Flow Chart



G = Start address

N = Program last address

Figure 4-2. Page Program Mode Timing

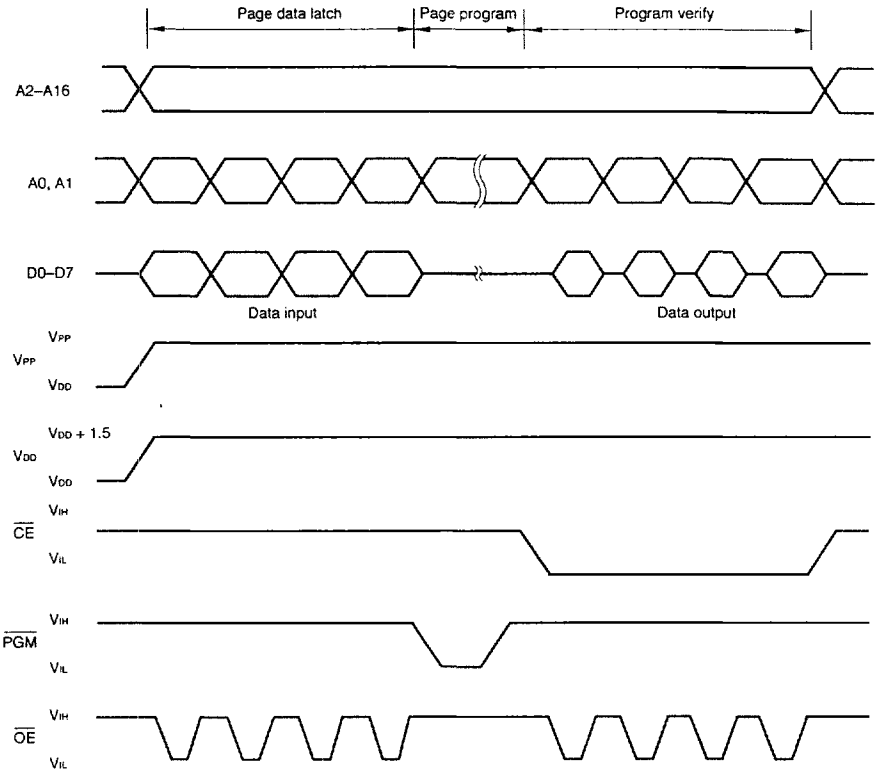
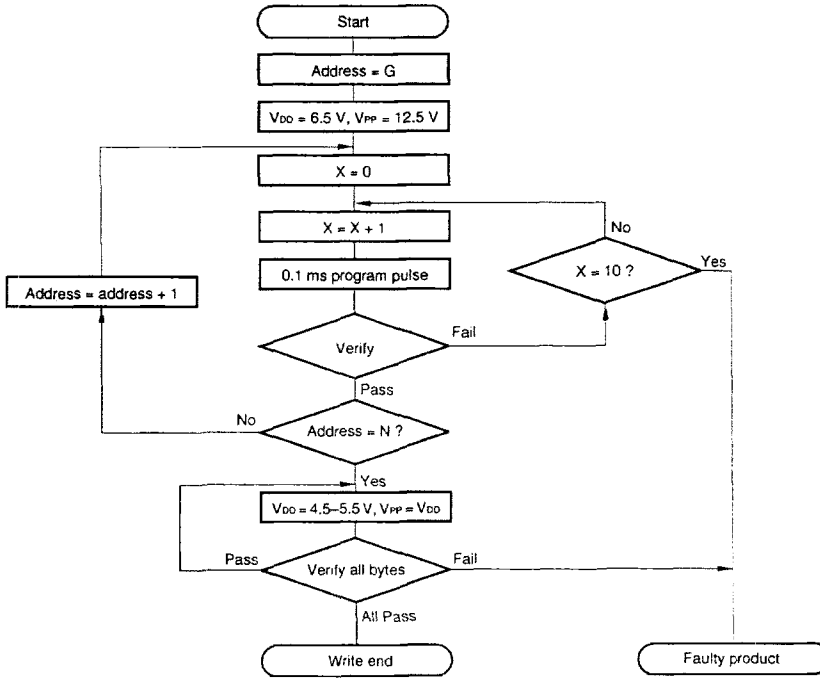
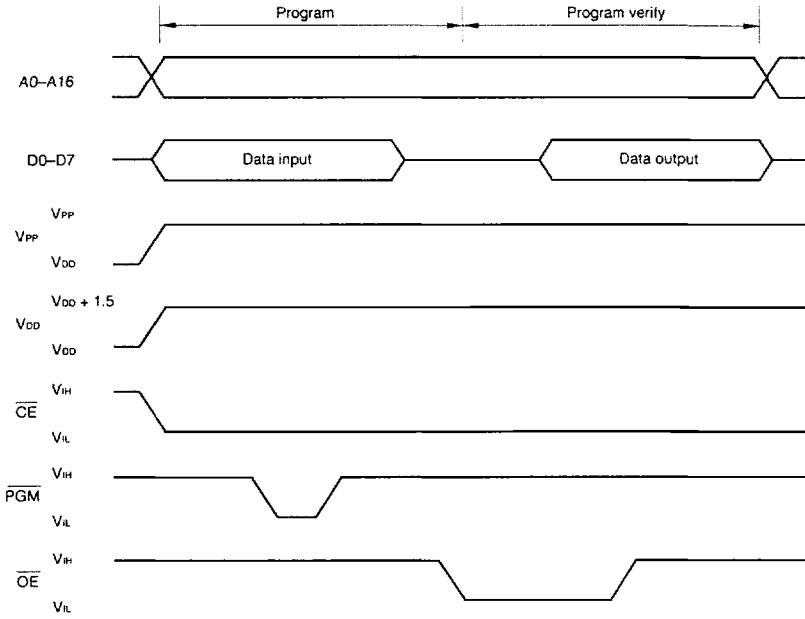


Figure 4-3. Byte Program Mode Flow Chart



G = Start address
N = Program last address

Figure 4-4. Byte Program Mode Timing



Cautions 1. V_{DD} should be applied before V_{PP} and cut after V_{PP}.

2. V_{PP} must not exceed +13.5 V including overshoot.

3. Reliability may be adversely affected if removal/reinsertion is performed while +12.5 V is being applied to V_{PP}.

4.3 PROM READ PROCEDURE

The contents of PROM are readable to the external data bus (D0 to D7) according to the read procedure shown below.

(1) Fix the $\overline{\text{RESET}}$ pin at low level, supply +5 V to the VPP pin, and connect all other unused pins as shown in **PIN CONFIGURATION (TOP VIEW) (2) PROM Programming Mode.**

(2) Supply +5 V to the V_{DD} and V_{PP} pins.

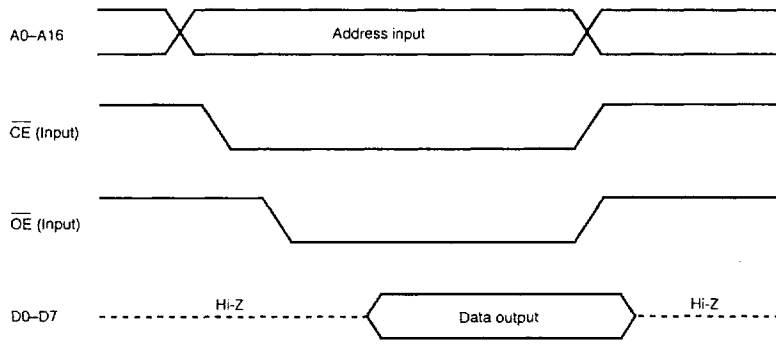
(3) Input address of read data into the A0 to A16 pins.

(4) Read mode

(5) Output data to D0 to D7 pins.

The timings of the above steps (2) to (5) are shown in Figure 4-5.

Figure 4-5. PROM Read Timings



5. ERASURE METHOD (μPD78P054KK-T ONLY)

The μPD78P054KK-T is capable of erasing (FFH) the contents of data written in a program memory and rewriting.

When erasing the contents of data, irradiate light having a wavelength of less than about 400 nm to the erasing window. Normally, irradiate ultraviolet rays of 254 nm wavelength. Volume of irradiation required to completely erase the contents of data is as follows:

★ • UV intensity × erasing time : 30 W•s/cm^2 or more

★ • Erasing time : 40 minutes MIN. (When a UV lamp of 12,000 μW/cm^2 is used. However, a longer time may be needed because of deterioration in performance of the UV lamp, contamination of the erasing window, etc.)

When erasing the contents of data, set up the UV lamp within 2.5 cm from the erasing window. Further, if a filter is provided for a UV lamp, irradiate the ultraviolet rays after removing the filter.

6. ERASURE WINDOW SEAL (μPD78P054KK-T ONLY)

To protect from miserasure by rays other than that of the lamp for erasing EPROM contents, or to protect internal circuit other than EPROM from misoperating by rays, stick a protection seal on the erasure window when EPROM contents erasure is not performed.

7. ONE-TIME PROM PRODUCTS SCREENING

The one-time PROM product (μPD78P054GC-3B9, 78P054GC-8BT, 78P054GK-BE9) can not be tested completely by NEC before it is shipped, because of its structure. It is recommended to perform screening to verify PROM after writing necessary data and performing high-temperature storage under the condition below.

Storage Temperature	Storage Time
125 °C	24 hours

At present, a fee is charged by NEC for one-time PROM after-programming imprinting, screening, and verify service for the QTOP Microcomputer. For details, contact your sales representative.

8. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

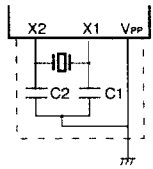
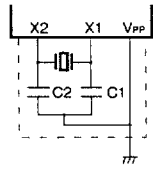
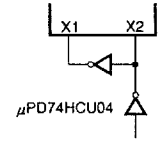
Parameter	Symbol	Test Conditions			Rating	Unit
Supply voltage	V_{DD}				−0.3 to +7.0	V
	V_{PP}				−0.3 to +13.5	V
	AV_{DD}				−0.3 to V_{DD} +0.3	V
	AV_{REF0}				−0.3 to V_{DD} +0.3	V
	AV_{REF1}				−0.3 to V_{DD} +0.3	V
	AV_{SS}				−0.3 to +0.3	V
Input voltage	V_{I1}	P00-P07, P10-P17, P20-P27, P30-P37, P40-47, P50-P57, P64-P67, P70-P72, P120-P127, P130, P131, X1, X2, XT2, $\overline{\text{RESET}}$			−0.3 to V_{DD} +0.3	V
	V_{I2}	P60-P63	N-ch open drain		−0.3 to +16	V
	V_{I3}	A9			−0.3 to +13.5	V
Output voltage	V_O				−0.3 to V_{DD} +0.3	V
Analog input voltage	V_{AN}	P10-P17	Analog input pins		AV_{SS} −0.3 to AV_{REF0} +0.3	V
Output current high	I_{OH}	1 pin			−10	mA
		Total for P01-P06, P30-P37, P56, P57, P60-P67, P120-P127			−15	mA
		Total for P10-P17, P20-P27, P40-P47, P50-P55, P70-P72, P130, P131			−15	mA
Output current low	I_{OL}[Note]	1 pin		Peak value	30	mA
				r.m.s. value	15	mA
		Total for P50-P55		Peak value	100	mA
				r.m.s. value	70	mA
		Total for P56, P57, P60-P63		Peak value	100	mA
				r.m.s. value	70	mA
		Total for P10-P17, P20-P27, P40-P47, P70-P72, P130, P131		Peak value	50	mA
				r.m.s. value	20	mA
		Total for P01-P06, P30-P37, P64-P67, P120-P127		Peak value	50	mA
				r.m.s. value	20	mA
Operating ambient temperature	T_A				−40 to +85	°C
Storage temperature	Tstg				−65 to +150	°C

Note The r.m.s. value should be calculated as follows: [r.m.s. value] = [Peak value] × $\sqrt{\text{Duty}}$

Caution Product quality may suffer if the absolute maximum rating is exceeded for even a single parameter, or even momentarily. In other words, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions which ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, dual-function pin characteristics are the same as port pin characteristics.

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note1	V_{DD} = Oscillation voltage range	1.0		5.0	MHz
		Oscillation stabilization timeNote2	After V_{DD} has reached MIN. of oscillation voltage range			4	ms
Crystal resonator		Oscillation frequency (f_X)Note1		1.0		5.0	MHz
		Oscillation stabilization timeNote2	V_{DD} = 4.5 to 6.0 V			10	ms
						30	
External clock		X1 input frequency (f_X)Note1		1.0		5.0	MHz
		X1 input high-/low-level width (t_{XH}/t_{XL})		85		500	ns

Notes 1. Only the oscillator characteristics are shown. Refer to the **AC characteristics** for instruction execution times.

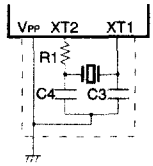
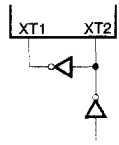
2. This is the time required for oscillation to stabilize after a reset or STOP mode release.

Cautions 1. When the main system clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a broken line to prevent the influence of wiring capacitance, etc.

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as V_{SS}.**
- **Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

2. When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Resonator	Recommended Circuit	Parameter	Test Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)[Note1]		32	32.768	35	MHz
		Oscillation stabilization time[Note2]	V_{DD} = 4.5 to 6.0 V		1.2	2	ms
						10	
External clock		X1 input frequency (f_X)[Note1]		32		100	MHz
		X1 input high-/low-level width (t_{XH}/t_{XL})		5		15	μs

Notes 1. Only the oscillator characteristics are shown. Refer to the **AC characteristics** for instruction execution times.

2. This is the time required for oscillation to stabilize after power (V_{DD}) is turned on.

Cautions 1. When the subsystem clock oscillator is used, the following should be noted concerning wiring in the area in the figure enclosed by a broken line to prevent the influence of wiring capacitance, etc.

- **The wiring should be kept as short as possible.**
- **No other signal lines should be crossed.**
- **Keep away from lines carrying a high fluctuating current.**
- **The oscillator capacitor grounding point should always be at the same potential as VSS.**
- **Do not connect to a ground pattern carrying a high current.**
- **A signal should not be taken from the oscillator.**

2. The subsystem clock oscillator is a low-amplitude circuit in order to achieve a low consumption current, and is more prone to misoperation due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

RECOMMENDED OSCILLATOR CONSTANT

MAIN SYSTEM CLOCK: CERAMIC RESONATOR (T_A = −40 to +85°C)

Manufacturer	Product Name	Frequency	Recommended Circuit Constant		Oscillation Voltage Range	
		(MHz)	C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
TDK Corp.	CCR4.0MC3	4.0	Built-in	Built-in	2.0	6.0
	CCR5.0MC3	5.0	Built-in	Built-in	2.0	6.0

SUBSYSTEM CLOCK: CRYSTAL RESONATOR (T_A = −40 to +85°C)

Manufacturer	Product Name	Frequency	Recommended Circuit Constant			Oscillation Voltage Range	
		(MHz)	C3 (pF)	C4 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)
Daishinku Corp.	DT-38 (1TA252E00, load capacitance 12.5 pF)	32.768	22	22	330	2.0	6.0

CAPACITANCE (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
Input/output capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0	P01-P06, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67, P70-P72, P120-P127, P130, P131			15	pF
			P60-P63			20	pF

★ **Caution The oscillation circuit constants and oscillation voltage range indicate conditions for stable oscillation but do not guarantee accuracy of the oscillation frequency. If the application circuit requires accuracy of the oscillation frequency, it is necessary to set the oscillation frequency in the application circuit. For this, it is necessary to directly contact the manufacturer of the resonator being used.**

Remark Unless specified otherwise, dual-function pin characteristics are the same as port pin characteristics.

DC CHARACTERISTICS (T_A = −40 to +85°C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH1}	P10-P17, P21, P23, P30-P32, P35-P37, P40-P47, P50-P57, P64-P67, P71, P120-P127, P130, P131	V_{DD} = 2.7 to 6.0 V	0.7V_{DD}		V_{DD}	V
				0.8V_{DD}		V_{DD}	V
	V_{IH2}	P00-P06, P20, P22, P24-P27, P33, P34, P70, P72, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 6.0 V	0.8V_{DD}		V_{DD}	V
				0.85V_{DD}		V_{DD}	V
	V_{IH3}	P60-P63 (N-ch open drain)	V_{DD} = 2.7 to 6.0 V	0.7V_{DD}		15	V
				0.8V_{DD}		15	V
	V_{IH4}	X1, X2	V_{DD} = 2.7 to 6.0 V	V_{DD} −0.5		V_{DD}	V
				V_{DD} −0.2		V_{DD}	V
	V_{IH5}	XT1/P07, XT2	4.5 V ≤ V_{DD} ≤ 6.0 V	0.8V_{DD}		V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0.9V_{DD}		V_{DD}	V
			2.0 V ≤ V_{DD} < 2.7 V[Note]	0.9V_{DD}		V_{DD}	V
Input voltage low	V_{IL1}	P10-P17, P21, P23, P30-P32, P35-P37, P40-P47, P50-P57, P64-P67, P71, P120-P127, P130, P131	V_{DD} = 2.7 to 6.0 V	0		0.3 V_{DD}	V
				0		0.2 V_{DD}	V
	V_{IL2}	P00-P06, P20, P22, P24-P27, P33, P34, P70, P72, $\overline{\text{RESET}}$	V_{DD} = 2.7 to 6.0 V	0		0.2 V_{DD}	V
				0		0.15 V_{DD}	V
	V_{IL3}	P60-P63	4.5 V ≤ V_{DD} ≤ 6.0 V	0		0.3 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.2 V_{DD}	V
				0		0.1 V_{DD}	V
	V_{IL4}	X1, X2	V_{DD} = 2.7 to 6.0 V	0		0.4	V
						0.2	V
	V_{IL5}	XT1/P07, XT2	4.5 V ≤ V_{DD} ≤ 6.0 V	0		0.2 V_{DD}	V
			2.7 V ≤ V_{DD} < 4.5 V	0		0.1 V_{DD}	V
			2.0 V ≤ V_{DD} < 2.7 V[Note]	0		0.1 V_{DD}	V
Output voltage high	V_{OH1}	V_{DD} = 4.5 to 6.0 V, I_{OH} = −1 mA		V_{DD} −1.0			V
		I_{OH} = −100 μA		V_{DD} −0.5			V
Output voltage low	V_{OL1}	P50-P57, P60-P63	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA		0.4	2.0	V
		P01-P06, P10-P17, P20-P27, P30-P37, P40-P47, P64-P67, P70-P72, P120-P127, P130, P131	V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{\text{SCK0}}$	V_{DD} = 4.5 to 6.0 V, N-ch open drain (R= 1kΩ)			0.2 V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V

Note When used as P07, the inverse phase of P07 should be input to XT2 using an inverter.

Remark Unless specified otherwise, dual-function pin characteristics are the same as port pin characteristics.

DC CHARACTERISTICS (T_A = −40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current high	I_{LIH1}	$V_{IN} = V_{DD}$	P00-P06, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P72, P120-P127, P130, P131, $\overline{RESET}$			3	μA
	I_{LIH2}		X1, X2, XT1/P07, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P60-P63			80	μA
Input leakage current low	I_{LIL1}	V_{IN} = 0 V	P00-P06, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67, P70-P72, P120-P127, P130, P131, $\overline{RESET}$			−3	μA
	I_{LIL2}		X1, X2, XT1/P07, XT2			−20	μA
	I_{LIL3}		P60-P63			−3[Note 1]	μA
Output leakage current high	I_{LOH1}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current low	I_{LOL1}	V_{OUT} = 0 V				−3	μA
Software pull-up resistor[Note 2]	R_2	V_{IN} = 0 V, P01-P06, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P64-P67, P70-P72, P120-P127, P130, P131	4.5 V ≤ V_{DD} ≤ 6.0 V	15	40	90	kΩ
			2.7 V ≤ V_{DD} < 4.5 V	20		500	kΩ

Notes 1. For P60 to P63, a low-level input leak current of −200 μA (MAX.) flows only during the 1.5 clocks after an instruction has been executed (no wait) to read out port 6 (P6) or port mode register 6 (PM6). Outside the period of 1.5 clocks following executing a read-out instruction, the current is −3 μA (MAX.).

2. A software pull-up resistor can only be used in the range V_{DD} = 2.7 to 6.0 V.

Remark Unless specified otherwise, dual-function pin characteristics are the same as port pin characteristics.

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

	Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
	Supply current[Note 5]	I_{DD1}	5.0 MHz crystal oscillation operating mode (f_{XX} = 2.5 MHz)[Note 3]	V_{DD} = 5.0V±10%[Note 1]		5	15	mA
				V_{DD} = 3.0V±10%[Note 2]		0.7	2.1	mA
				V_{DD} = 2.2V±10%[Note 2]		0.4	1.2	mA
			5.0 MHz crystal oscillation operating mode (f_{XX} = 5.0 MHz)[Note 4]	V_{DD} = 5.0V±10%[Note 1]		9.0	27.0	mA
				V_{DD} = 3.0V±10%[Note 2]		1.0	3.0	mA
		I_{DD2}	5.0 MHz crystal oscillation HALT mode (f_{XX} = 2.5 MHz)[Note 3]	V_{DD} = 5.0V±10%		1.4	4.2	mA
				V_{DD} = 3.0V±10%		0.5	1.5	mA
				V_{DD} = 2.2V±10%		280	840	μA
			5.0 MHz crystal oscillation HALT mode (f_{XX} = 5.0 MHz)[Note 4]	V_{DD} = 5.0V±10%		1.6	4.8	mA
				V_{DD} = 3.0V±10%		0.65	1.95	mA
		I_{DD3}	32.768 kHz crystal oscillation operating mode[Note 6]	V_{DD} = 5.0V±10%		135	270	μA
				V_{DD} = 3.0V±10%		95	190	μA
				V_{DD} = 2.2V±10%		70	140	μA
		I_{DD4}	32.768 kHz crystal oscillation HALT mode[Note 6]	V_{DD} = 5.0V±10%		25	55	μA
				V_{DD} = 3.0V±10%		5	15	μA
				V_{DD} = 2.2V±10%		2.5	12.5	μA
★		I_{DD5}	XT1 = V_{DD} STOP mode Feedback resistor used	V_{DD} = 5.0V±10%		1	30	μA
				V_{DD} = 3.0V±10%		0.5	10	μA
				V_{DD} = 2.2V±10%		0.3	10	μA
★		I_{DD6}	XT1 = V_{DD} STOP mode Feedback resistor not used	V_{DD} = 5.0V±10%		0.1	30	μA
				V_{DD} = 3.0V±10%		0.05	10	μA
				V_{DD} = 2.2V±10%		0.05	10	μA

Notes 1. High-speed mode operation (when processor clock control register (PCC) is set to 00H).

2. Low-speed mode operation (when PCC is set to 04H).

3. f_{XX} = f_X/2 operation (when oscillation mode selection register (OSMS) is set to 00H).

4. f_{XX} = f_X operation (when OSMS is set to 01H).

5. A current flowing in V_{DD} pin. Not including A/D converter, D/A converter, and on-chip pull-up resistors.

6. When the main system clock is stopped.

Remark f_{XX}: Main system clock frequency (f_X or f_X/2)
f_X : Main system clock oscillation frequency

AC CHARACTERISTICS

(1) Basic Operation (T_A = −40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions			MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T_{CY}	Operating on main system clock	$f_{XX} = f_X/2$ (Note 1)	V_{DD} = 2.7 to 6.0 V	0.8		64	μs
					2.2		64	μs
			$f_{XX} = f_X$ (Note 2)	4.5 V ≤ V_{DD} ≤ 6.0 V	0.4		32	μs
				2.7 V ≤ V_{DD} < 4.5 V	0.8		32	μs
		Operating on subsystem clock			40	122	125	μs
TI00, TI01, TI1, TI2 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V			0		4	MHz
					0		275	kHz
TI00 input high-/low-level width	t_{TIH}, t_{TIL}				$8/f_{sam}$ (Note 3)			μs
TI01, TI1, TI2 input high-/low-level width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V			100			ns
					1.8			μs
Interrupt input high-/low-level width		INTP0			$8/f_{sam}$ (Note 3)			μs
		INTP1-INTP6, KR0-KR7		V_{DD} = 2.7 to 6.0 V	10			μs
					20			μs
$\overline{RESET}$ low-level width	t_{RSL}	V_{DD} = 2.7 to 6.0 V			10			μs
					20			μs

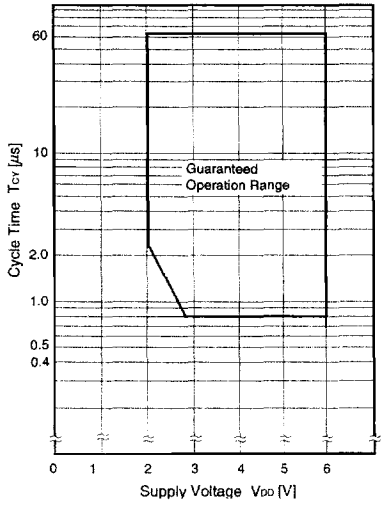
Notes 1. When oscillation mode selection register (OSMS) is set to 00H.

2. When OSMS is set to 01H.

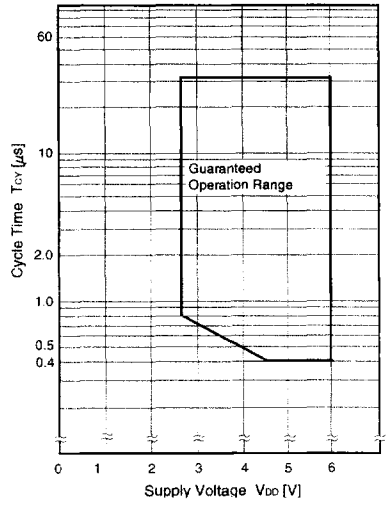
3. f_{sam} can be selected as $f_{XX}/2^N$, $f_{XX}/32$, $f_{XX}/64$, or $f_{XX}/128$ by bits 0 and 1 (SCS0 and SCS1) of the sampling clock selection register (SCS) (N = 0 to 4).

Remark f_{XX} : Main system clock frequency (f_X or $f_X/2$)
f_X : Main system clock oscillator frequency

T_{CY} vs V_{DD} (Main System Clock $f_{XX} = f_X/2$ Operation)



T_{CY} vs V_{DD} (Main System Clock $f_{XX} = f_X$ Operation)



(2) Read/Write Operations

(a) When MCS = 1, PCC2 to PCC0 = 000B (T_A = −40 to +85 °C, V_{DD} = 4.5 to 6.0 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		0.85t_{CY} − 50		ns
Address setup time	t_{ADS}		0.85t_{CY} − 50		ns
Address hold time	t_{ADH}		50		ns
Data input time from address	t_{ADD1}			(2.85 + 2n)t_{CY} − 80	ns
	t_{ADD2}			(4 + 2n)t_{CY} − 100	ns
Data input time from $\overline{RD}$↓	t_{RDD1}			(2 + 2n)t_{CY} − 100	ns
	t_{RDD2}			(2.85 + 2n)t_{CY} − 100	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(2 + 2n)t_{CY} − 60		ns
	t_{RDL2}		(2.85 + 2n)t_{CY} − 60		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{RDWT1}			0.85t_{CY} − 50	ns
	t_{RDWT2}			2t_{CY} − 60	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{WRWT}			2t_{CY} − 60	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1.15 + 2n)t_{CY}	(2 + 2n)t_{CY}	ns
Write data setup time	t_{WDS}		(2.85 + 2n)t_{CY} − 100		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL1}		(2.85 + 2n)t_{CY} − 60		ns
$\overline{RD}$↓ delay time from ASTB↓	t_{ASTRD}		25		ns
$\overline{WR}$↓ delay time from ASTB↓	t_{ASTWR}		0.85t_{CY} + 20		ns
ASTB↑ delay time from $\overline{RD}$↑ in external fetch	t_{RDAST}		0.85t_{CY} − 10	1.15t_{CY} + 20	ns
Address hold time from $\overline{RD}$↑ in external fetch	t_{RDADH}		0.85t_{CY} − 50	1.15t_{CY} + 50	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}		40		ns
Write data output time from $\overline{WR}$↓	t_{WRWD}		0	50	ns
Address hold time from $\overline{WR}$↑	t_{WRADH}		0.85t_{CY}	1.15t_{CY} + 40	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{WTRD}		1.15t_{CY} + 40	3.15t_{CY} + 40	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{WTWR}		1.15t_{CY} + 30	3.15t_{CY} + 30	ns

Remarks 1. MCS: Bit 0 of the oscillation mode selection register (OSMS)

2. PCC2 to PCC0: Bit 2 to bit 0 of the processor clock control register (PCC)

3. $t_{CY} = T_{CY}/4$

4. n indicates the number of waits.

(b) Except when MCS = 1, PCC2 to PCC0 = 000B (T_A = −40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}	V_{DD} = 2.7 to 6.0V	t_{CY} − 80		ns
			t_{CY} − 150		ns
Address setup time	t_{ADS}	V_{DD} = 2.7 to 6.0V	t_{CY} − 80		ns
			t_{CY} − 150		ns
Address hold time	t_{ADH}	V_{DD} = 2.7 to 6.0V	0.4t_{CY} − 10		ns
			0.37t_{CY} − 40		ns
Data input time from address	t_{ADD1}	V_{DD} = 2.7 to 6.0V		(3 + 2n)t_{CY} − 160	ns
				(3 + 2n)t_{CY} − 320	ns
	t_{ADD2}	V_{DD} = 2.7 to 6.0V		(4 + 2n)t_{CY} − 200	ns
				(4 + 2n)t_{CY} − 300	ns
Data input time from $\overline{RD}$↓	t_{RDD1}	V_{DD} = 2.7 to 6.0V		(1.4 + 2n)t_{CY} − 70	ns
				(1.37 + 2n)t_{CY} − 120	ns
	t_{RDD2}	V_{DD} = 2.7 to 6.0V		(2.4 + 2n)t_{CY} − 70	ns
				(2.37 + 2n)t_{CY} − 120	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}	V_{DD} = 2.7 to 6.0V	(1.4 + 2n)t_{CY} − 20		ns
			(1.37 + 2n)t_{CY} − 20		ns
	t_{RDL2}	V_{DD} = 2.7 to 6.0V	(2.4 + 2n)t_{CY} − 20		ns
			(2.37 + 2n)t_{CY} − 20		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{RDWT1}	V_{DD} = 2.7 to 6.0V		t_{CY} − 100	ns
				t_{CY} − 200	ns
	t_{RDWT2}	V_{DD} = 2.7 to 6.0V		2t_{CY} − 100	ns
				2t_{CY} − 200	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{WRWT}	V_{DD} = 2.7 to 6.0V		2t_{CY} − 100	ns
				2t_{CY} − 200	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(1 + 2n)t_{CY}	(2 + 2n)t_{CY}	ns
Write data setup time	t_{WDS}	V_{DD} = 2.7 to 6.0V	(2.4 + 2n)t_{CY} − 60		ns
			(2.37 + 2n)t_{CY} − 100		ns
Write data hold time	t_{WDH}		20		ns
$\overline{WR}$ low-level width	t_{WRL1}	V_{DD} = 2.7 to 6.0V	(2.4 + 2n)t_{CY} − 20		ns
			(2.37 + 2n)t_{CY} − 20		ns

Remarks 1. MCS: Bit 0 of the oscillation mode selection register (OSMS)

2. PCC2 to PCC0: Bit 2 to bit 0 of the processor clock control register (PCC)

3. t_{CY} = T_{CY}/4

4. n indicates the number of waits.

(b) Except when MCS = 1, PCC2 to PCC0 = 000B (T_A = −40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Test Conditions	MIN.	MAX.	Unit
$\overline{RD}$↓ delay time from ASTB↓	t_{ASTRD}	V_{DD} = 2.7 to 6.0V	0.4t_{CY} − 30		ns
			0.37t_{CY} − 50		ns
$\overline{WR}$↓ delay time from ASTB↓	t_{ASTWR}	V_{DD} = 2.7 to 6.0V	1.4t_{CY} − 30		ns
			1.37t_{CY} − 50		ns
ASTB↑delay time from $\overline{RD}$↑ in external fetch	t_{RDAST}		t_{CY} − 10	t_{CY} + 20	ns
Address hold time from $\overline{RD}$↑ in external fetch	t_{RDADH}		t_{CY} − 50	t_{CY} + 50	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}	V_{DD} = 2.7 to 6.0V	0.4t_{CY} − 20		ns
			0.37t_{CY} − 40		ns
Write data output time from $\overline{WR}$↓	t_{WRWD}	V_{DD} = 2.7 to 6.0V	0	60	ns
			0	120	ns
Address hold time from $\overline{WR}$↑	t_{WRADH}	V_{DD} = 2.7 to 6.0V	t_{CY}	t_{CY} + 60	ns
			t_{CY}	t_{CY} + 120	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{WTRD}	V_{DD} = 2.7 to 6.0V	0.6t_{CY} + 180	2.6t_{CY} + 180	ns
			0.63t_{CY} + 350	2.63t_{CY} + 350	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{WTWR}	V_{DD} = 2.7 to 6.0V	0.6t_{CY} + 120	2.6t_{CY} + 120	ns
			0.63t_{CY} + 240	2.63t_{CY} + 240	ns

Remarks 1. MCS: Bit 0 of the oscillation mode selection register (OSMS)

2. PCC2 to PCC0: Bit 2 to bit 0 of the processor clock control register (PCC)

3. t_{CY} = T_{CY}/4

4. n indicates the number of waits.

(3) Serial Interface (T_A = −40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

(a) Serial interface channel 0

(i) 3-wire serial I/O mode ($\overline{SCK0}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY1}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH1},	V_{DD} = 4.5 to 6.0 V	t_{KCY1}/2−50			ns
	t_{KL1}		t_{KCY1}/2−100			ns
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK1}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI1}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO1}	C = 100 pF [Note]			300	ns

Note C is the SO0 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{SCK0}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY2}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH2},	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
	t_{KL2}	2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			
SI0 setup time (to $\overline{SCK0}$↑)	t_{SIK2}		100			ns
SI0 hold time (from $\overline{SCK0}$↑)	t_{KSI2}		400			ns
SO0 output delay time from $\overline{SCK0}$↓	t_{KSO2}	*C = 100 pF* [Note]			*300*	ns
$\overline{SCK0}$ rise, fall time	t_{R2}, t_{F2}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO0 output line load capacitance.

(iii) SBI mode ($\overline{SCK0}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V	800			ns
			3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH3}, t_{KL3}	V_{DD} = 4.5 to 6.0 V	$t_{KCY3}/2-50$			ns
			$t_{KCY3}/2-100$			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK3}	V_{DD} = 4.5 to 6.0 V	100			ns
			300			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI3}		$t_{KCY3}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO3}	R = 1 kΩ, C = 100 pF (Note), V_{DD} = 4.5 to 6.0 V	0		250	ns
			0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}		t_{KCY3}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}		t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}		t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}		t_{KCY3}			ns

Note R and C are the SB0 & SB1 output line load resistance and load capacitance.

(iv) SBI mode ($\overline{SCK0}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V	800			ns
			3200			ns
$\overline{SCK0}$ high-/low-level width	t_{KH4}, t_{KL4}	V_{DD} = 4.5 to 6.0 V	400			ns
			1600			ns
SB0, SB1 setup time (to $\overline{SCK0}$↑)	t_{SIK4}	V_{DD} = 4.5 to 6.0 V	100			ns
			300			ns
SB0, SB1 hold time (from $\overline{SCK0}$↑)	t_{KSI4}		$t_{KCY4}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}$↓	t_{KSO4}	R = 1 kΩ, C = 100 pF (Note), V_{DD} = 4.5 to 6.0 V	0		300	ns
			0		1000	ns
SB0, SB1↓ from $\overline{SCK0}$↑	t_{KSB}		t_{KCY4}			ns
$\overline{SCK0}$↓ from SB0, SB1↓	t_{SBK}		t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}		t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}		t_{KCY4}			ns
$\overline{SCK0}$ rise, fall time	t_{R4}, t_{F4}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note R and C are the SCK0, SB0 & SB1 output line load resistance and load capacitance.

(v) 2-wire serial I/O mode ($\overline{SCK0}$ ... internal clock output)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY5}	R = 1 kΩ, C = 100 pF Note	V_{DD} = 2.7 to 6.0 V	1600			ns
				3200			ns
$\overline{SCK0}$ high-level width	t_{KH5}		V_{DD} = 2.7 to 6.0 V	$t_{KCY5}/2-160$			ns
				$t_{KCY5}/2-190$			ns
$\overline{SCK0}$ low-level width	t_{KL5}		V_{DD} = 4.5 to 6.0 V	$t_{KCY5}/2-50$			ns
				$t_{KCY5}/2-100$			ns
SB0, SB1 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK5}		4.5 V≤V_{DD}≤6.0 V	300			ns
			2.7 V≤V_{DD}<4.5 V	350			ns
				400			ns
SB0, SB1 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI5}			600			ns
SB0, SB1 output delay time from $\overline{SCK0}\downarrow$	t_{KSO5}			0		300	ns

Note R and C are the $\overline{SCK0}$, SB0 & SB1 output line load resistance and load capacitance.

(vi) 2-wire serial I/O mode ($\overline{SCK0}$ ... external clock input)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCK0}$ cycle time	t_{KCY6}	V_{DD} = 2.7 to 6.0 V		1600			ns
				3200			ns
$\overline{SCK0}$ high-level width	t_{KH6}	V_{DD} = 2.7 to 6.0 V		650			ns
				1300			ns
$\overline{SCK0}$ low-level width	t_{KL6}	V_{DD} = 2.7 to 6.0 V		800			ns
				1600			ns
SB0, SB1 setup time (to $\overline{SCK0}\uparrow$)	t_{SIK6}			100			ns
SB0, SB1 hold time (from $\overline{SCK0}\uparrow$)	t_{KSI6}			$t_{KCY6}/2$			ns
SB0, SB1 output delay time from $\overline{SCK0}\downarrow$	t_{KSO6}	R = 1 kΩ, C = 100 pF Note	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		500	ns
$\overline{SCK0}$ rise, fall time	t_{R6}, t_{F6}	When using external device expansion function				160	ns
		When not using external device expansion function				1000	ns

Note R and C are the SB0 & SB1 output line load resistance and load capacitance.

(b) Serial interface channel 1

(i) 3-wire serial I/O mode ($\overline{SCK1}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY7}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK1}$ high-/low-level width	t_{KH7},	V_{DD} = 4.5 to 6.0 V	$t_{KCY7}/2-50$			ns
	t_{KL7}		$t_{KCY7}/2-100$			ns
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK7}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI7}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO7}	C = 100 pF Note			300	ns

Note C is the SO1 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{SCK1}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY8}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK1}$ high-/low-level width	t_{KH8},	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
	t_{KL8}	2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			
SI1 setup time (to $\overline{SCK1}$↑)	t_{SIK8}		100			ns
SI1 hold time (from $\overline{SCK1}$↑)	t_{KSI8}		400			ns
SO1 output delay time from $\overline{SCK1}$↓	t_{KSO8}	C = 100 pF Note			300	ns
$\overline{SCK1}$ rise, fall time	t_{R8}, t_{F8}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO1 output line load capacitance.

(iii) Automatic transmission/reception function 3-wire serial I/O mode (SCK1 ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
SCK1 cycle time	t_{KCY9}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
SCK1 high-/low-level width	t_{KH9}, t_{KL9}	V_{DD} ≥ 4.5 to 6.0 V	t_{KCY9}/2–50			ns
			t_{KCY9}/2–100			ns
SI1 setup time (to SCK1↑)	t_{SIK9}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI1 hold time (from SCK1↑)	t_{KSI9}		400			ns
SO output delay time from SCK1↓	t_{KSO9}	C = 100 pF [Note]			300	ns
STB↑ from SCK1↑	t_{SBD}		t_{KCY9}/2–100		t_{KCY9}/2+100	ns
Strobe signal high-level width	t_{SBW}	V_{DD} ≥ 2.7 to 6.0 V	t_{KCY9}–30		t_{KCY9}+30	ns
			t_{KCY9}–60		t_{KCY9}+60	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}		100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			200			ns
SCK1↓ from busy inactivation	t_{SPS}				$2t_{KCY9}$	ns

Note C is the SO1 output line load capacitance.

(iv) Automatic transmission/reception function 3-wire serial I/O mode (SCK1 ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
SCK1 cycle time	t_{KCY10}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
SCK1 high-/low-level width	t_{KH10}, t_{KL10}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI1 setup time (to SCK1↑)	t_{SIK10}		100			ns
SI1 hold time (from SCK1↑)	t_{KSI10}		400			ns
SO1 output delay time from SCK1↓	t_{KSO10}	C = 100 pF [Note]			300	ns
SCK1 rise, fall time	t_{R10}, t_{F10}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO1 output line load capacitance.

(c) Serial interface channel 2

(i) 3-wire serial I/O mode ($\overline{SCK2}$ ... internal clock output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY11}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK2}$ high-/low-level width	t_{KH11}, t_{KL11}	V_{DD} = 4.5 to 6.0 V	t_{KCY11}/2–50			ns
			t_{KCY11}/2–100			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK11}	4.5 V ≤ V_{DD} ≤ 6.0 V	100			ns
		2.7 V ≤ V_{DD} < 4.5 V	150			ns
			300			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI11}		400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO11}	C = 100 pF Note			300	ns

Note C is the SO2 output line load capacitance.

(ii) 3-wire serial I/O mode ($\overline{SCK2}$ ... external clock input)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK2}$ cycle time	t_{KCY12}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
$\overline{SCK2}$ high-/low-level width	t_{KH12}, t_{KL12}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
SI2 setup time (to $\overline{SCK2}$↑)	t_{SIK12}		100			ns
SI2 hold time (from $\overline{SCK2}$↑)	t_{KSI12}		400			ns
SO2 output delay time from $\overline{SCK2}$↓	t_{KSO12}	C = 100 pF Note			300	ns
$\overline{SCK2}$ rise, fall time	t_{R12}, t_{F12}	When using external device expansion function			160	ns
		When not using external device expansion function			1000	ns

Note C is the SO2 output line load capacitance.

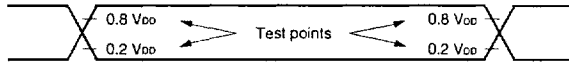
(iii) UART mode (Dedicated baud rate generator output)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		4.5 V ≤ V_{DD} ≤ 6.0 V			78125	bps
		2.7 V ≤ V_{DD} < 4.5 V			39063	bps
					19531	bps

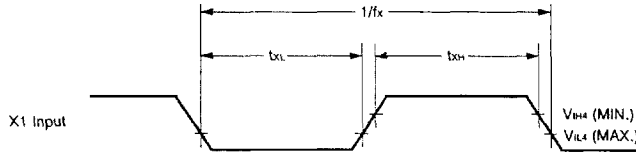
(iv) UART mode (External clock input)

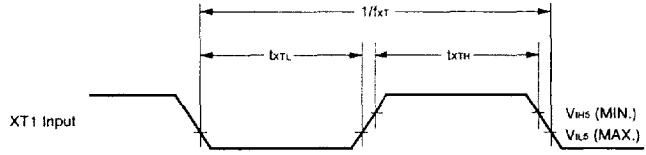
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
ASCK cycle time	t_{KCY13}	4.5 V ≤ V_{DD} ≤ 6.0 V	800			ns
		2.7 V ≤ V_{DD} < 4.5 V	1600			ns
			3200			ns
ASCK high-/low-level width	t_{KH13}, t_{KL13}	4.5 V ≤ V_{DD} ≤ 6.0 V	400			ns
		2.7 V ≤ V_{DD} < 4.5 V	800			ns
			1600			ns
Transfer rate		4.5 V ≤ V_{DD} ≤ 6.0 V			39063	bps
		2.7 V ≤ V_{DD} < 4.5 V			19531	bps
					9766	bps
$\overline{SCK}$ rise, fall time	t_{R13}, t_{F13}	V_{DD} = 4.5 to 6.0 V, when not using external device expansion function			1000	ns
					160	ns

AC Timing Test Point (Excluding X1, XT1 Input)

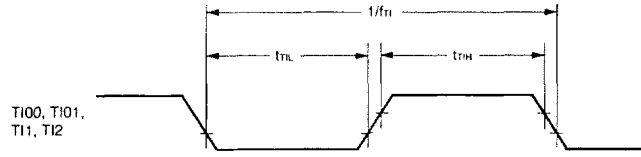


Clock Timing



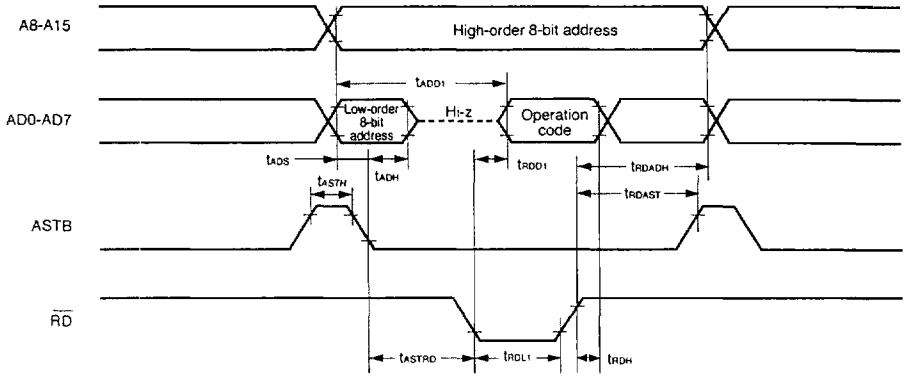


TI Timing

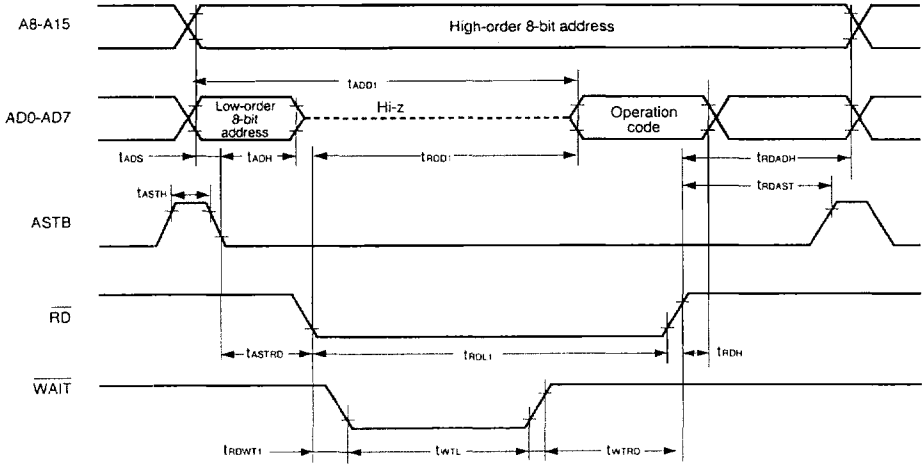


Read/Write Operations

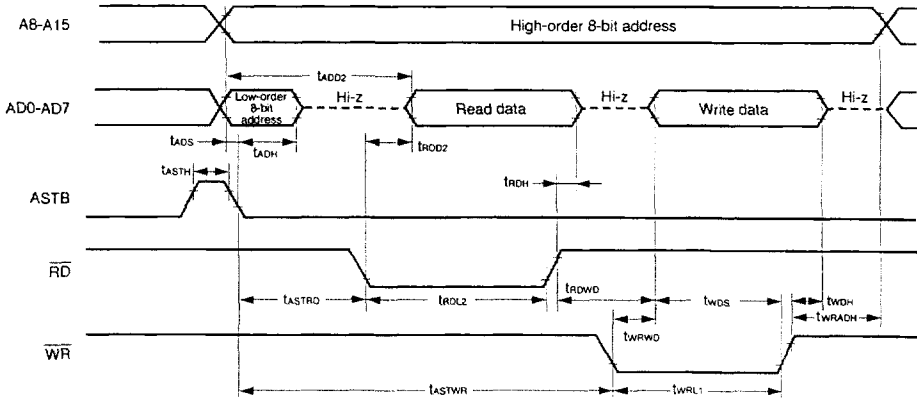
External fetch (no wait):



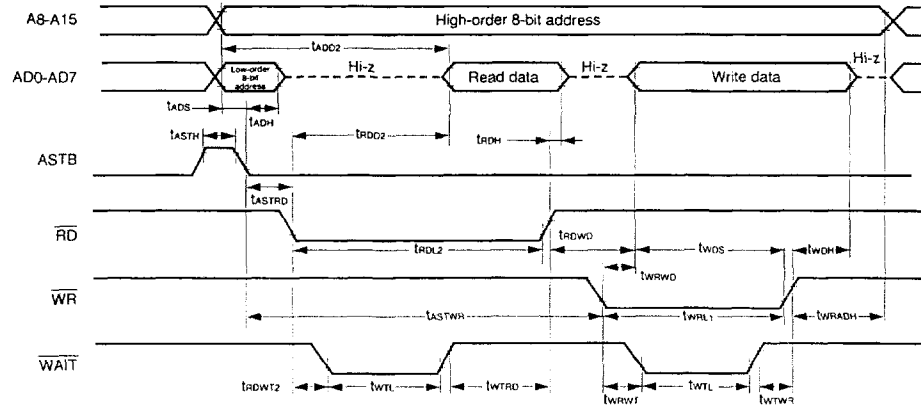
External fetch (wait insertion):



External data access (no wait):

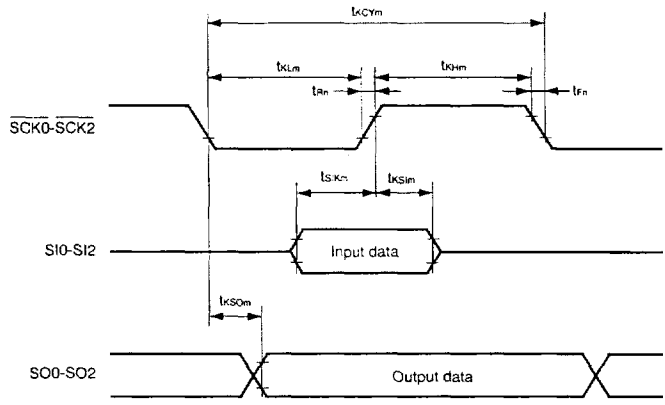


External data access (wait insertion):



Serial Transfer Timing

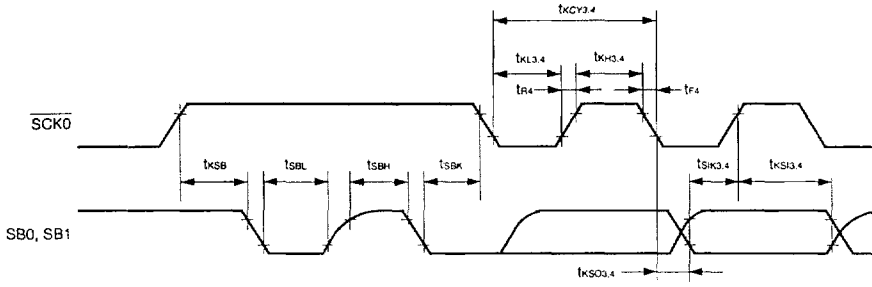
3-wire serial I/O mode:



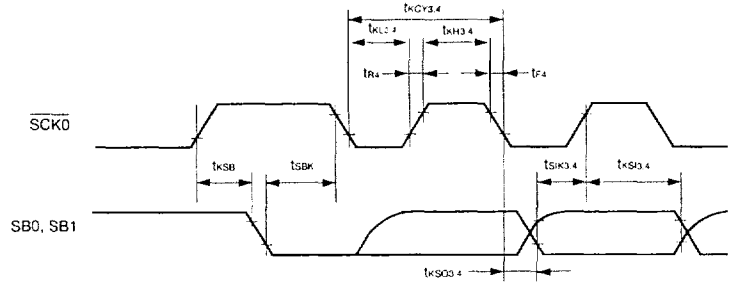
m = 1, 2, 7, 8, 11, 12

n = 2, 8, 12

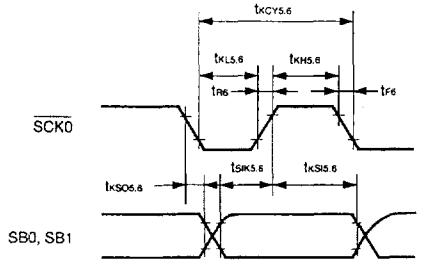
SBI mode (bus release signal transfer):



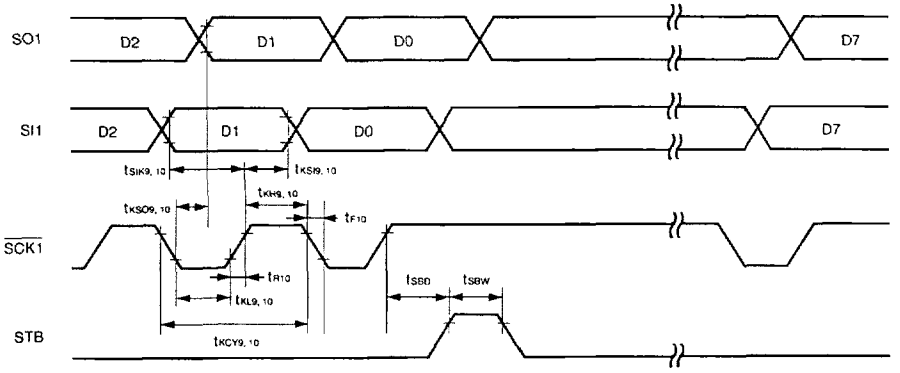
SBI mode (command signal transfer):



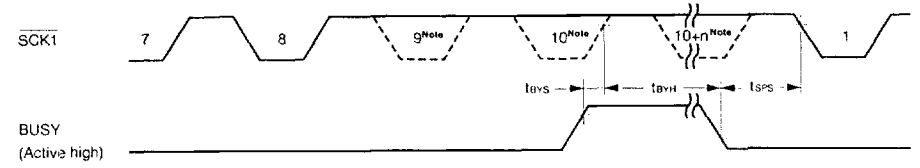
2-wire serial I/O mode:



Automatic transmission/reception function 3-wire serial I/O mode:

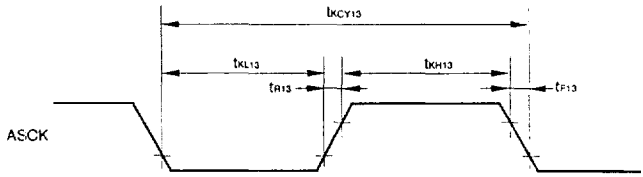


Automatic transmission/reception function 3-wire serial I/O mode (busy processing):



Note The signal is not actually low here, but is represented in this way to show the timing.

UART mode (external clock input):



A/D CONVERTER CHARACTERISTICS (T_A = –40 to +85 °C, AV_{DD} = V_{DD} = 2.7 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Total error[Note]		2.7 V ≤ AV_{REF0} ≤ AV_{DD}			1.0	%
Conversion time	t_{CONV}		19.1		200	μs
Sampling time	t_{SAMP}		12/f_{XX}			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF0}	V
Reference voltage	AV_{REF0}		2.7		AV_{DD}	V
AV_{REF0}-AV_{SS} resistance	R_{AIREF0}		4			kΩ

Note Excluding quantization error (±1/2 LSB). Shown as a percentage of the full scale value.

Remark f_{XX} : Main system clock frequency (f_X or f_X/2)
f_X : Main system clock oscillation frequency

D/A CONVERTER CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = 2.0 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Resolution						8	bit
Total error		R = 2 MΩ [Note 1]				1.2	%
		R = 4 MΩ [Note 1]				0.8	%
		R = 10 MΩ [Note 1]				0.6	%
Settling time		C = 30 pF [Note 1]	4.5 V ≤ AV_{REF1} ≤ 6.0 V			10	μs
			2.7 V ≤ AV_{REF1} < 4.5 V			15	μs
			2.0 V ≤ AV_{REF1} < 2.7 V			20	μs
Output resistor	R_O	DACS0, DACS1 = 55H [Note 2]			10		kΩ
Analog reference voltage	AV_{REF1}			2.0		V_{DD}	V
AV_{REF1} current	AI_{REF1}	**Note 2**				1.5	mA

Notes 1. R and C are the D/A converter output pin load resistance and load capacitance.
2. Value for one D/A converter channel.

★ **Remark** DACS0, DACS1: D/A conversion value setting register 0, 1

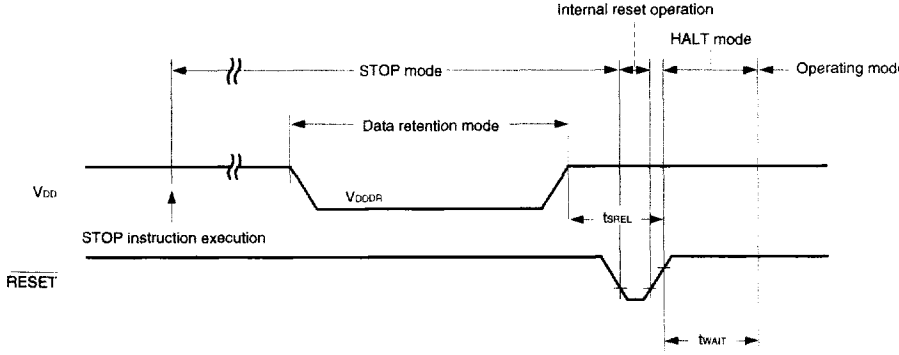
DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (T_A = −40 to +85 °C)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.8		6.0	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V Subsystem clock stopped, feedback resister disconnected		0.1	10	μA
Release signal setup time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_x$		ms
		Release by interrupt		**Note**		ms

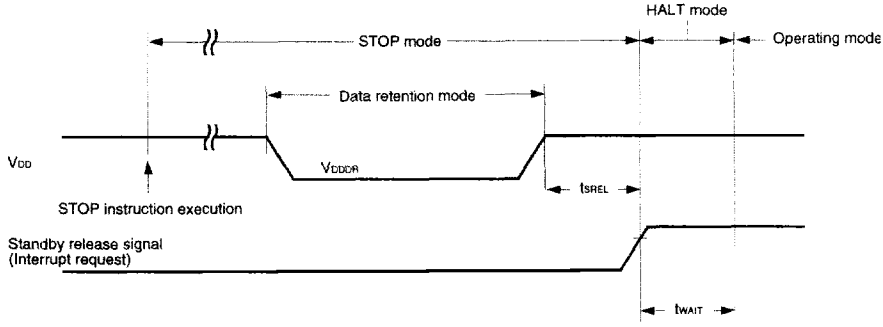
Note $2^{12}/fxx$, or $2^{14}/fxx$ through $2^{17}fxx$ can be selected by bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time selection register (OSTS).

Remark fxx: Main system clock frequency (fx or fx/2)
fx : Main system clock oscillator frequency

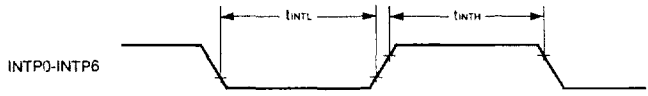
Data Retention Timing (STOP mode release by $\overline{RESET}$)



Data Retention Timing (STOP mode release by standby release signal: interrupt signal)



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing

PROM PROGRAMMING CHARACTERISTICS

DC CHARACTERISTICS

(1) PROM Write Mode (T_A = 25 ±5 °C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH}	V_{IH}		0.7 V_{DD}		V_{DD}	V
Input voltage low	V_{IL}	V_{IL}		0		0.3 V_{DD}	V
Output voltage high	V_{OH}	V_{OH}	I_{OH} = −1 mA	V_{DD} −1.0			V
Output voltage low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 ≤ V_{IN} ≤ V_{DD}	−10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		12.2	12.5	12.8	V
V_{DD} supply voltage	V_{DD}	V_{CC}		6.25	6.5	6.75	V
V_{PP} supply current	I_{PP}	I_{PP}	$\overline{PGM}$ = V_{IL}			50	mA
V_{DD} supply current	I_{DD}	I_{CC}				50	mA

(2) PROM Read Mode (T_A = 25 ±5 °C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Input voltage high	V_{IH}	V_{IH}		0.7 V_{DD}		V_{DD}	V
Input voltage low	V_{IL}	V_{IL}		0		0.3 V_{DD}	V
Output voltage high	V_{OH1}	V_{OH1}	I_{OH} = −1 mA	V_{DD} −1.0			V
	V_{OH2}	V_{OH2}	I_{OH} = −100 μA	V_{DD} −0.5			V
Output voltage low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 ≤ V_{IN} ≤ V_{DD}	−10		+10	μA
Output leakage current	I_{LO}	I_{LO}	0 ≤ V_{OUT} ≤ V_{DD}, $\overline{OE}$ = V_{IH}	−10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		V_{DD} −0.6	V_{DD}	V_{DD} +0.6	V
V_{DD} supply voltage	V_{DD}	V_{CC}		4.5	5.0	5.5	V
V_{PP} supply current	I_{PP}	I_{PP}	V_{PP} = V_{DD}			100	μA
V_{DD} supply current	I_{DD}	I_{CC1}	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH}			50	mA

Note Corresponding μPD27C1001A symbol.

AC CHARACTERISTICS

(1) PROM Write Mode

(a) Page program mode (T_A = 25 ±5 °C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{OE}\downarrow$)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ setup time	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{OE}\downarrow$)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{OE}\downarrow$)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}\uparrow$)	t_{AH}	t_{AH}		2			μs
	t_{AHL}	t_{AHL}		2			μs
	t_{AHV}	t_{AHV}		0			μs
Input data hold time (from $\overline{OE}\uparrow$)	t_{DH}	t_{DH}		2			μs
Data output float delay time from $\overline{OE}\uparrow$	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{OE}\downarrow$)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{OE}\downarrow$)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
Valid data delay time from $\overline{OE}\downarrow$	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ pulse width during data latching	t_{LW}	t_{LW}		1			μs
$\overline{PGM}$ setup time	t_{PGMS}	t_{PGMS}		2			μs
$\overline{CE}$ hold time	t_{CEH}	t_{CEH}		2			μs
$\overline{OE}$ hold time	t_{OEH}	t_{OEH}		2			μs

(b) Byte program mode (T_A = 25 ±5 °C, V_{DD} = 6.5 ±0.25 V, V_{PP} = 12.5 ±0.3 V)

Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Address setup time (to $\overline{PGM}\downarrow$)	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ setup time	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (to $\overline{PGM}\downarrow$)	t_{CES}	t_{CES}		2			μs
Input data setup time (to $\overline{PGM}\downarrow$)	t_{DS}	t_{DS}		2			μs
Address hold time (from $\overline{OE}\uparrow$)	t_{AH}	t_{AH}		2			μs
Input data hold time (from $\overline{PGM}\uparrow$)	t_{DH}	t_{DH}		2			μs
Data output float delay time from $\overline{OE}\uparrow$	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (to $\overline{PGM}\downarrow$)	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (to $\overline{PGM}\downarrow$)	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
Valid data delay time from $\overline{OE}\downarrow$	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ hold time	t_{OEH}	—		2			μs

Note Corresponding μPD27C1001A symbol

(2) PROM Read Mode (T_A = 25 ±5 °C, V_{DD} = 5.0 ±0.5 V, V_{PP} = V_{DD} ±0.6 V)

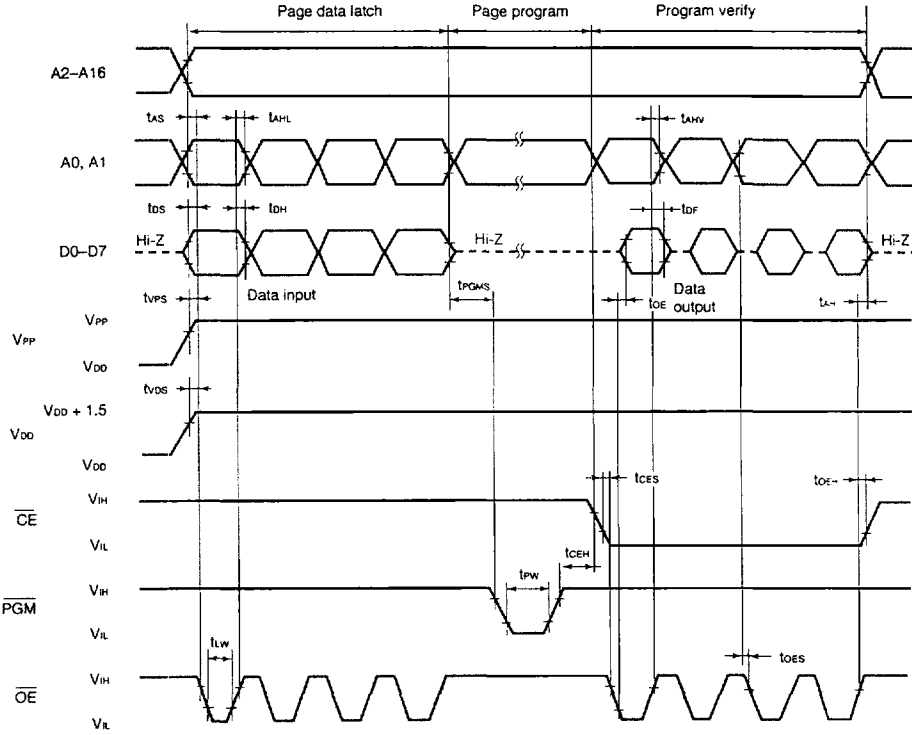
Parameter	Symbol	Symbol[Note]	Test Conditions	MIN.	TYP.	MAX.	Unit
Data output delay time from address	t_{ACC}	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			800	ns
Data output delay time from $\overline{CE}$↓	t_{CE}	t_{CE}	$\overline{OE}$ = V_{IL}			800	ns
Data output delay time from $\overline{OE}$↓	t_{OE}	t_{OE}	$\overline{CE}$ = V_{IL}			200	ns
Data output float delay time from $\overline{OE}$↑	t_{DF}	t_{DF}	$\overline{CE}$ = V_{IL}	0		60	ns
Data hold time from address	t_{OH}	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0			ns

Note Corresponding μPD27C1001A symbol

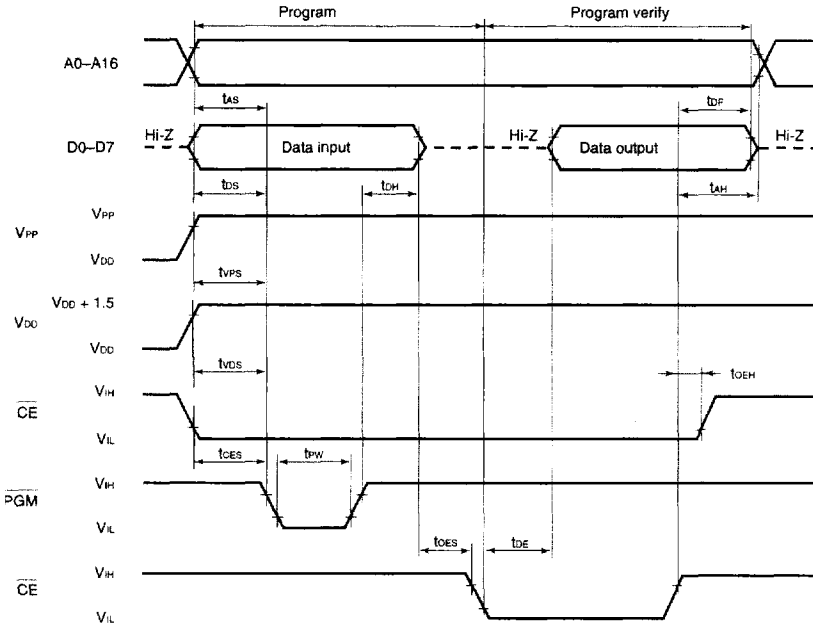
(3) PROM Programming Mode Setting (T_A = 25 °C, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
PROM programming mode setup time	t_{SMA}		10			μs

PROM Write Mode Timing (page program mode)



PROM Write Mode Timing (byte program mode)

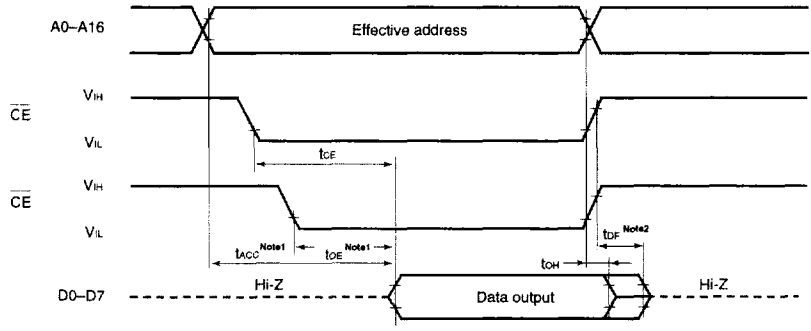


Cautions 1. V_{DD} should be applied before V_{PP}, and cut after V_{PP}.

2. V_{PP} should not exceed +13.5 V including overshoot.

3. Disconnection during application of ±12.5V to V_{PP} may have an adverse effect on reliability.

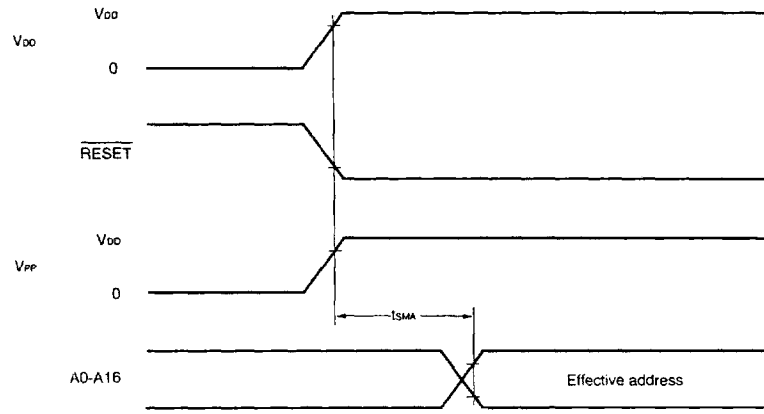
PROM Read Mode Timing



Notes 1. If you want to read within the t_{ACC} range, make the $\overline{OE}$ input delay time from the fall of $\overline{CE}$ a maximum of $t_{ACC} - t_{OE}$.

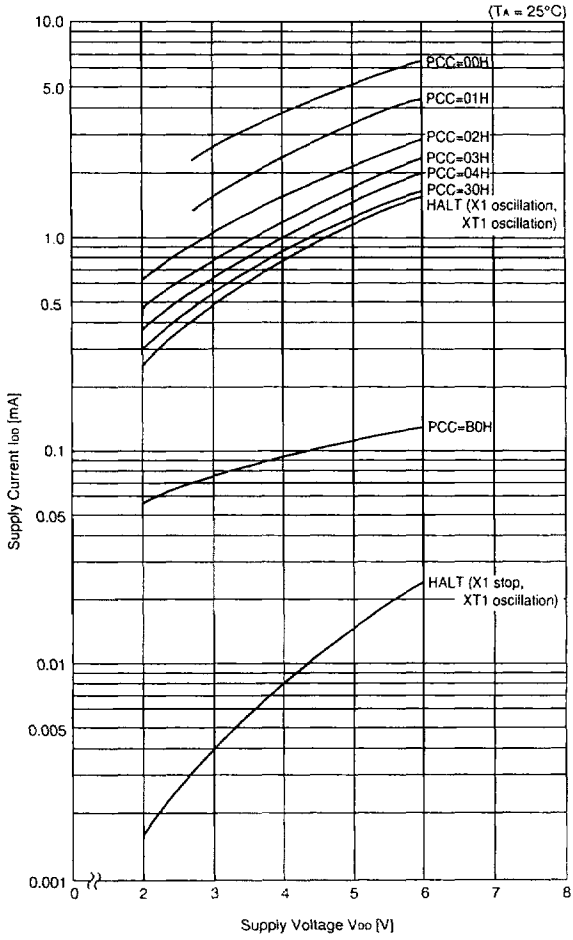
2. t_{DF} is the time from when either $\overline{OE}$ or $\overline{CE}$ first reaches V_{IH}.

PROM Programming Mode Setting Timing

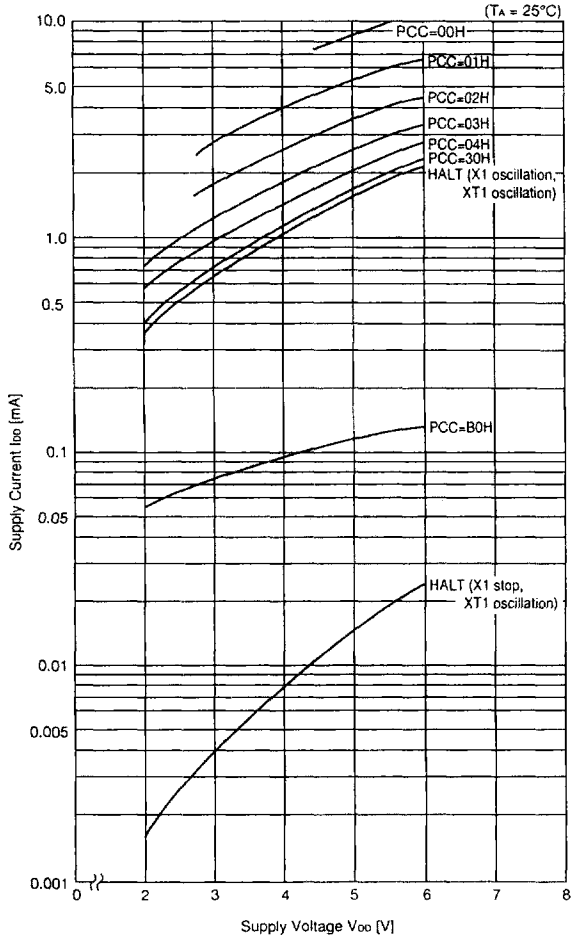


9. CHARACTERISTIC CURVES (REFERENCE VALUES)

I_{DD} vs V_{DD} (f_X = 5.0 MHz, f_{XX} = 2.5 MHz)



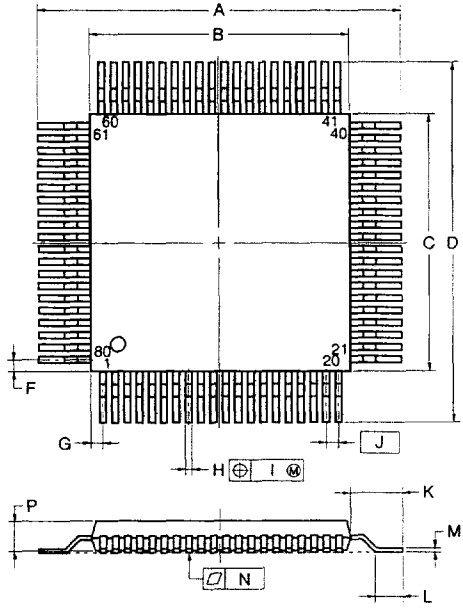
I_{DD} vs V_{DD} ($f_X = f_{XX} = 5.0$ MHz)



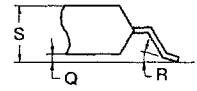
10. PACKAGE DRAWINGS

★ • μPD78P054GC-3B9

80 PIN PLASTIC QFP (14×14)



detail of lead end



NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

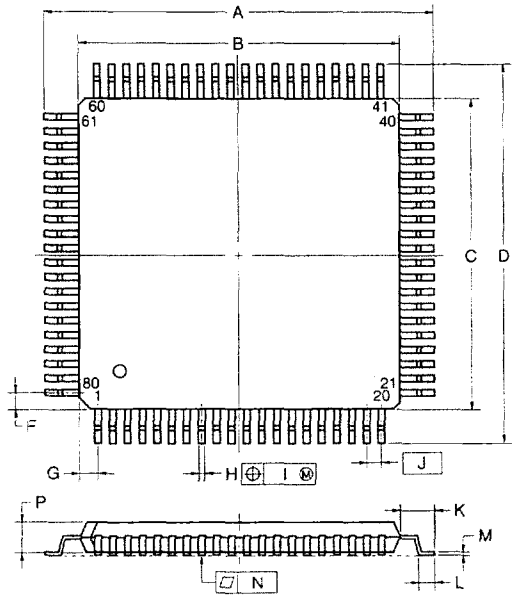
ITEM	MILLIMETERS	INCHES
A	17.2±0.4	0.677±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.2±0.4	0.677±0.016
F	0.825	0.032
G	0.825	0.032
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.6±0.2	0.063±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
R	5°±5°	5°±5°
S	3.0 MAX.	0.119 MAX.

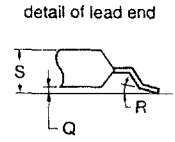
S80GC-65-3B9-4

★ **Remark** Dimensions and materials of the ES models are the same as those of the mass-production models.

★ • μPD78P054GC-8BT

80 PIN PLASTIC QFP (14×14)





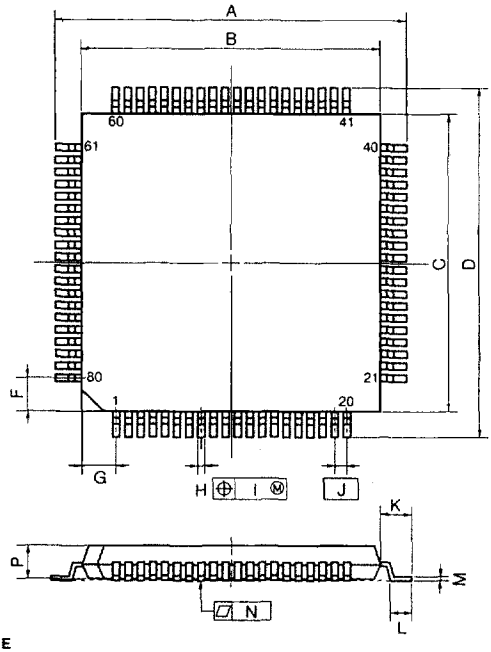
NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

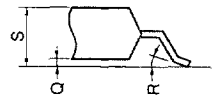
ITEM	MILLIMETERS	INCHES
A	17.20±0.20	0.677±0.008
B	14.00±0.20	$0.551^{+0.009}_{-0.008}$
C	14.00±0.20	$0.551^{+0.009}_{-0.008}$
D	17.20±0.20	0.677±0.008
F	0.825	0.032
G	0.825	0.032
H	0.32±0.06	$0.013^{+0.002}_{-0.003}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.60±0.20	0.063±0.008
L	0.80±0.20	$0.031^{+0.009}_{-0.008}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.40±0.10	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$
S	1.70 MAX.	0.067 MAX.

P80GC-65-8BT

80 PIN PLASTIC TQFP (FINE PITCH) (□12)



detail of lead end



NOTE

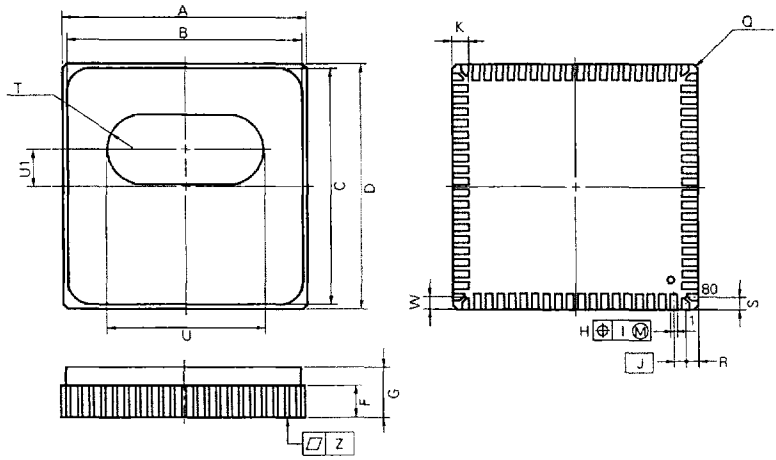
Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	$0.551^{+0.009}_{-0.008}$
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.0±0.2	$0.551^{+0.009}_{-0.008}$
F	1.25	0.049
G	1.25	0.049
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.05	0.041
Q	0.05±0.05	0.002±0.002
R	5°±5°	5°±5°
S	1.27 MAX.	0.050 MAX.

P80GK-50-BE9-4

★ **Remark** Dimensions and materials of the ES models are the same as those of the mass-production models.

80 PIN CERAMIC WQFN



X80KW-65A-1

NOTE

Each lead centerline is located within 0.06 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.0±0.2	0.551±0.008
B	13.6	0.535
C	13.6	0.535
D	14.0±0.2	0.551±0.008
F	1.84	0.072
G	3.6 MAX.	0.142 MAX.
H	0.45±0.10	$0.018^{+0.004}_{-0.005}$
I	0.06	0.003
J	0.65 (T.P.)	0.024 (T.P.)
K	1.0±0.15	$0.039^{+0.007}_{-0.006}$
Q	C 0.3	C 0.012
R	0.825	0.032
S	0.825	0.032
T	R 2.0	R 0.079
U	9.0	0.354
U1	2.1	0.083
W	0.75±0.15	$0.030^{+0.005}_{-0.007}$
Z	0.10	0.004

11. RECOMMENDED SOLDERING CONDITIONS

These products should be soldered and mounted under the conditions recommended below.

For details of recommended soldering conditions, refer to the information document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended, please contact your NEC sales representative.

★ **Table 11-1. Surface Mount Type Soldering Conditions**

(1) μPD78P054GC-3B9: 80-Pin Plastic QFP (14 × 14 mm, resin thickness 2.7 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Duration: 30 sec. max. (210°C or above) Number of times: Max. 3	IR35-00-3
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (200°C or above) Number of times: Max. 3	VP15-00-3
Wave soldering	Solder bath temperature: 260°C or less, Duration: 10 sec. max. Number of times: one Preparatory heating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C or less, Duration: 3 sec. max. (per side of device)	—

(2) μPD78P054GK-BE9: 80-Pin Plastic TQFP (Fine Pitch) (12 × 12 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Duration: 30 sec. max. (210°C or above) Number of times: Max. 3 Time limit: 7 days[Note] (thereafter 10 hours 125°C prebaking required) <Precaution> Products cannot be baked while packed in anything other than in a heat resistant tray (i.e. they cannot be baked in a magazine, taping, or heat-labile tray).	IR35-107-3
VPS	Package peak temperature: 215°C, Duration: 40 sec. max. (200°C or above) Number of times: Max. 3 Time limit: 7 days[Note] (thereafter 10 hours 125°C prebaking required) <Precaution> Products cannot be baked while packed in anything other than in a heat resistance tray (i.e. they cannot be baked in a magazine, taping, or non-heat-resistance tray).	VP15-107-3
Partial heating	Pin temperature: 300°C or less, Duration: 3 sec. max. (per side of device)	—

Note For the storage period after dry-pack decapsulation, storage conditions are max. 25°C, 65% RH.

Cautions 1. Do not use two or more soldering methods in combination (except partial heating).

2. Because the μPD78P054GC-8BT is under development, soldering conditions are not determined.