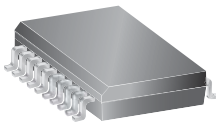


## DABIC-5 8-Channel Source Driver with Overcurrent Protection

### Features and Benefits

- 4.75 to 35 V driver supply voltage
- Output enable-disable (OE/R)
- 350 mA output source current
- Overcurrent protected
- Internal ground clamp diodes
- Output Breakdown Voltage 35 V minimum
- TTL, DTL, PMOS, or CMOS compatible inputs
- Internal Thermal Shutdown (TSD)

### Packages:



20-pin SOICW  
(LW package)



20-pin DIP  
(A package)

### Description

Providing overcurrent protection for each of its eight sourcing outputs, the UDN2987A-6 and UDN2987LW-6 drivers are used as an interface between standard low-level logic and relays, motors, solenoids, LEDs, and incandescent lamps. These devices include thermal shut down and output transient protection/clamp diodes for use with sustaining voltages to 35 V.

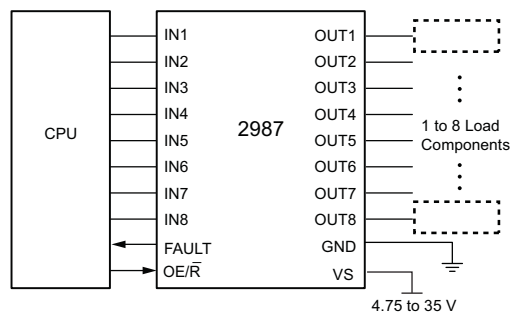
In these drivers, each channel includes a latch to turn off that channel if the maximum channel current is exceeded. All channels are disabled if the thermal shutdown is activated. A common FAULT output is used to indicate either chip thermal shutdown or any overcurrent condition. All outputs are enabled by pulling the common OE/R input high. When OE/R is low, all outputs are inhibited and the eight latches are reset. The OE/R function can be especially important during power-up, in preventing floating inputs from turning on the outputs.

Under normal operating conditions, each of eight outputs will source in excess of 100 mA continuously at an ambient temperature of 25°C and a supply of 35 V. The overcurrent

*Continued on the next page...*

*Not to scale*

### Typical Application



## Description (continued)

fault circuit will protect the device from short-circuits to ground with supply voltages of up to 30 V.

The inputs are compatible with 5 and 12 V logic systems: TTL, Schottky TTL, DTL, PMOS, and CMOS. In all cases, the output is switched ON by an active high input level. Compared to their predecessor devices, the UDN2987A and UDN2987LW, the

UDN2987A-6 and UDN2987LW-6 have a significantly faster  $T_{PHL}$  (200 ns typical) and a lower driver supply voltage rating (4.75 V), which allows the use of 5 V logic.

The UDN2987A-6 is supplied in a 20-pin dual in-line plastic (DIP) package; the UDN2987LW-6 is supplied in a 20-lead small-outline (SOIC-W) plastic package. All packages are lead (Pb) free, with 100% matte-tin leadframe plating.

## Selection Guide

| Part Number     | Packing                 | Package                |
|-----------------|-------------------------|------------------------|
| UDN2987A-6-T*   | 18 pieces/tube          | 20-pin DIP             |
| UDN2987LWTR-6-T | 1000 pieces/13-in. reel | 20-pin SOIC, wide body |

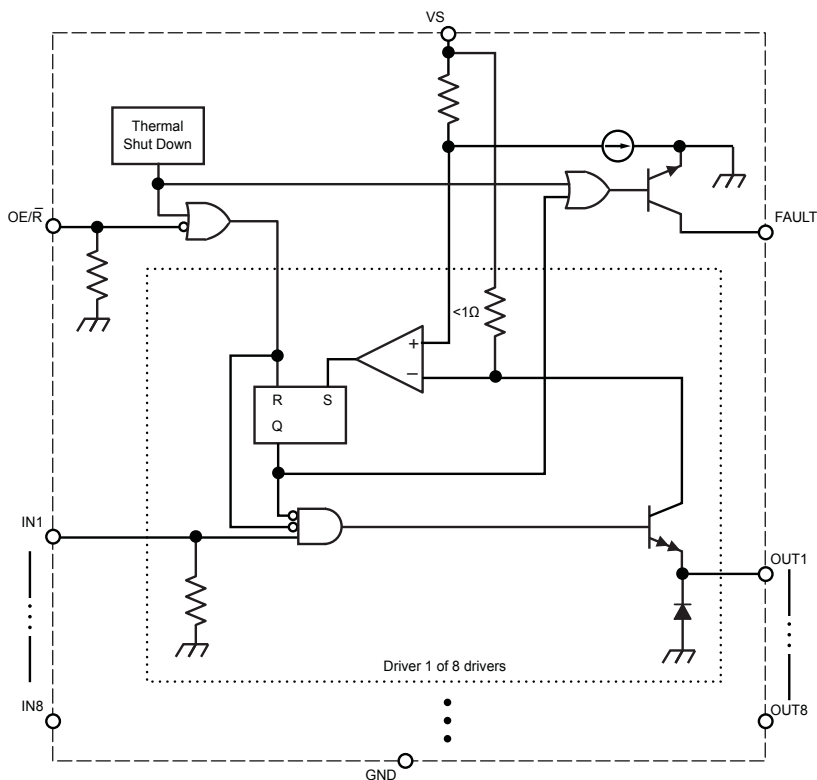
\*Variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change January 30, 2012. Deadline for receipt of LAST TIME BUY orders is April 27, 2012.

## Absolute Maximum Ratings

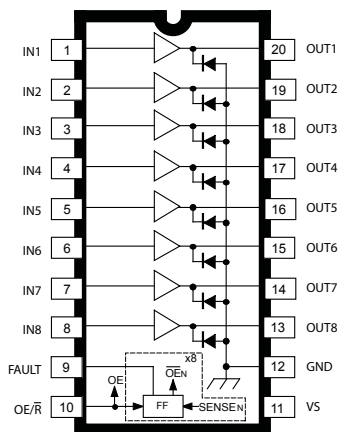
| Parameter                   | Symbol    | Notes   | Rating     | Units |
|-----------------------------|-----------|---|------------|-------|
| Supply Voltage              | $V_S$     |   | 35         | V     |
| Continuous Output Current*  | $I_{OUT}$ | Outputs are disabled at approximately -500 mA | -500       | mA    |
| FAULT Output Voltage        | $V_{CE}$  |   | 35         | V     |
| FAULT Output Current        | $I_C$     |   | 30         | mA    |
| Input Voltage               | $V_{IN}$  |   | -0.3 to 14 | V     |
| Junction Temperature        | $T_J$     |   | 150        | °C    |
| Storage Temperature Range   | $T_S$     | Range N                                       | -55 to 150 | °C    |
| Operating Temperature Range | $T_A$     |   | -20 to 85  | °C    |

\*For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.

## Functional Block Diagram



## Pin-Out Diagram



Dwg. PP-067

Package A (DIP) shown. Package LW (SOIC-W) is electrically identical and has the same terminal number assignment.

Terminal List Table

| Number | Name  | Description                             |
|--------|-------|---|
| 1      | IN1   | Logic input 1                           |
| 2      | IN2   | Logic input 2                           |
| 3      | IN3   | Logic input 3                           |
| 4      | IN4   | Logic input 4                           |
| 5      | IN5   | Logic input 5                           |
| 6      | IN6   | Logic input 6                           |
| 7      | IN7   | Logic input 7                           |
| 8      | IN8   | Logic input 8                           |
| 9      | FAULT | Fault output                            |
| 10     | OE/R  | Logic input for Output Enable and Reset |
| 11     | VS    | Supply voltage                          |
| 12     | GND   | Supply ground                           |
| 13     | OUT8  | Output 8 to load                        |
| 14     | OUT7  | Output 7 to load                        |
| 15     | OUT6  | Output 6 to load                        |
| 16     | OUT5  | Output 5 to load                        |
| 17     | OUT4  | Output 4 to load                        |
| 18     | OUT3  | Output 3 to load                        |
| 19     | OUT2  | Output 2 to load                        |
| 20     | OUT1  | Output 1 to load                        |

**ELECTRICAL CHARACTERISTICS, valid at  $T_A = 25^\circ\text{C}$ ,  $V_{OER} = 2.4\text{ V}$ ,  $V_S = 35\text{ V}$ , unless otherwise noted**

| Characteristic                           | Symbol         | Test Conditions   | Min. | Typ. <sup>1</sup> | Max. | Units            |
|--|----------------|---|------|-------------------|------|------------------|
| Supply Voltage Functional Range          | $V_S$          |   | 4.75 | —                 | 35   | V                |
| Output Leakage Current <sup>2</sup>      | $I_{OUTCEX}$   | $V_{IN} = 0.4\text{ V}$ , all inputs simultaneously                   | -200 | <-5.0             | -    | $\mu\text{A}$    |
| Output Sustaining Voltage                | $V_{OUT(SUS)}$ | $I_{OUT} = -350\text{ mA}$ , $L = 2.0\text{ mH}$                      | 35   | —                 | —    | V                |
| Output Saturation Voltage                | $V_{OUT(SAT)}$ | $V_{IN} = 2.4\text{ V}$ , $I_{OUT} = -100\text{ mA}$                  | —    | 1.6               | 1.8  | V                |
|  |                | $V_{IN} = 2.4\text{ V}$ , $I_{OUT} = -225\text{ mA}$                  | —    | 1.7               | 1.9  | V                |
|  |                | $V_{IN} = 2.4\text{ V}$ , $I_{OUT} = -350\text{ mA}$                  | —    | 1.8               | 2.0  | V                |
| Channel Shut Down Threshold <sup>2</sup> | $I_M$          | $V_{IN} = 2.4\text{ V}$ , $V_S = 30\text{ V}$                         | -    | -500              | -370 | mA               |
| FAULT Leakage Current                    | $I_{CEX}$      | $V_{CC} = 35\text{ V}$  | —    | <1.0              | 100  | $\mu\text{A}$    |
| FAULT Saturation Voltage                 | $V_{CE(SAT)}$  | $I_C = 30\text{ mA}$  | —    | 0.3               | 0.8  | V                |
| Input Voltage                            | $V_{IN(ON)}$   |   | 2.4  | —                 | —    | V                |
|  | $V_{IN(OFF)}$  |   | —    | —                 | 0.4  | V                |
| Input Current: INx, OE/ $\bar{R}$ pins   | $I_{IN(ON)}$   | $V_{IN} = 2.4\text{ V}$   | —    | —                 | 100  | $\mu\text{A}$    |
|  |                | $V_{IN} = 5.0\text{ V}$   | —    | —                 | 600  | $\mu\text{A}$    |
|  |                | $V_{IN} = 12\text{ V}$  | —    | —                 | 1000 | $\mu\text{A}$    |
|  | $I_{IN(OFF)}$  | $V_{IN} = 0.4\text{ V}$   | —    | —                 | 15   | $\mu\text{A}$    |
| Clamp Diode Leakage Current              | $I_R$          | $V_R = 35\text{ V}$ , $T_A = 70^\circ\text{C}$                        | —    | —                 | 50   | $\mu\text{A}$    |
| Clamp Diode Forward Voltage              | $V_F$          | $I_F = 350\text{ mA}$   | —    | 1.5               | 1.8  | V                |
| Supply Current                           | $I_{S(ON)}$    | $V_{IN} = 2.4\text{ V}$ , all inputs simultaneously; outputs open     | —    | 7.0               | 18   | mA               |
|  | $I_{S(OFF)}$   | $V_{IN} = 0.4\text{ V}$ , all inputs simultaneously                   | —    | 6.0               | 12   | mA               |
| Thermal Shut Down                        | $T_{JTSD}$     |   | —    | 165               | —    | $^\circ\text{C}$ |
| Thermal Hysteresis                       | $T_{JTSDhys}$  |   | —    | 15                | —    | $^\circ\text{C}$ |
| Reset Pulse Duration                     | $t_{RPD}$      |   | 1.0  | —                 | —    | $\mu\text{s}$    |
| Propagation Delay Time                   | $t_{PLH}$      | $V_S = 35\text{ V}$ , $R_L = 100\ \Omega$ , $C_{LOAD} = 30\text{ pF}$ | —    | 100               | 600  | ns               |
|  | $t_{PHL}$      | $V_S = 35\text{ V}$ , $R_L = 100\ \Omega$ , $C_{LOAD} = 30\text{ pF}$ | —    | 200               | 1000 | ns               |
| Blank Time                               | $t_{BLANK}$    |   | —    | 1.0               | —    | $\mu\text{s}$    |

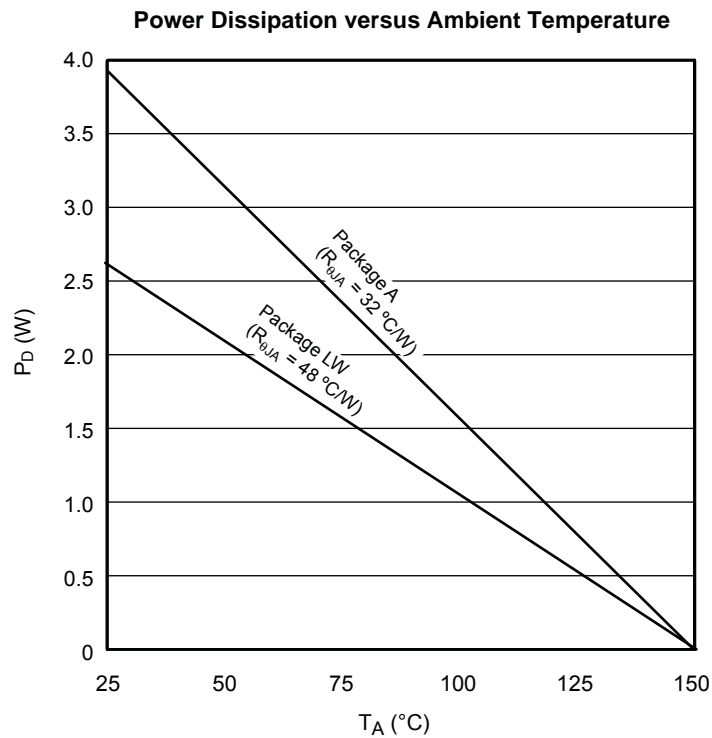
<sup>1</sup>Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.

<sup>2</sup>For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.

## THERMAL CHARACTERISTICS

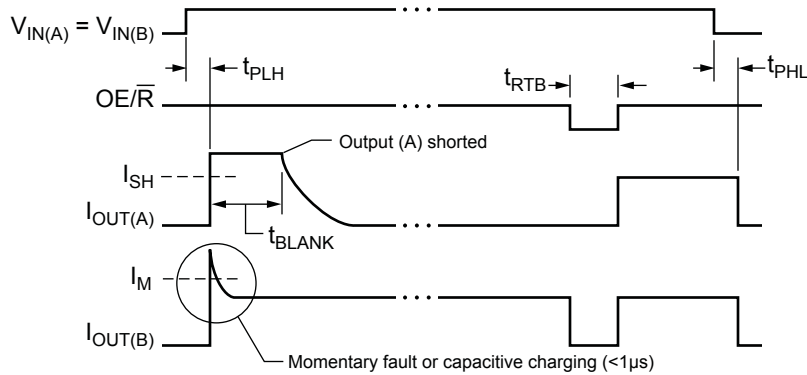
| Characteristics             | Symbol          | Test Conditions                                      | Rating | Unit |
|-----------------------------|-----------------|--|--------|------|
| Package Thermal Resistance* | $R_{\theta JA}$ | Package A, on 4-layer board based on JEDEC standard  | 32     | °C/W |
|                             |                 | Package LW, on 4-layer board based on JEDEC standard | 48     | °C/W |

\*Additional thermal information is available on the Allegro Web site.



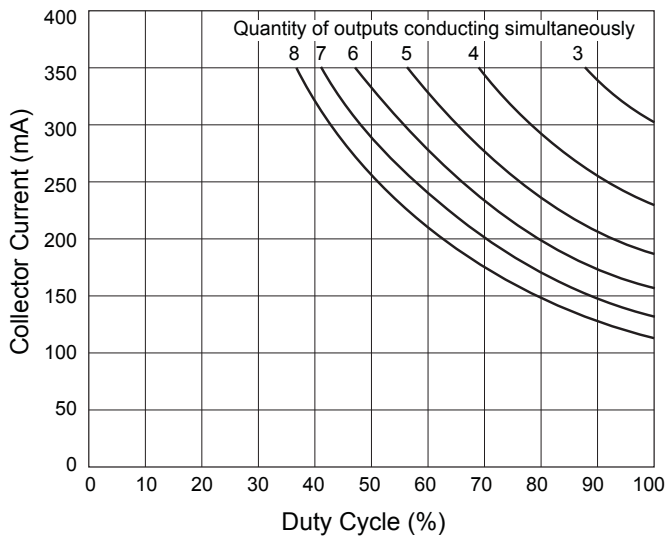
## Characteristic Performance

### Output Current Waveshapes

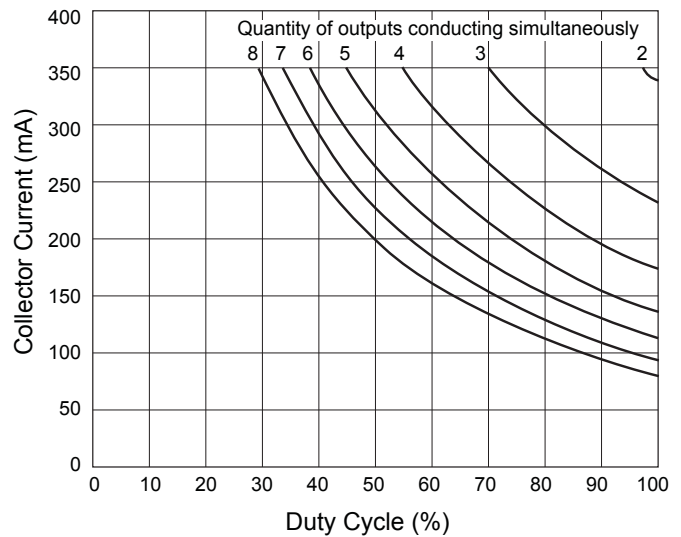


### Allowable Output Current as a Function of Duty Cycle (UDN2987A-6 shown, multiply by 78% for UDN2987LW-6)

$T_A = 25^\circ\text{C}, V_S = 35\text{ V}$



$T_A = 50^\circ\text{C}, V_S = 35\text{ V}$



## Applications Information and Circuit Description

As with all power integrated circuits, the UDN2987A-6 and UDN2987LW-6 have a maximum allowable output current rating. The 500 mA rating does not imply that operation at that value is permitted or even obtainable. The channel output current trip point is specified as  $-370$  mA, minimum; therefore, attempted operation at current levels greater than  $-370$  mA may cause a fault indication and channel shut down. The device is tested at a maximum of  $-350$  mA and that is the recommended maximum output current per driver. It provides protection for current overloads or shorted loads up to 30 V.

All outputs are enabled by pulling the  $\text{OE}/\bar{\text{R}}$  input high. When  $\text{OE}/\bar{\text{R}}$  is low or allowed to float (internal pull-down), all outputs are inhibited and the latches are reset. Note that the reset pulse duration ( $\text{OE}/\bar{\text{R}}$  low) should be at least  $1 \mu\text{s}$ . This will ensure safe operation under attempted reset conditions with a shorted load. The latches are also reset during power-up, regardless of the state of the  $\text{OE}/\bar{\text{R}}$  input.

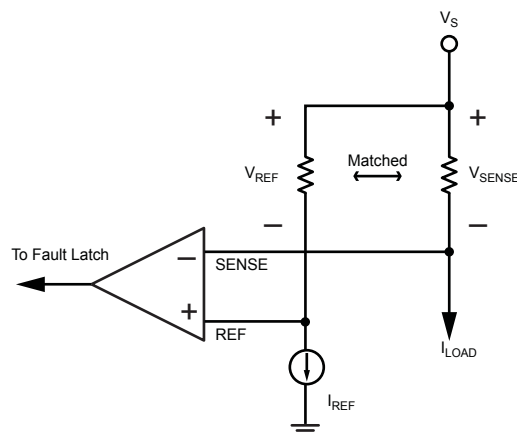
The load current causes a small voltage drop across the internal low-value sense resistor. This voltage is com-

pared to the voltage drop across a reference resistor with a constant current. The two resistors are matched to eliminate errors due to manufacturing tolerances or temperature effects. Each channel includes a comparator and its own latch. An overcurrent fault ( $V_{\text{SENSE}} > V_{\text{REF}}$ ) will set the affected latch and shut down only that channel. All other channels will continue to operate normally. The latch includes a  $1 \mu\text{s}$  blanking delay,  $t_{\text{BLANK}}$ , to prevent unwanted triggering due to crossover currents generated when switching inductive loads. For an abrupt short circuit, the blanking and output switching times will allow a brief, permissible current in excess of the trip current before the output driver is turned off.

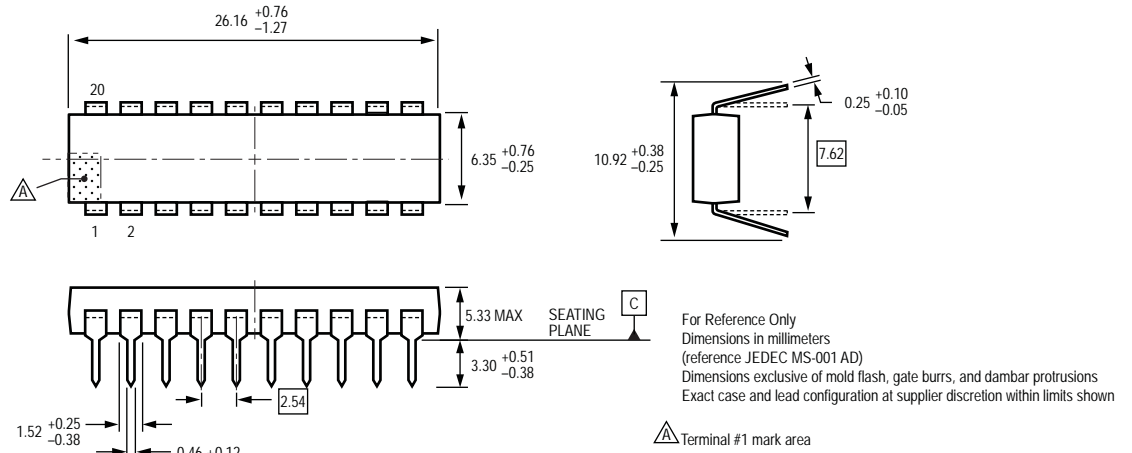
A common thermal shut down disables all outputs if the chip temperature exceeds  $165^\circ\text{C}$ . At thermal shut down, all latches are reset. The outputs are disabled until the chip cools down to approximately  $150^\circ\text{C}$  (thermal hysteresis).

In the event of an overcurrent condition on any channel, or chip thermal shut down, the FAULT open-collector output is pulled low (turned on).

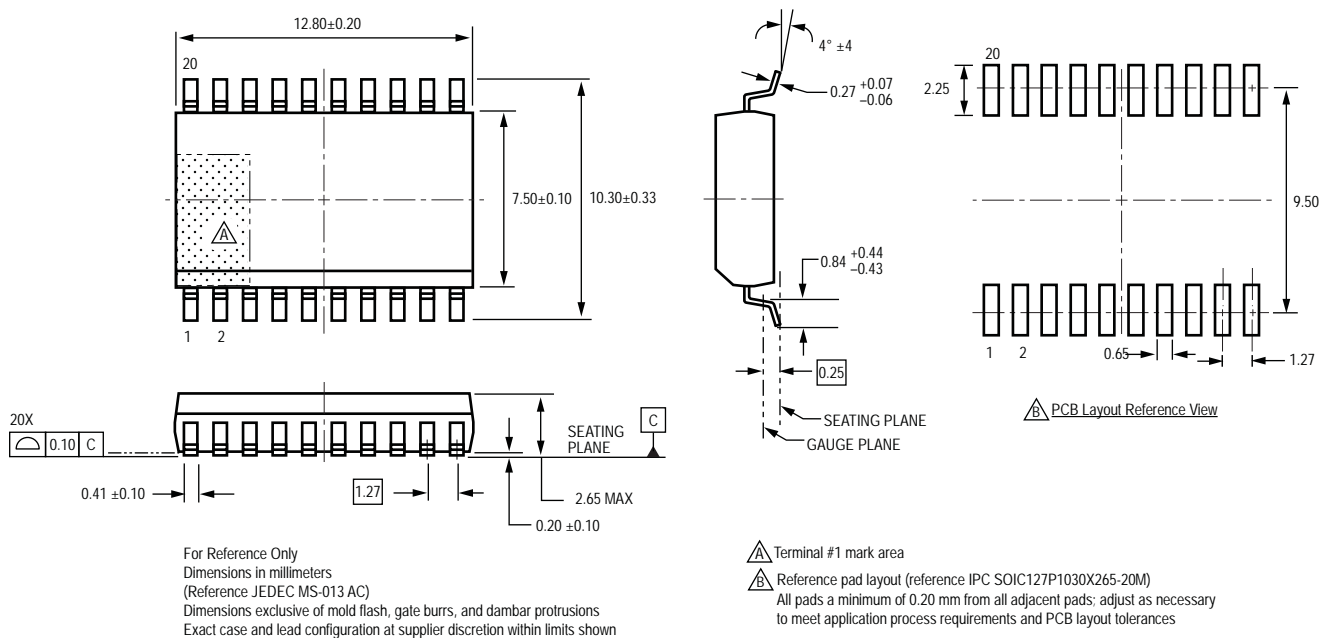
### Overcurrent Fault Sense Circuit



## Package A, 20-Pin DIP



## Package LW, 20-pin SOIC-W





**Revision History**

| Revision | Revision Date    | Description of Revision     |
|----------|------------------|-----------------------------|
| Rev. 5   | January 30, 2012 | Update product availability |
|          |                  |                             |

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