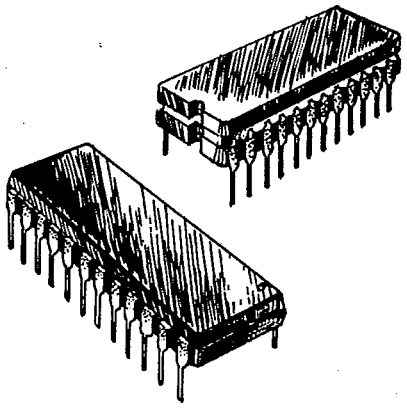
TELEDYNE SEMICONDUCTOR
The Analog Signal Processing Company™

TSC8703
TSC8704
TSC8705

BINARY OUTPUT ADCs

T-51-10-01



FEATURES

- High Accuracy — Up to 12 Bit Resolution With <±1/2 LSB Error
- Monotonic Performance — No Missing Codes
- Monolithic CMOS Construction Gives Low Power Dissipation — 20 mW Typical
- Contains All Required Active Elements — Needs only Passive Support Components, Reference Voltage and Dual Power Supply
- High Stability Over Full Temperature Range
  - Gain Temperature Coefficient Typically <25 ppm/°C
  - Zero Drift Typically <30 μV/°C
  - Differential Non-Linearity Drift Typically <25 ppm/°C
- Latched Parallel Binary Outputs
- LPTTL, 74LS, CMOS Compatible Outputs and Control Inputs
- Strobed or Free Running Conversion
- Infinite Input Range — Any Positive Voltage Can Be Applied Via a Scaling Resistor

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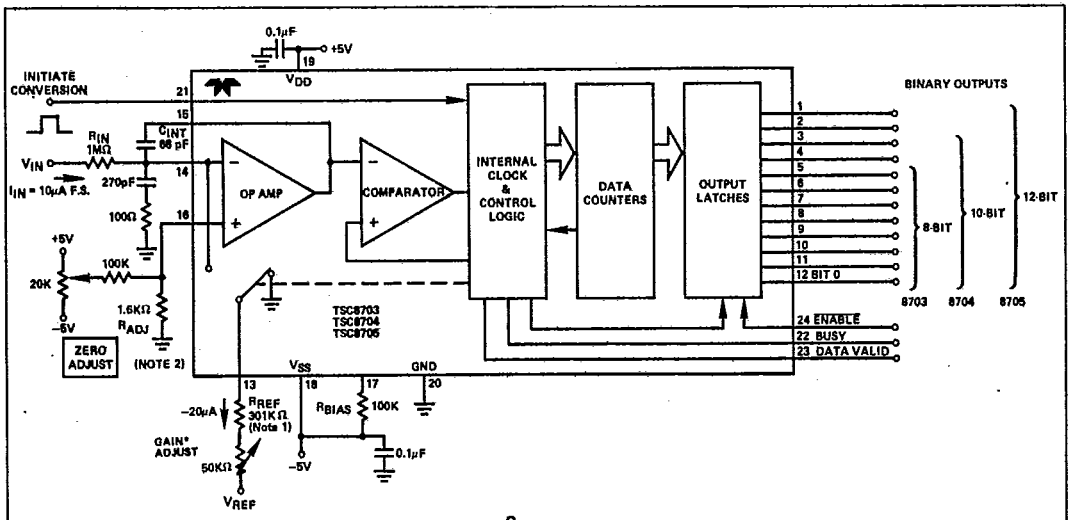
Test Circuit



Note:

1. Any V_{REF} greater than -1 V can be used.

$$R_{REF} = \frac{V_{REF}}{-20\ \mu A}$$

For example with V_{REF} = -5 V, R_{REF} = 250 k.

2.

Part No.	R_{ADJ}	C_{INT}	Zero Offset Spec
TSC8703	1.6 kΩ	68 pF	±80 mV
TSC8703	1.0 kΩ	33 pF	±50 mV
TSC8704/8705	1.0 kΩ	68 pF	±50 mV

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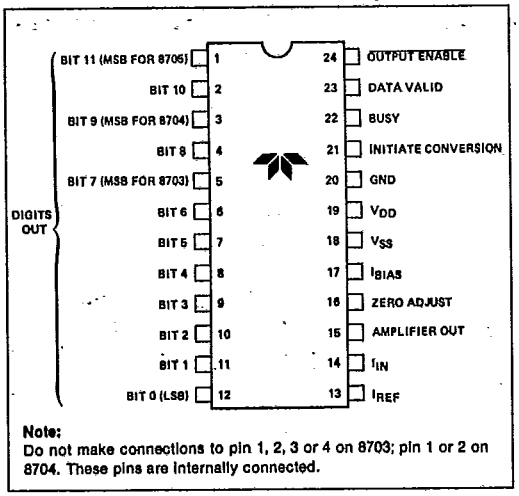
GENERAL DESCRIPTION

The TSC8703/8704/8705 are 8/10/12 bit monolithic CMOS analog-to-digital converters. Fully self-contained in a single 24-pin dual in-line package, each converter requires only passive support components, reference and power supplies.

Conversion is performed by an incremental charge balancing technique which has inherently high accuracy, linearity and noise immunity. An amplifier integrates the sum of the unknown analog current and pulses of a reference current, and the number of pulses (charge increments) needed to maintain the amplifier summing junction near zero is counted. At the end of conversion the total count is latched into the digital outputs as an 8/10/12 bit binary word. The Output Enable control switches the outputs to a high impedance or off state when held high. The off state allows bus organized output connections.

Pin Configuration



Note:
Do not make connections to pin 1, 2, 3 or 4 on 8703; pin 1 or 2 on 8704. These pins are internally connected.

Ordering Information

Part No.	Resolution	Conv. Time	Package	Temp. Range
TSC8703CJ	8-Bit	1.25 mSec	24-Pin Plastic Dip	0°C to +70°C
TSC8703CL	8-Bit	1.25 mSec	24-Pin CerDIP	-40°C to +85°C
TSC8703BL	8-Bit	1.25 mSec	24-Pin CerDIP	-55°C to +125°C
TSC8704CJ	10-Bit	5.0 mSec	24-Pin Plastic Dip	0°C to +70°C
TSC8704CL	10-Bit	5.0 mSec	24-Pin CerDIP	-40°C to +85°C
TSC8704BL	10-Bit	5.0 mSec	24-Pin CerDIP	-55°C to +125°C
TSC8705CJ	12-Bit	20 mSec	24-Pin Plastic Dip	0°C to +70°C
TSC8705CN	12-Bit	20 mSec	24-Pin Ceramic	-40°C to +85°C
TSC8705BN	12-Bit	20 mSec	24-Pin Ceramic	-55°C to +125°C
Devices with MIL-STD-883 Processing				
TSC8703BL/883	8-Bit	1.25 mSec	24-Pin CerDIP	-55°C to +125°C
TSC8704BL/883	10-Bit	5.0 mSec	24-Pin CerDIP	-55°C to +125°C
TSC8705BN/883	12-Bit	20 mSec	24-Pin Ceramic	-55°C to +125°C

Handling Precautions

The 8700 series are CMOS devices must be handled correctly to prevent damage. Package and store only in conductive foam, anti-static tubes or other conductive material. Use proper anti-static handling procedures. Do not connect in circuits under "power on" conditions, as high transients may cause permanent damage.

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Absolute Maximum Ratings

Storage Temperature ..... -65°C to + 150°C
Operating Temperature
- (BL, BN) ..... -55°C to +125°C
- (CL) Package ..... -40°C to + 85°C
- (CJ) Package ..... 0° to + 70°C

V_{DD} -V_{SS} ..... 18 V
I_{IN} ..... ±10 mA
I_{REF} ..... ±10 mA
Digital Input Voltage ..... -0.3 to V_{DD} +0.3 V
Operating V_{DD} and V_{SS} Range ..... 3.5 V to 7 V
Package Dissipation ..... 500 mW
Lead Temperature ..... 300°C
(Soldering, 10 seconds)

Electrical Characteristics: Unless otherwise specified, V_{DD} = +5 V, V_{SS} = -5 V, V_{GND} = 0, V_{REF} = -6.4 V, R_{BIAS} = 100 kΩ, test circuit shown. T_A = 25°C unless Full Temperature Range is specified (-55°C to +125°C for BN and BL package, -40°C to +85°C for CL package, 0° to 70°C for CJ package).

PARAMETER	CONDITIONS	DEFINITION	MIN	TYP	CJ/CN MAX	BN/BL MAX	UNITS
Accuracy							
Resolution		Binary Word Length					
Accuracy		Of Digital Output					
		TSC8703	8	—	—	—	Bits
		TSC8704	10	—	—	—	Bits
		TSC8705	12	—	—	—	Bits
Relative Accuracy		Output Deviation From Straight Line Between Normalized Zero and Full-Scale Input	—	±1/4	±1/2	±1/2	LSB
		TSC8705CJ (Only)	—	1.0	±1.5		LSB
Differential Non-Linearity		Deviation From 1 LSB Between Transition Points	—	±1/4	±1/2	±1/2	LSB
Differential Non-Linearity Temperature Drift	Full Temperature Range	Variation In Differential Non-Linearity Due To Temperature Change	—	±2.5	±5	±5	ppm/°C
Gain Variance		Variation From Exact A (Compensate By Trimming R_{IN} or R_{REF})		±2	±5	±5	% of Nominal
Gain Temperature Drift	Full Temperature Range	Variation In A Due To Temperature Change	—	±25	±75	±80	ppm/°C
Zero Offset (TSC8703)	I_{IN} = 0 C_{INT} = 68 pF R_{ADJ} = 1.6 kΩ See Test Circuit.	Correction at Zero Adjust to Give Zero Output When Input Is Zero Integration Cap. = 68 pF R_{ADJ} = 1.6 kΩ	—	—	±80	±80	mV
Zero Offset (TSC8703)	I_{IN} = 0 C_{INT} = 33 pF R_{ADJ} = 1.0 kΩ See Test Circuit.	Correction at Zero Adjust to Give Zero Output When Input Is Zero Integration Cap. = 33 pF R_{ADJ} = 1.0 kΩ	—	±10	±50	±50	mV
Zero Offset (TSC8704) (TSC8705)	I_{IN} = 0 C_{INT} = 68 pF R_{ADJ} = 1.0 kΩ See Test Circuit.	Correction at Zero Adjust to Give Zero Output When Input Is Zero Integration Cap. = 68 pF R_{ADJ} = 1.0 kΩ	—	±10	±50	±50	mV
Zero Temperature Drift	Full Temperature Range	Variation In Zero Offest Due to Temperature Change	—	±3	±5	±8	ppm/°C

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Electrical Characteristics (Cont.)

PARAMETER	CONDITIONS	DEFINITION	MIN	TYP	CJ/CN MAX	BN/B MAX	UNITS
Analog Inputs							
I_{IN} Full-Scale		Full-Scale Analog Input Current To Achieve Specified Accuracy	—	10	—	—	μA
I_{REF} (Note 1)		Reference Current Input To Achieve Specified Accuracy	—	-20	—	—	μA
Digital Inputs							
$V_{IN}^{(1)}$	Full Temperature Range	Logical "1" Input Threshold For Initiate Conversion Input	3.5	—	—	—	V
$V_{IN}^{(0)}$	Full Temperature Range	Logical "0" Input Threshold For Initiate Conversion Input	—	—	1.5	1.5	V
Propagation Delay							
Output Enable	C_L = 100 pF, R_L = 1 KΩ	T_{PLH}, T_{PHL}	—	500	—	1,000	ns
Digital Outputs							
$I_{O(OFF)}$	OE = 3.5 V, 0.4 V < V_O <2.4	Off-state Output Current	—	0.1	±10	±10	μA
$V_{OUT}^{(1)}$	Full Temp. Range	Logical "1" Output Voltage	4.5	—	—	—	V
	I_{OUT} = -10 μA	For Digits Out, Busy, and	2.4	—	—	—	V
	I_{OUT} = -500 μA	Data Valid Outputs					
$V_{OUT}^{(0)}$	Full Temp. Range V_{DD} = 4.75 V I_{OUT} = 500 μA	Logical "0" Output Voltage For Digits Out, Busy, and Data Valid Outputs	—	—	0.4	0.4	V
Dynamic							
Conversion Time	Full Temp. Range	Time Required to Perform One Complete A/D Conversion					
		TSC8703	—	1.25	1.8	1.8	ms
		TSC8704	—	5	6	6	ms
		TSC8705	—	20	24	24	ms
Conversion Rate In Free-Run Mode	$V_{INT\ CONV}$ = + 5 V	TSC8703	555	800	—	—	Conv'ns
		TSC8704	167	200	—	—	per
		TSC8705	42	50	—	—	Second
Minimum Pulse Width for Initiate Conversion	Full Temp. Range		500	—	—	—	ns
Supply Current							
I_{DD} Quiescent (L/N Package)	Full Temp. Range	Current Required From Positive	—	1.4	2.5	3.5	mA
(J Package)	$V_{INT\ CONV}$ = 0V	Supply During Operation	—	1.4	5.0		mA
I_{SS} Quiescent (L/N Package)	Full Temp. Range	Current Required From Negative	—	-1.6	-2.5	-3.5	mA
(J Package)	$V_{INIT\ CONV}$ = 0V	Supply During Operation	—	-1.6	-5.0		mA
Supply Sensitivity	V_{DD} ± 1 V, V_{SS} ±1 V	Change in Full-Scale Gain vs Supply Voltage Change	—	±0.5	±1.0	±1.0	%/V
	$\|V_{DD}\| = \|V_{SS}\|$ = 5 V ± 1 V	Change in Full-Scale Gain vs Supply Voltage Change for Tracking Supplies	—	±0.05	±0.1	±0.1	%/V

NOTE:
I_{IN} and I_{REF} pins connect to the summing junction of an operational amplifier. Voltage sources cannot be attached directly but must be buffered by external resistors. See Test Circuit.

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Circuit Description

During conversion the sum of a continuous current I_{IN} and pulses of a reference current I_{REF} is integrated for a fixed number of clock periods. I_{IN} is proportional to the analog input voltage; I_{REF} is switched in for exactly one clock period just frequently enough to maintain the output of the integrator near zero. Thus, the charge from the continuous I_{IN} current is balanced against the pulses of I_{REF} current. The total number of I_{REF} pulses needed during the conversion period to maintain the charge balance is counted, and the result (in Binary) is latched into the outputs at the end of the conversion.

The converter contains two counters and a clock in addition to an operational amplifier, comparator, latching output buffers and housekeeping logic. One counter is a clock counter which (after a reset pulse) starts counting clock pulses; when the required count is reached, the clock counter generates a pulse to start the end-of-conversion routine. The other counter is a data counter, which is reset synchronously with the clock counter and counts the number of times the I_{REF} current is switched into the summing input of the amplifier during the period defined by the clock counter.

When the Initiate Conversion input is strobed with a positive signal, the busy line latches high and a 10 μs (times given are approximate) start up cycle begins. The integrating capacitor is discharged and both counters are reset during this start up period. Conversion begins at the end of the reset pulse and ends with a pulse generated either by the clock counter or by an overflow condition in the data counter. This pulse disables further inputs into both counters and triggers a 10 μs shutdown cycle. During the shutdown cycle Data Valid goes low for 5 μs. This binary sequence is shown in the timing diagrams. Busy is true high, and when the circuit is busy, Initiate Conversion has no effect and may be high or low. Data Valid is also true high. The data from a conversion remain valid for as long as power is applied to the circuit or until Data Valid falls at the end of a subsequent conversion, at which time the output data are updated to reflect the latest conversion.

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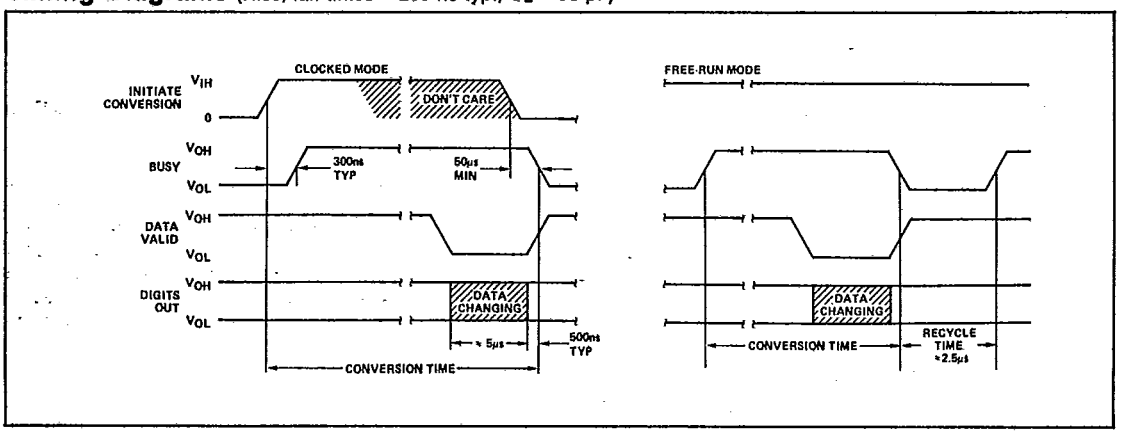
Timing Diagrams (Rise, fall times = 200 ns typ., C_L = 50 pF)



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Pin Functions

Initiate Conversion Input

Accepts CMOS and most 5 V logic inputs. Applying a logic "1" to the Initiate Conversion pin initiates the A/D conversion cycle. Once conversion has been initiated, the cycle cannot be interrupted, and the Initiate Conversion pin is disabled until conversion is complete. Two modes of operation are permitted, clocked or free-running. For clocked operation the Initiate Conversion input is held at logic "0" for standby and taken to logic "1" when a conversion is desired. For free-running operation the Initiate Conversion pin is connected to V_{DD} or similar permanent logic "1" voltage.

Busy Output

A digital status output which is compatible with CMOS logic and low power TTL (can sink and source 500 μA). A logic "1" output on the Busy pin indicates a conversion cycle is in process. A logic "1" to logic "0" transition indicates that conversion is complete and the result has been latched at the Digits Out pins. A logic "0" to logic "1" transition indicates a new conversion cycle has been initiated. If the device is operating in the free-running mode, the Busy output will remain low for approximately 2.5 μs, marking the completion and initiation of consecutive conversion cycles.

Data Valid Output

A digital status which is compatible with CMOS logic and low power TTL (can sink and source 50 μA). A logic "1" output at the Data Valid pin indicates that the Digits Out pins are latched with the result of the last conversion cycle. The Data Valid output goes to logic "0" approximately 5 μs before the completion of a conversion cycle. During this 5 μs interval new data is being transferred to the Digits Out pins, and the Digits Out are not valid.

Digits Out
(Bit 0, Bit 1, etc.)

The binary digit outputs which are the result of the A/D conversion. These outputs are CMOS logic and low power TTL compatible.

Applications Information

Input/Output Relationships

The analog input voltage (V_{IN}) is related to the output by the transfer equation:

$$\text{Digital Counts} = \frac{V_{IN} \cdot A \cdot R_{REF}}{R_{IN} \cdot V_{REF}}$$

A = 528 for 8703
A = 2064 for 8704
A = 8208 for 8705

where Digital Counts is the value of the binary output word presented at Digits Out pins in response to V_{IN}.

The digital output code format is as follows:

Analog Input	Digital Output MSB LSB
$V_{IN} \leq$ Full-Scale	1 . . . 111 . . . 1
= Full-Scale -1 LSB	1 . . . 111 . . . 1
= 1 LSB	0 . . . 000 . . . 1
≤ 0	0 . . . 000 . . . 0

Two's complement coding can be generated by inverting the Most Significant Bit (MSB) signal.

External Component Selection

Obtaining a high accuracy conversion system depends on the voltage regulation of V_{REF} and the thermal stability of R_{IN} and R_{REF}. The exact dependence is given by the transfer function. System accuracy also depends, to a lesser degree, on the voltage regulation of V_{DD} and V_{SS}. The supply connections V_{DD} and V_{SS} should have bypass capacitors of value 0.1 μF or larger right at the device pins.

R_{IN}, R_{EF}

Values of these components are chosen to give a full-scale input current of approximately 10 μA and a reference current of approximately -20 μA.

$$R_{IN} \cong \frac{V_{IN}\ \text{Full-Scale}}{10\ \mu A} \qquad R_{REF} \cong \frac{V_{REF}}{-20\ \mu A}$$

Examples:

$$R_{IN} \cong \frac{10\ V}{10\ \mu A} = 1\ M\Omega \qquad R_{REF} \cong \frac{-6.4\ V}{-20\ \mu A} = 320\ k\Omega$$

Note that these values are approximations, and the exact relationships are defined by the transfer equation. In practice, the value of R_{IN} typically would be trimmed using the optional gain adjust circuit to obtain full-scale output at V_{IN} full-scale (see adjustment procedure). Metal film resistors with 1% tolerance or better are recommended for high accuracy applications because of their thermal stability and low noise generation.

R_{BIAS}

Specifications for the 87XX are based on R_{BIAS} = 100 kΩ ±10% unless otherwise noted. However, there are instances when the designer may want to change this resistor in order to affect the conversion time and the supply current. By decreasing R_{BIAS} the A/D will convert much faster and the supply current will be higher. (For example: When R_{BIAS} is 20 k the conversion time is reduced by 1/3, and the supply current will increase from 2 mA to 7 mA.) Likewise, if the R_{BIAS} is increased the conversion time will be longer and the supply current will be much lower. (For example: When R_{BIAS} = 1 mΩ the conversion time will be six times longer, and supply current is now reduced to .5 mA). For details of this relationship refer to AN9 typical performance curves.

Applications Information (Cont.)

RDAMP

Exact value not critical but should have a nominal value of 100 Ω ±10%. Locate close to pin 14.

CDAMP

Exact value not critical but should have a nominal value of 270 pF ±20%. Locate close to pin 14.

CINT

Exact value not critical but should have a nominal value of 68 pF ± 10%. Low leakage types are recommended, although mica or ceramic devices can be used in applications where their temperature limits are not exceeded. Locate as close as possible to pins 14, 15. For the TSC8703 C_{INT} = 33 pF is adequate with R_{ADJ} = 1 kΩ.

VREF

A negative reference voltage must be supplied. This may be obtained from a constant current source circuit or from the negative supply.

VDD, VSS

Power supplies of ±5 V are recommended, with 0.05% line and load regulation and 0.1 μF decoupling capacitors.

Adjustment Procedure

The test circuit diagram shows optional circuits for trimming the zero location and full-scale gain. Because the digital outputs remain constant outside of the normal operating range (i.e. below zero and above full-scale), it is recommended that transition points be used in setting the zero and full-scale values. Recommended procedure is as follows:

- Set the initiate conversion control high to provide free-run operation and verify that converter is operating.
- Set V_{IN} to +1/2 LSB and trim the zero adjust circuit to obtain a 000 . . . 000 . . . to 000 . . . 001 transition. This will correctly locate the zero end.
- For full-scale adjustment, set V_{IN} to the full-scale value less 1 1/2 LSB and trim the gain adjust circuit for a 111 . . . 110 to 111 . . . 111 transition.

If adjustments are performed in this order, there should be no interaction and they should not have to be repeated.

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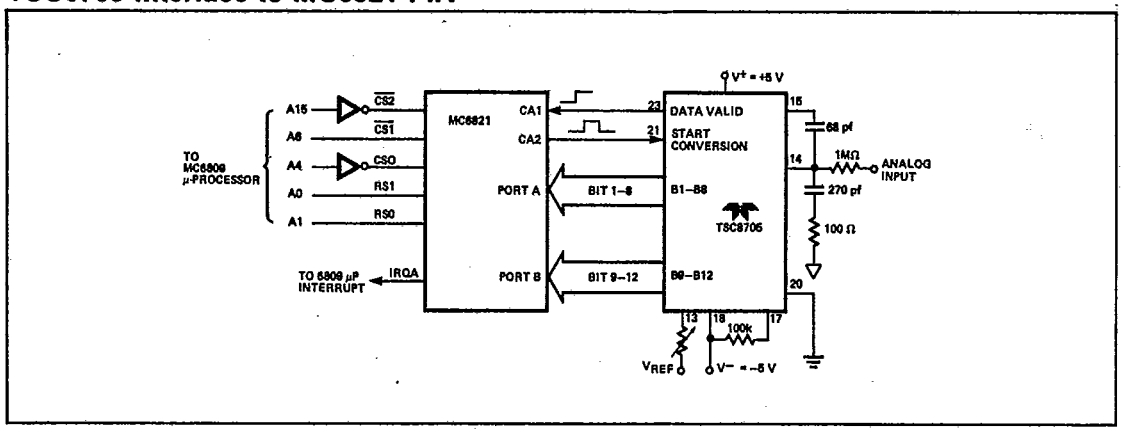
TSC8705 Interface to MC6821 PIA



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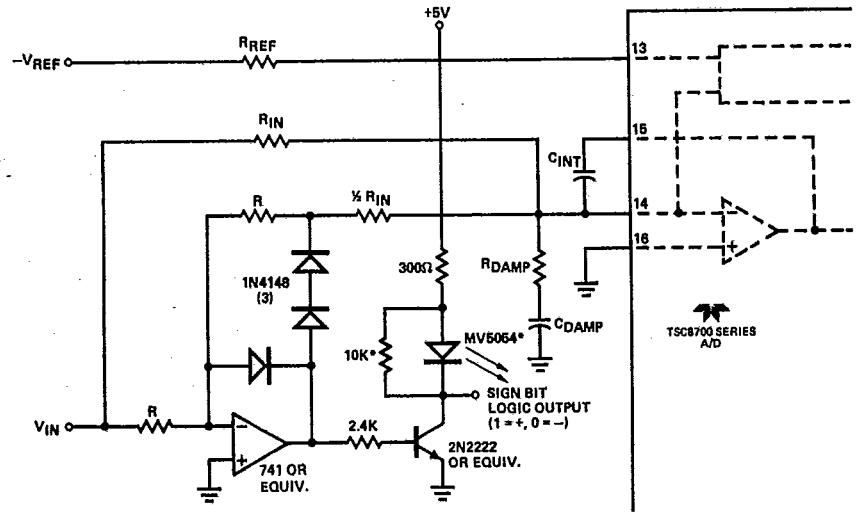
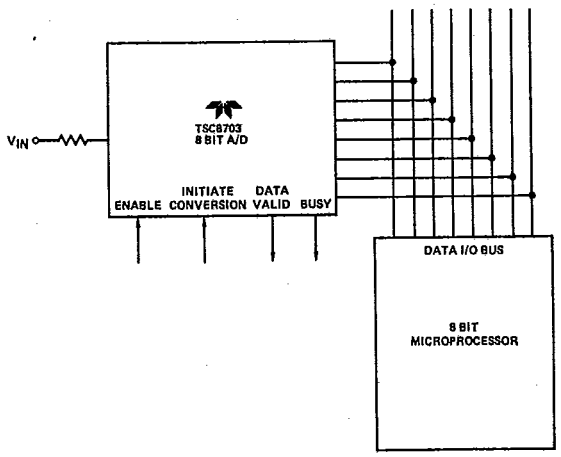
Application/Design Circuits
Bipolar Operation (+ and -Inputs)



*Optional visual indication of negative input
NOTE: Values for R should be between 10KΩ and 100KΩ

Absolute Value Circuit With Sign

8-Bit Microprocessor Interface



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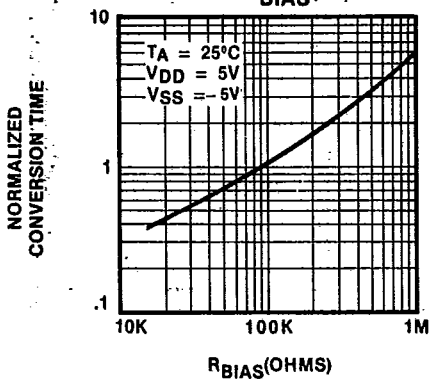
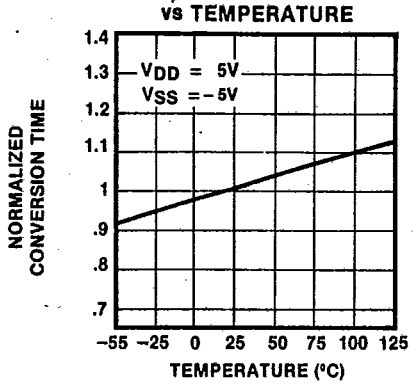
TYPICAL PERFORMANCE CURVES

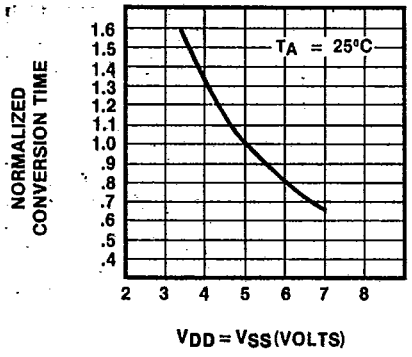
CONVERSION TIME vs R_{BIAS}



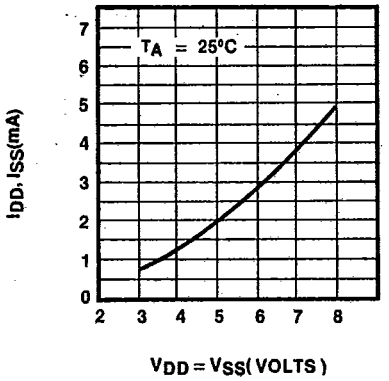
CONVERSION TIME vs TEMPERATURE



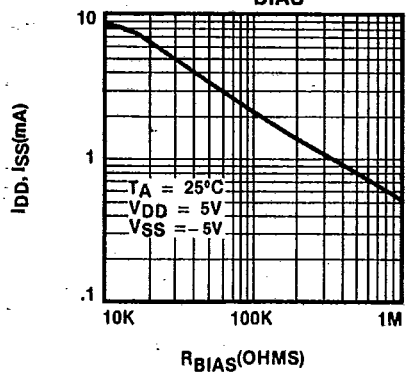
CONVERSION TIME vs SUPPLY VOLTAGE



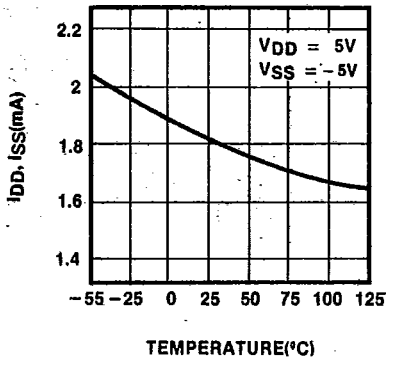
SUPPLY CURRENT vs SUPPLY VOLTAGE



SUPPLY CURRENT vs R_{BIAS}



SUPPLY CURRENT vs TEMPERATURE



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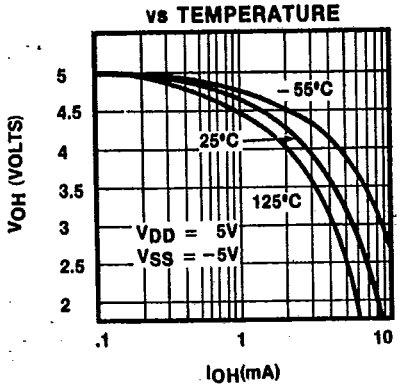
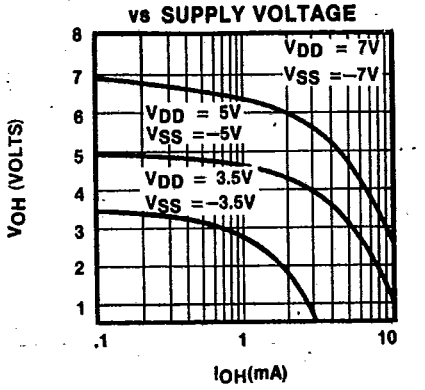
TYPICAL PERFORMANCE CURVES

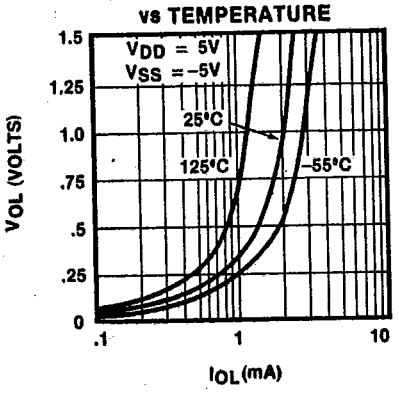
OUTPUT SOURCE CURRENT vs TEMPERATURE



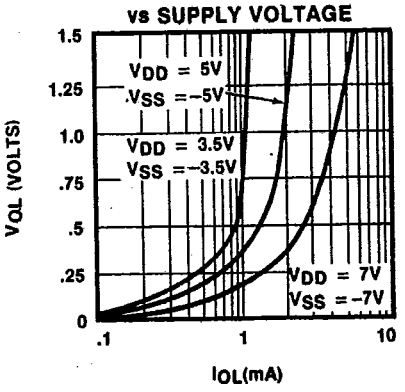
OUTPUT SOURCE CURRENT vs SUPPLY VOLTAGE



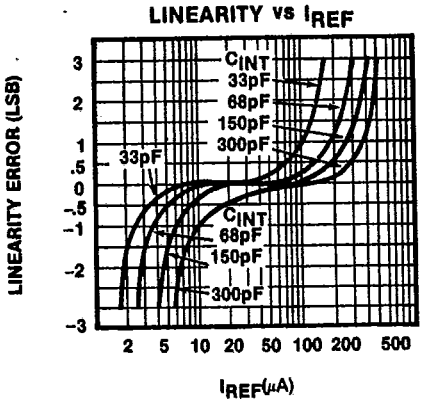
OUTPUT SINK CURRENT vs TEMPERATURE



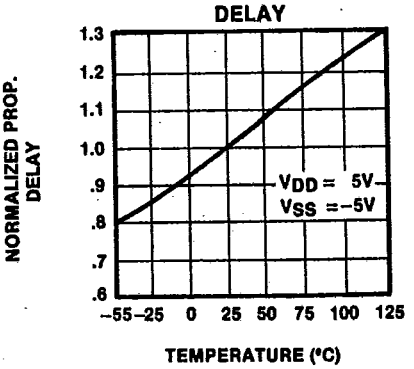
OUTPUT SINK CURRENT vs SUPPLY VOLTAGE



LINEARITY vs I_{REF}



TRI-STATE PROPAGATION DELAY

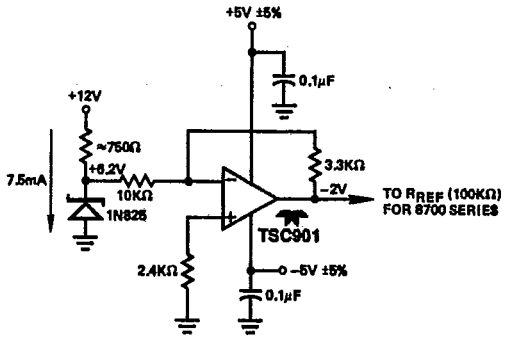


PRODUCT INFORMATION T-51-10-01

TSC8703
TSC8704
TSC8705

Application/Design Circuits (Cont.)

Reference Voltage Supply

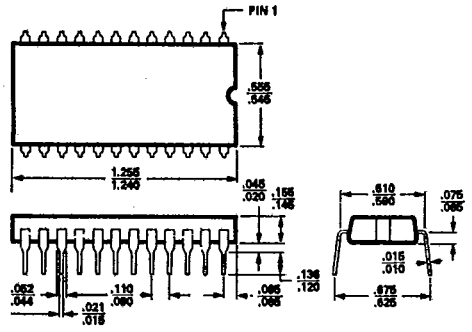


2 V Reference Voltage Using Voltages Derived from 8080A μP.

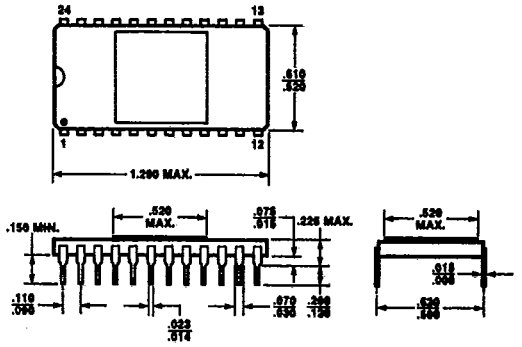
8

Package Information

24-Pin Plastic Dip (J Package)
(Package #12)



24-Pin Ceramic Dip (N Package)
(Package #13)



24-Pin CerDIP (L Package)
(Package #14)