HCMOS MULTI FUNCTION PERIPHERAL

DESCRIPTION

The TS 68C901B multi-function peripheral (CMFP) is a member of the TS 68000 Family of peripheral and the CMOS version of the TS 68901. The CMFP directly interfaces to the TS 68000 processor family via an asynchronous bus structure and can also support both multiplexed and non multiplexed buses. Both vectored, non vectored and polled interrupt schemes are supported, with the CMFP providing unique vector number generation for each of its 16 interrupt sources. Additionally, handshake line are provided to facilitate DMAC interfacing.

The TS 68C901B performs many of the functions common to most microprocessor-based systems.

By incorporating multiple functions within the CMFP, the system designer retains flexibility while minimizing device' count.

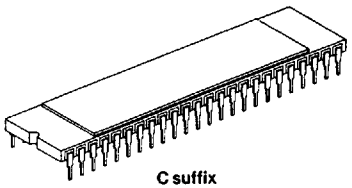
MAIN FEATURES

- 8 input/output pins
  - Individually programmable direction
  - Individual interrupt source capability
    - Programmable edge selection.
- 16 source interrupt controller
  - 8 internal sources
  - 8 external sources
  - Individual source enable
  - Individual source masking
  - Programmable interrupt service modes
    - Polling
    - Vector generation
      - Optimal in-service status
  - Daisy chaining capability.
- Four timers with individually programmable prescaling
  - Two multimode timers
    - Delay mode
    - Pulse width measurement mode
    - Event counter mode
  - Two delay mode timers
  - Independent clock input
  - Time out output option.
- Single channel USART
  - Full duplex
  - Asynchronous to 65 kbps
  - Byte synchronous to 1 Mbps
  - Internal/external baud rate generation
  - DMA handshake signals
  - Modem control
  - Loop back mode.
- 68000 Bus compatible.
- CMOS technology
  low power dissipation P_D = 55 mW max.
- Available in 4, 5 and 8 MHz.
- See application note.

SCREENING / QUALITY

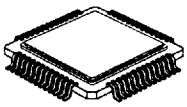
This product is manufactured in full compliance with :

- CECC 90000 (class B, quality assessment level Y).
- MIL-STD-883 (class B).
- DESC Drawing : 5962-90864.
- TCS STANDARDS.

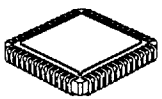


C suffix
DIL 48
Ceramic Side Brazed package

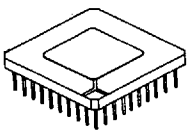
E suffix
LCCC 52
Leadless Ceramic Chip Carrier



F suffix
CQFP 52
Ceramic Quad Flat Pack



W suffix
LDCC 52
Leaded Ceramic Chip Carrier
(on request only)



F suffix
PGA 68
Ceramic Pin Grid Array

PIN CONNECTIONS (see A2)

Ordering information (see chapter 10).

5

SUMMARY

A - GENERAL DESCRIPTION

1 - DETAILED BLOCK DIAGRAM

2 - PIN ASSIGNMENTS

3 - TERMINAL DESIGNATIONS

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- 9.3 - 52 Pins - Leaded ceramic chip carrier
- 9.4 - 52 Pins - Ceramic quad flat pack
- 9.5 - 68 Pins - Pin Grid Array

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- 10.2 - Standard product
- 10.3 - Detailed TS 68C901B part list

A - GENERAL DESCRIPTION

INTRODUCTION

The TS 68C901B CMFP (Multi-Function Peripheral) is a combination of many of the necessary peripheral functions in a microprocessor system. Included are :

- Eight parallel I/O lines,
- Interrupt controller for 16 sources,
- Four timers,
- Single channel full duplex USART.

The use of the CMFP in a system can significantly reduce chip count, thereby reducing system cost. The CMFP is completely 68000 bus compatible, and 24 directly addressable internal registers provide the necessary control and status interface to the programmer.

1 - DETAILED BLOCK DIAGRAM

The functional block diagram is given in Figure 1 below.

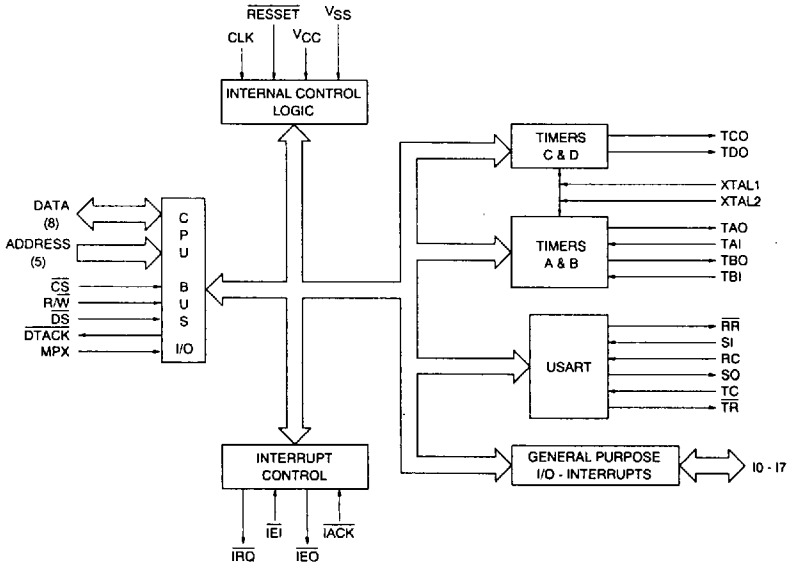

Figure 1 : Functional block diagram.

2 - PIN ASSIGNMENTS

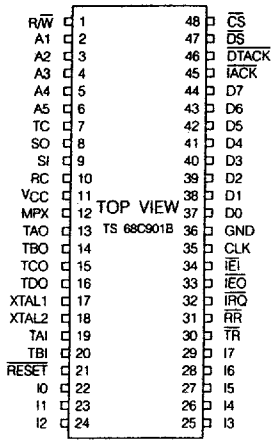

Figure 2.1 : Pin DIL package.

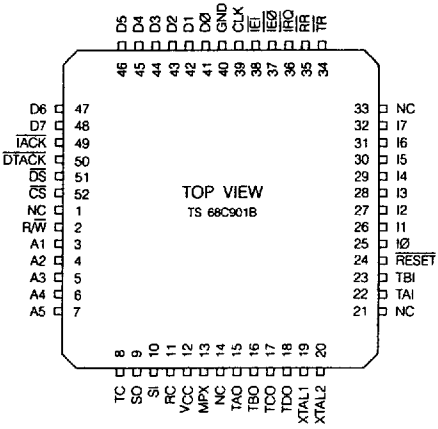

Figure 2.2 : Terminal Chip Carrier package.
(codes : E and W).

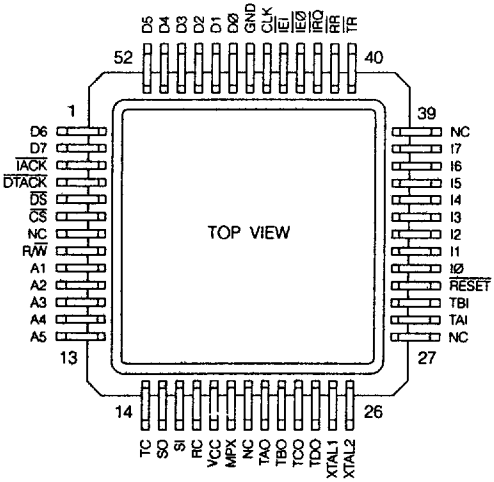

Figure 2.3 : CQFP terminal designation.

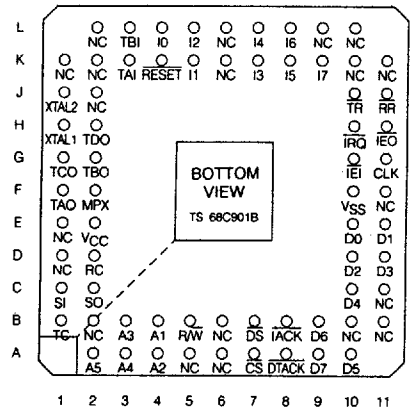

Figure 2.4 : PGA terminal Pin Grid Array.

3 - TERMINAL DESIGNATIONS

The function, category and relevant symbol of each terminal of the device are given in the following table :

Table 1

Symbol	Function	Category
V_{CC}	Power supply	Supply Terminals
V_{SS}*	Power supply	
$\overline{CS}$	Chip select	Input
$\overline{DS}$	Data strobe	Input
R/$\overline{W}$	Read/Write	Input
$\overline{DTACK}$	Data transfert acknowledge	Output
A1 to A15	Address bus	Inputs
D0 to D7	Data bus	Bi-directionnal
CLK	Clock	Input
$\overline{RESET}$	Device Reset	Input
$\overline{IRQ}$	Interrupt Request	Output
$\overline{IACK}$	Interrupt Acknowledge	Input
$\overline{IEI}$	Interrupt Enable In	Input
$\overline{IEO}$	Interrupt Enable Out	Output
I0-I7	General purpose interrupt I/O lines	Bi-directionnal
SO	Serial Output	Output
SI	Serial Input	Input
TC	Transmitter Clock	Input
MPX	Multiplex Mode Select	Input
XTAL 1, 2	Timer clock	Input
TAI, TBI	Timer input	Input
TAO, TBO, TCO, TDO	Timer output	Output
RC	Receiver clock	Input
$\overline{RR}$	Receiver ready	Output
$\overline{TR}$	Transmitter ready	Output

* V_{SS} is the reference terminal for the voltage.

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4 - SIGNAL DESCRIPTION

The input and output signals can be functionnaly organized into the groups shown in Figure 3.

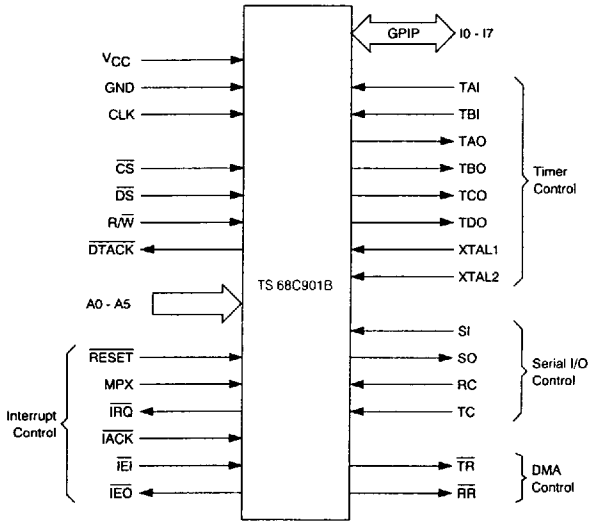

Figure 3 : Input and output signals.

4.1 - Pin description

GND : Ground.

V_{CC} : +5 Volts (± 10 %).

$\overline{CS}$: Chip Select (input, active low). $\overline{CS}$ is used to select the TS 68C901B for accesses to the internal registers. $\overline{CS}$ and IACK must not be asserted at the same time.

$\overline{DS}$: Data Strobe (input, active low). $\overline{DS}$ is used as part of the chip select and interrupt acknowledge functions.

R/$\overline{W}$: Read/Write (input). R/$\overline{W}$ is the signal from the bus master indicating whether the current bus cycle is a Read (High) or Write (Low) cycle.

$\overline{DTACK}$: Data Transfert Acknowledge (output, active low, tri-stateable). $\overline{DTACK}$ is used to signal the bus master that the data is ready, or that data has been accepted by the TS 68C901B.

A1-A5 : Address Bus (inputs). The address bus is used to address one of the internal registers during a read or write cycle.

D0-D7 : Data Bus (bi-directionnal, tri-stateable). The data bus is used to receive data from or transmit data to one of the internal registers during a read or write cycle. It is also used to pass a vector during an interrupt acknowledge cycle.

CLK : Clock (input). This input is used to provide the internal timing for the TS 68C901B.

$\overline{RESET}$: Device reset (input, active low). Reset disables the USART receiver and transmitter, stops all timers and forces the timer outputs low, disables all interrupt channels and clears any pending interrupts. The General Purpose Interrupt I/O lines will be placed in the tri-stated input mode. All internal registers (except the timer, USART data registers, and transmit status register) will be cleared.

$\overline{IRQ}$: Interrupt Request (output, active low, open drain). $\overline{IRQ}$ is asserted when the TS 68C901B is requesting an interrupt. $\overline{IRQ}$ is negated during an interrupt acknowledge cycle or by clearing the pending interrupt(s) through software.

$\overline{IACK}$: Interrupt Acknowledge (input, active low). $\overline{IACK}$ is used to signal the TS 68C901B that the CPU is acknowledging an interrupt. $\overline{CS}$ and $\overline{IACK}$ must not be asserted at the same time.

$\overline{IEI}$: Interrupt Enable In (input, active low). $\overline{IEI}$ is used to signal the TS 68C901B that no higher priority device is requesting interrupt service.

$\overline{IEO}$: Interrupt Enable Out (output, active low). $\overline{IEO}$ is used to signal lower priority peripherals that neither the TS 68C901B nor another higher priority peripheral is requesting interrupt service.

I0-I7 : General Purpose Interrupt I/O lines. These lines may be used as interrupt inputs and/or I/O lines. When used as interrupt inputs, their active edge is programmable. A data direction register is used to define which lines are to be Hi-Z inputs and which lines are to be push-pull TTL compatible outputs.

SO : Serial Output. This is the output of the USART transmitter. This output is configured by the TSR register.

SI : Serial Input. This is the input to the USART receiver.

RC : Receiver Clock. This input controls the serial bit rate of the USART receiver.

TC : Transmitter Clock. This input controls the serial bit rate of the USART transmitter.

$\overline{RR}$: Receiver Ready (output, active low). DMA output for receiver, which reflects the same status of Buffer Full in port number 15.

$\overline{TR}$: Transmitter Ready (output, active low). DMA output for transmitter, which reflects the status of Buffer Full in port number 16.

TAO, TBO
TCO, TDO : Timer Outputs. Each of the four timers has an output which can produce a square wave. The output will change states each timer cycle ; thus one full period of the timer out signal is equal to two timer cycles. TAO or TBO can be reset (logic «0») by a write to TACR or TBCR respectively.

XTAL 1
XTAL 2 : Timer Clock Inputs. A crystal can be connected between XTAL1 and XTAL2, or XTAL1 can be driven with EXTERNAL clock. When driving XTAL1 with EXTERNAL clock. XTAL2 must be allowed to float. When using a crystal, external capacitors are required. See Figure 19. All chip accesses are independent of the timer clock.

TAI, TBI : Timer A, B Inputs. Used when running the timers in the event count or the pulse width measurement mode. The interrupt channels associated with 14 and 13 are used for TAI and TBI respectively. Thus, when running a timer in the pulse width measurement mode, 14 or 13 can be used for I/O only.

MPX : This signal select the data bus mode :
MPX = 0 : non multiplex mode
MPX = 1 : multiplex mode. The register select lines RS1-RS5 and the data bus D0-D7 are multiplexed.
An address strobe must be connected to the CLK pin.

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4.2 · Signal Summary

Table 2 is a summary of all the signals discussed in the previous paragraph.

Table 2 · Signal summary

Symbol	Signal name	I/O	Active
V_{CC}	Power input	Input	High
GND	Ground	Input	Low
CLK	Clock	Input	N/A
$\overline{CS}$	Chip Select	Input	Low
$\overline{DS}$	Data Strobe	Input	Low
R/$\overline{W}$	Read/Write	Input	Read - High, Write - Low
$\overline{DTACK}$	Data Transfer Acknowledge	Output	Low
A1-A5	Register Select Bus	Input	N/A
D0-D7	Data Bus	I/O	N/A
$\overline{RESET}$	Reset	Input	Low
$\overline{IRQ}$	Interrupt Request	Output	Low
$\overline{IACK}$	Interrupt Acknowledge	Input	Low
$\overline{IEI}$	Interrupt Enable In	Input	Low
$\overline{IEO}$	Interrupt Enable Out	Output	Low
I0-I7	General Purpose I/O - Interrupt Lines	I/O	N/A
XTAL1, XTAL2	Timer Clock	Input	High
TAI, TBI	Timer Inputs	Input	N/A
TAO, TBO, TCO, TDO	Timer Outputs	Output	N/A
SI	Serial Input	Input	N/A
SO	Serial Output	Output	N/A
RC	Receiver Clock	Input	N/A
TC	Transmitter Clock	Input	N/A
$\overline{RR}$	Receiver Ready	Output	Low
$\overline{TR}$	Transmitter Ready	Output	Low
MPX	MPX	Input	N/A

B · DETAILED SPECIFICATIONS

1 · SCOPE

This drawing describes the specific requirements for the multi function peripheral TS 68C901B-4, 5 and 8 MHz, in compliance either with MIL-STD-883 class B or CECC 90000.

2 · APPLICABLE DOCUMENTS

2.1 · MIL-STD-883

1) MIL-STD-883 : test methods and procedures for electronics
2) MIL-M-38510 : general specifications for microcircuits
3) DESC 5962-90864

3 - REQUIREMENTS

3.1 - General

The microcircuits are in accordance with the applicable document and as specified herein.

3.2 - Design and construction

3.2.1 - Terminal connections

Depending on the package, the terminal connections shall be is shown in figures 2.1 and 2.2 (§ A).

3.2.2 - Lead material and finish

Lead material and finish shall be any option of MIL-M-38535 except finish C (as described in § 3.5.6.1 of 38535).

3.2.3 - Package

The macrocircuits are packaged in a hermetically sealed ceramic package which is conform to case outlines of MIL-M-38510 appendix C (when defined) :

- 48 LEAD DIP Style D14
- SQ LCC 52 PINS Style C6
- 52 TERMINAL JCC
- CQFP 52
- PGA 68.

The precise case outlines are described at the end of the specification (chapter 9) and into MIL-M-38510.

3.3 - Electrical characteristics

3.3.1 - Absolute maximum ratings

Limiting conditions (ratings) defined below shall not be for inspection purposes. Some limiting conditions (ratings) may however be taken in other parts of this specification as detail conditions for an applicable test.

5

If limiting condition(s) is (are) got over during testing or using of the component, the device can be damaged, even destroyed. Anyhow, component characteristics can be disturbed and they are not guaranteed any more.

Table 3 - Absolute maximum ratings

Symbol	Parameter	Condition	Min	Max	Unit
V_{CC}	Supply voltage		−0.3	7.0	V
V_I	Input voltage		−0.3	7.0	V
V_O	Output voltage		NA	NA	V
V_{OZ}	Off state voltage		NA	NA	V
I_O	Output currents		NA	NA	mA
I_I	Input currents		NA	NA	mA
P_d	Power dissipation	T_{case} = −55°C		55	mW
		T_{case} = +125°C		55	mW
T_c	Operating temperature		−55	+125	°C
T_{stg}	Storage temperature		−55	+150	°C
T_j	Junction temperature			+170	°C
T_{lead}	Lead temperature	Max. 5 sec soldering		+270	°C

3.3.2 - Guaranteed characteristics - recommended conditions of use

3.3.2.1 - Guaranteed characteristics

The characteristics associated to a specified measurement in the detail specification shall only be for inspection purposes.

Such characteristic defined in this specification is guaranteed only under conditions and within the limits which are specified for the relevant measurement. Unless otherwise specified, this guarantee applies within all the recommended operating ranges specified in § 3.3.2.2. below.

3.3.2.2 - Recommended conditions of use

To the correct operation of the device, the conditions of use shall be within the ranges specified below (see also § 3.3.2.1. above).

These conditions shall not be for inspection purposes.

Some recommended values may, however, be taken in other parts of this specification as detail conditions for an applicable test.

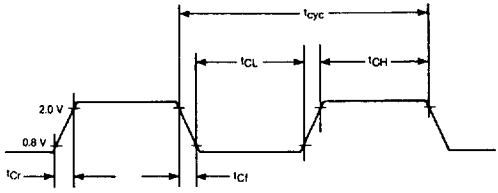


Figure 4 : Clock input timing diagram.

Table 4 - Recommended conditions of use

Unless otherwise stated, all voltages are referenced to the reference terminal (see § A.3).

Symbol	Parameter	Operating range			
		Model	Min	Max	Unit
V_{CC}	Supply voltage		4.5	5.5	V
V_{IL}	Low level input voltage (except XTAL1, XTAL2 and CLK : $V_{IL\ max}$ = 0.5 V)		−0.3	0.8	V
V_{IH}	High level input voltage		2.0	V_{CC}	V
T_{case}	Operating temperature		−55	+125	°C
R_L	Value of output load resistance		Note		Ω
C_L	Output loading capacitance			Note	pF
t_{cr}	Clock rise time (see Figure 4)			10	ns
t_{cf}	Clock fall time (see Figure 4)			10	ns
f_c	Clock frequency (see Figure 4)	TS 68C901B-4	1	4	MHz
		TS 68C901B-5	1	5	MHz
		TS 68C901B-8	1	8	MHz
t_{cyc}	Cycle time (see Figure 4)	TS 68C901B-4	250	1000	ns
		TS 68C901B-5	200	1000	ns
		TS 68C901B-8	125	1000	ns
$t_{w\,(cL)}$	Clock pulse width low (see Figure 4)	TS 68C901B-4	110		ns
		TS 68C901B-5	90		ns
		TS 68C901B-8	55		ns
$t_{w\,(cH)}$	Clock pulse width high (see Figure 4)	TS 68C901B-4	110		ns
		TS 68C901B-5	90		ns
		TS 68C901B-8	55		ns
V_{IL}	Low level input voltage for clock		−0.3	0.5	V

Note : Load network number 1 and 2 as specified in (Figures 5 and 6) gives the maximum loading of the relevant output.

3.3.3 · Special recommanded conditions for C.MOS devices

a) CMOS latch-up

The CMOS cell is basically composed of two complementary transistors (a P-channel and an N-channel), and, in the steady state, only one transistor is turned-on. The active P-channel transistor sources current when the output is a logic high and presents a high impedance when the output is a logic low. Thus the overall result is extremely low power consumption because there is no power loss through the active P-channel transistor. Also since only once transistor is determined by leakage currents.

Because the basic CMOS cell is composed of two complementary transistors, a virtual semiconductor controlled rectifier (SCR) may be formed when an input exceeds the supply voltage. The SCR that is formed by this high input causes the device to become «latched» in a mode that may result in excessive current drain and eventual destruction of the device. Although the device is implemented with input protection diodes, care should be exercised to ensure that the maximum input voltages specification is not exceeded from voltage transients ; others may require no additional circuitery.

b) CMOS applications

– The TS 68C901B completely satisfies the input/output drive requirements of CMOS logic devices.

– The HCMOS TS 68C901B, provides an order of magnitude power dissipation reduction when compared to the HMOS TS 68901. However the TS 68C901B does not offer a «power down» or «halt» mode. The minimum operating frequency of the TS 68C901B is 1 MHz.

3.4 · Thermal characteristics

Table 5

Package	Symbol	Parameter	Value	Unit
DIL 48	$\theta_{J\text{-}A}$	Thermal resistance Junction-to-Ambient	30	°C/W
	$\theta_{J\text{-}C}$	Thermal resistance Junction-to-Case	10	°C/W
LCCC 52	$\theta_{J\text{-}A}$	Thermal resistance Junction-to-Ambient	40	°C/W
	$\theta_{J\text{-}C}$	Thermal resistance Junction-to-Case	10	°C/W
LDCC 52	$\theta_{J\text{-}A}$	Thermal resistance Junction-to-Ambient	40	°C/W
	$\theta_{J\text{-}C}$	Thermal resistance Junction-to-Case	10	°C/W
CQFP 52	$\theta_{J\text{-}A}$	Thermal resistance Junction-to-Ambient	40	°C/W
	$\theta_{J\text{-}C}$	Thermal resistance Junction-to-Case	10	°C/W
PGA 68	$\theta_{J\text{-}A}$	Thermal resistance Junction-to-Ambient	5	°C/W
	$\theta_{J\text{-}C}$	Thermal resistance Junction-to-Case	33	°C/W

Power considerations : The average chip-junction temperature, T_J, in °C can be obtained from :

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

TA = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate reliationship between P_D and T_J (if $P_{I/O}$ is neglected) is :

$$P_D = K : (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives : $K = P_D \bullet (T_A + 273) + \theta_{JA} \bullet P_D^2$ (3)

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation :

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

3.5 · Mechanical and environment

The microcircuits shall meet all mechanical environmental requirements of MIL-STD-883 for class B devices.

3.6 · Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legible and permanently marked with the following information as minimum :

- Thomson logo
- Manufacturer's part number
- Class B identification
- Date-code of inspection lot
- ESD identifier if available
- Country of manufacturing

4 · QUALITY CONFORMANCE INSPECTION

4.1 · DESC / MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspection are performed on a periodical basis.

5 · ELECTRICAL CHARACTERISTICS

5.1 · General requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below :

- Table 6 : Static electrical characteristics for the electrical variants.
- Table 7 : Dynamic electrical characteristics for TS 68C901B-4 (4 MHz), TS 68C901B-5 (5 MHz) and TS 68C901B-8 (8 MHz).

For static characteristics (Table 6), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics (Table 7), test methods refer to clause 5.4 of this specification.

Indication of «min.» or «max.» in the column «test temperature» means minimum or maximum operating temperature as defined in sub-clause 3.3.2.2 here above.

Table 6 · Static characteristics for all covered models

$-55°C \leqslant T_c \leqslant +125°C$; $V_{CC} = 5.0\,V_{DC} \pm 10\,\%$; $GND = 0\,V_{DC}$

Test Nbr	Symbol	Characteristic	Method (*)	Test Conditions	Test Temp.	Limits Min	Limits Max	Unit
1	I_{CC}	Supply current outputs opens	41	$V_{CC} = 5.5\,V$	all		10	mA
2	V_{OL}	Low level output voltage (Except $\overline{DTACK}$/)	37	$V_{CC} = 4.5\,V$ $I_{OL} = 2.0\,mA$	all		0.5	V
3	V_{OH}	High level output voltage (Except $\overline{DTACK}$/)	37	$V_{CC} = 4.5\,V$ $I_{OH} = -120\,\mu A$	all	2.4		V
4	I_{OH}	$\overline{DTACK}$/ output source current		$V_{OUT} = 2.4\,V$	all		−400	µA
5	I_{OL}	$\overline{DTACK}$/ output sink current		$V_{OUT} = 0.5\,V$	all	5.3		mA
6	I_{IN}	Input leakage current (0 to 5.5 V)			all	−10	+10	µA
7	I_{LOH}	Three-state input current in float		$V_{OUT} = 2.4$ to V_{CC}	all		+10	µA
8	I_{LOL}	Three-state input current in float		$V_{OUT} = 0.5$	all		−10	µA
9	V_{IH1}	High level input voltage for all inputs (except : XTAL1, XTAL2, CLK)			all	2.0	V_{CC} +0.3	V
9A	V_{IH2}	High level input voltage for XTAL1, XTAL2, CLK			all	V_{CC} −1.5	V_{CC} +0.3	V
10	V_{IL1}	Low level input voltage for all inputs (except : XTAL1, XTAL2, CLK)			all	−0.3	0.8	V
10A	V_{IL2}	Low level input voltage for CLK, XTAL1, XTAL2			all	−0.3	0.5	V
97	C_{IN}	Input capacitance all inputs	11	Reverse voltage = 0 V F = 1.0 MHz	25°C		10	pF
					min		NA	pF
					max		NA	pF
98	C_{OUT}	Output capacitance all inputs	11	Reverse voltage = 0 V F = 1.0 MHz	25°C		10	pF
					min		NA	pF
					max		NA	pF
99	V_{ESD}	Internal protection Transient energy rating	See Note 7	See Note 7 5 cycles	25°C	−500	+500	V
					min	NA	NA	V
					max	NA	NA	V

* IEC measurement method number unless otherwise stated (see § 5.1).
Refered note is given after Table 7.

5

5.3 · Dynamic characteristics

Table 7 · Dynamic (switching) characteristics TS 68C901B-4, 5 and 8 MHz (see Figures 5 and 6)
$-55°C \leqslant T_C \leqslant +125°C$ or $-40°C \leqslant T_C \leqslant +85°C$; $V_{CC} = 5.0\ V_{DC} \pm 10\ \%$; $GND = 0\ V_{DC}$

Test Nbr	Symbol	Parameter	Fig. / Ref. (*)	Test Conditions	4 MHz Limits		5 MHz Limits		8 MHz Limits		Unit
					Min	Max	Min	Max	Min	Max	
11	t_w (T_{SWH})	$\overline{CS}$ $\overline{DS}$ width high (Note 5)	Fig. 8 - 9 Ref. 1	See 5.4 (a) to (c) f_C = 4 MHz	50		35		25		ns
12	t_{su} (T_{RASL})	R/$\overline{W}$, A1-A5 valid to falling $\overline{CS}$	Fig. 8 - 9 Ref. 2	See test 11	30		25		20		ns
13	t_{su} (T_{DVCL})	Data valid prior to $\overline{DS}$ high	Fig. 9 Ref. 3	See test 11	250		200		120		ns
14	t_{su} (T_{SVCL})	$\overline{CS}$, $\overline{IACK}$ valid prior to falling CLK (Note 3)	Fig. 8 - 10 - 11 Ref. 4	See test 11	50		50		50		ns
15	t_{phl} (T_{CLDL})	CLK low to $\overline{DTACK}$ low	Fig. 8 - 9 Ref. 5	See test 11 Load : 3		220		180		90	ns
16	t_{phl} (T_{SHDH})	$\overline{CS}$, $\overline{DS}$ or $\overline{IACK}$ high to $\overline{DTACK}$ high	Fig. 8 - 9 Ref. 6	See test 11 Load : 3		60		55		50	ns
18	t_h (T_{SLDIW})	$\overline{CSDS}$ or $\overline{IACK}$ high to data invalid (WRITE)	Fig. 9 Ref. 8	See test 11	0		0		0		ns
18A	t_h (T_{SLDIR})	$\overline{CSDS}$ or $\overline{IACK}$ high to data invalid (READ)	Fig. 8 Ref. 8A	See test 11	0		0		0		ns
20	t_h (T_{SHRAI})	$\overline{CS}$, $\overline{DS}$ or $\overline{IACK}$ high to R/$\overline{W}$ A1-A5 invalid	Fig. 8 - 10 - 11 Ref. 10	See test 11	0		0		0		ns
21	t_{phl} t_{plh} (T_{DVSL})	Data valid from $\overline{CS}$ low (Notes 3 and 5)	Fig. 8 - 9 Ref. 11	See test 11		310		260		180	ns
22	t_{su} (T_{RVDL})	Read data valid to $\overline{DTACK}$ low valid	Fig. 8 Ref. 12	See test 11 Load : 3	10		10		10		ns
23	t_h (T_{DLSH})	$\overline{DTACK}$ low to $\overline{DS}$, $\overline{CS}$ or $\overline{IACK}$ high	Fig. 8 - 10 Ref. 13	See test 11	10		10		10		ns
24	t_{su} (T_{ILCL})	$\overline{IEI}$ low to falling CLK	Fig. 10 - 11 Ref. 14	See test 11	50		50		50		ns
25	t_{phl} (T_{IVCL})	$\overline{IEO}$ valid from CLK low (Note 1)	Fig. 10 - 11 Ref. 15	See test 11		180		180		120	ns
26	t_{phl} t_{plh} (T_{DAVCL})	Data valid from CLK low	Fig. 10 Ref. 16	See test 11		300		300		180	ns
27	t_{plh} (T_{IIIH})	$\overline{IEO}$ invalid from $\overline{IACK}$ high	Fig. 10 - 11 Ref. 17	See test 11		150		150		100	ns
28	t_{plh} (T_{DLCH})	$\overline{DTACK}$ low from CLK high	Fig. 10 - 11 Ref. 18	See test 11		180		165		100	ns
29	t_{phl} (T_{IVIL})	$\overline{IEO}$ valid from $\overline{IEI}$ low (Note 1)	Fig. 11 Ref. 19	See test 11		100		100		100	ns
30	t_{phl} t_{plh} (T_{DAVIL})	Data valid from $\overline{IEI}$ low	Fig. 10 Ref. 20	See test 11		220		220		140	ns
31	t_{cy} (T_{CT})	CLK cycle time	Fig. 8 Ref. 21	See test 11	250		200		125		ns
32	t_w (T_{CU})	CLK width low	Fig. 8 Ref. 22	See test 11	110		90		55		ns
33	t_w (T_{CH})	CLK width high	Fig. 8 Ref. 23	See test 11	110		90		55		ns
34	t_{su} (T_{SICH})	$\overline{CS}$ $\overline{IACK}$ inactive to rising CLK (Note 4)	Fig. 8 - 11 Ref. 24	See test 11	100		80		50		ns
35	t_w (T_{IOAW})	I/O min active pulse width	Fig. 15 Ref. 25	See test 11	100		100		100		ns
36	t_w (T_{IWH})	$\overline{IACK}$ width high	Fig. 9 - 10 Ref. 26			2		2		2	TCLK
37	t_{phl} t_{plh} (T_{IDVSL})	I/O data valid from the first CLK ↓ following $\overline{CS}$ ↓ or $\overline{DS}$ ↓	Fig. 16 Ref. 27	See test 11		220		210		190	ns

* Measurement method : see § 5.4.

Refered notes are given after Table 7.

Table 7 · Dynamic (switching) characteristics TS 68C901B-4, 5 and 8 MHz (continued) (see Figures 5 and 6)
$-55°C \leq T_C \leq +125°C$ or $-40°C \leq T_C \leq +85°C$; $V_{CC} = 5.0\ V_{DC} \pm 10\ \%$; $GND = 0\ V_{DC}$

Test Nbr	Symbol	Parameter	Fig. / Ref. (*)	Test Conditions	4 MHz Limits		5 MHz Limits		8 MHz Limits		Unit
					Min	Max	Min	Max	Min	Max	
38	t_{phl} (T_{RRCL})	Receiver ready delay from rising RC	Fig. 17 Ref. 28	See test 11		600		600		200	ns
39	t_{phl} (T_{TRCL})	Transmitter ready delay from rising RC	Fig. 18 Ref. 29	See test 11		600		600		200	ns
40	t_{phl} (T_{TLSH})	Timer output low from rising edge of CS/ DS/ (Note 7)	Fig. 19 Ref. 30	See test 11		450		450		200	ns
42	t_w (T_{TCL})	Timer CLK low time	Fig. 19 Ref. 32	See test 11	110		90		55		ns
43	t_w (T_{TCH})	Timer CLK high time	Fig. 19 Ref. 33	See test 11	110		90		55		ns
44	t_w (T_{TCC})	Timer CLK cycle time	Fig. 19 Ref. 34	See test 11	250	1000	200	1000	125	1000	ns
45	t_w (T_{RL})	RESET/ low time	Fig. 20 Ref. 35	See test 11	2.0		1.6		1.0		µs
46	t_{phl} (T_{DILI})	Delay to falling IRQ from external interrupt active transition	Fig. 15 Ref. 36	See test 11		380		380		250	ns
47	t_{phl} (T_{TTCL})	Transmitter interrupt delay falling TC	Fig. 18 Ref. 37	See test 11		550		550		300	ns
47a	t_{phl} (T_{TTCH})	Transmitter underrun error or end of break interrupt delay from rising edge of TC	Fig. 18 Ref. 37a	See test 11		550		550		300	ns
48	t_{phl} (T_{RICL})	Receiver buffer full inter trans delay FR rising RC	Fig. 17 Ref. 38	See test 11		800		800		400	ns
49	t_{plh} (T_{RIRCL})	Receive error interrupt trans delay FR falling edge of RC	Fig. 17 Ref. 39	See test 11		800		800		800	ns
50	t_{plh} (T_{SRCL})	Serial in set-up time of rising edge of RC (divide by one only	Fig. 17 Ref. 40	See test 11	80		70		50		ns
51	t_h (T_{DHRL})	Data hold time FR rising edge of RC (divide by one only)	Fig. 17 Ref. 41	See test 11	350		325		100		ns
52	t_{plh} t_{phl} (T_{DTCL})	Serial output data valid FR falling edge of TC/(1)	Fig. 18 Ref. 42	See test 11		440		420		200	ns
53	t_w (T_{TACL})	Transmitter CLK low time	Fig. 18 Ref. 43	See test 11	500		450		250		ns
54	t_w (T_{TACH})	Transmitter CLK high time	Fig. 18 Ref. 44	See test 11	500		450		250		ns
55	t_w (T_{TACC})	Transmitter CLK cycle time	Fig. 18 Ref. 45	See test 11	1000		900		500		ns
56	t_w (T_{RCL})	Receiver CLK low time	Fig. 17 Ref. 46	See test 11	500		450		250		ns
57	t_w (T_{RCH})	Receiver CLK high time	Fig. 17 Ref. 47	See test 11	500		450		250		ns
58	t_{cy} (T_{RCC})	Receiver CLK cycle time	Fig. 17 Ref. 48	See test 11	1000		900		500		ns
59	t_w (T_{SWL})	CS/IACK/DS/ width low (Note 2)	Fig. 19 Ref. 49	See test 11		80		80		80	TCLK
60	t_{plh} t_{phl} (T_{DATCL})	Serial output data valid from falling edge TC (+ 16)	Fig. 18 Ref. 50	See test 11		490		370		240	ns
61	t_{cy} (T_{CY})	Cycle time	Fig. 12 Ref. 51	See test 11	1000		1000		1000		ns
62	t_w (T_{WEH})	Pulse width, E high	Fig. 12 Ref. 52	See test 11	430		430		430		ns
63	t_w (T_{WEL})	Pulse width, E low	Fig. 12 Ref. 53	See test 11	450		450		450		ns

* Measurement method : see § 5.4.
Refered notes are given after Table 7.

Table 7 - Dynamic (switching) characteristics TS 68C901B-4, 5 and 8 MHz (continued) (see Figures 5 and 6)
$-55°C \leq T_C \leq +125°C$ or $-40°C \leq T_C \leq +85°C$; $V_{CC} = 5.0\,V_{DC} \pm 10\,\%$; $GND = 0\,V_{DC}$

Test Nbr	Symbol	Parameter	Fig. / Ref. (*)	Test Conditions	4 MHz Limits		5 MHz Limits		8 MHz Limits		Unit
					Min	Max	Min	Max	Min	Max	
64	t_{su} (T_{AEH})	Address R/W/Setup time before E	Fig. 12 Ref. 54	See test 11	80		80		80		ns
65	t_{su} (T_{SEH})	$\overline{CS}$/Setup time before E	Fig. 12 Ref. 55	See test 11	80		80		80		ns
66	t_h (T_{HA})	Address hold time	Fig. 12 Ref. 56	See test 11	10		10		10		ns
67	t_h (T_{HS})	$\overline{CS}$/Hold time	Fig. 12 Ref. 57	See test 11	10		10		10		ns
68	t_{plh} (T_{EDV})	Output data delay (READ)	Fig. 12 Ref. 58	See test 11		250		250		250	ns
69	t_h (T_{HD})	Data hold time	Fig. 12 Ref. 59	See test 11	0	100	0	100	0	100	ns
70	t_{su} (T_{DEL})	Input data setup time (WRITE)	Fig. 12 Ref. 60	See test 11	280		280		280		ns
71	t_h (T_{HDW})	Data hold time (WRITE)	Fig. 12 Ref. 61	See test 11	20		20		20		ns
72	t_{cy} (T_{CY})	Cycle time	Fig. 13 - 14 Ref. 62	See test 11	800		800		800		ns
73	t_w (T_{SWH})	Pulse width $\overline{DS}$/ low or RD/WR/High	Fig. 13 - 14 Ref. 63	See test 11	350		350		350		ns
74	t_w (T_{SWL})	Pulse width $\overline{DS}$/ low or RD/WR/low	Fig. 13 - 14 Ref. 64	See test 11	340		340		340		ns
75	t_w (T_{ALEH})	Pulse width AS/ALE high	Fig. 13 - 14 Ref. 65	See test 11	100		100		100		ns
76	t_{phl} (T_{SLSL})	Delay as fall to $\overline{DS}$/ rise or Ale fall to RD/WR/Fall	Fig. 13 - 14 Ref. 66	See test 11	30		30		30		ns
77	t_{plh} (T_{SHSH})	Delay $\overline{DS}$/ or RD/WR/ rise to AS/ALE	Fig. 13 - 14 Ref. 67	See test 11	30		30		30		ns
78	t_{su} (T_{RLSH})	R/$\overline{W}$/Setup time $\overline{DS}$/	Fig. 13 - 14 Ref. 68	See test 11	100		100		100		ns
79	t_h (T_{RHSL})	R/$\overline{W}$/Hold time to $\overline{DS}$/	Fig. 13 - 14 Ref. 69	See test 11	10		10		10		ns
80	t_{su} (T_{ASL})	Address setup time to AS/ALE	Fig. 13 - 14 Ref. 70	See test 11	20		20		20		ns
81	t_h (T_{SLAV})	Address setup to AS/ALE	Fig. 13 - 14 Ref. 71	See test 11	20		20		20		ns
82	t_{su} (T_{DVSL})	Data setup time to $\overline{DS}$/ or or WR (WRITE)	Fig. 13 - 14 Ref. 72	See test 11	280		280		280		ns
83	t_{plh} (T_{SHDV})	Delay data to $\overline{DS}$/ or RD (Read)	Fig. 13 - 14 Ref. 73	See test 11		250		250		250	ns
84	t_h (T_{SLDV})	Data hold time to $\overline{DS}$ or WR (Write)	Fig. 13 - 14 Ref. 74	See test 11	20		20		20		ns
85	t_h (T_{SLDZ})	Data hold time to $\overline{DS}$ or RD (Read)	Fig. 13 - 14 Ref. 75	See test 11	0	100	0	100	0	100	ns
86	t_{su} (T_{RSH})	CE setup time to as/Ale Fallll	Fig. 13 - 14 Ref. 76	See test 11	20		20		20		ns
87	t_h (T_{SLCEH})	CE hold time to $\overline{DS}$ RD or WR	Fig. 13 - 14 Ref. 77	See test 11	20		20		20		ns

* Measurement method : see § 5.4.
Refered notes are given after Table 7.

REFERED NOTES TO THE TABLES

The following notes shall apply where referred into the tables and/or additional information given in of this specification.

Note 1 : IEO only goes low if no acknwoledgeable interrupt is pending. If $\overline{IEO}$ goes low, $\overline{DTACK}$ and the data bus remain tri-stated.

Note 2 : T_{CLK} refers to the clock applied to the MFP CLK input pin. t_{CLK} refers to the timer clock signal, regard less of whether this signal comes from the XTAL1/XTAL2 crystal clock inputs or the TAI or TBI timer inputs.

Note 3 : If the set-up time is not met, $\overline{CS}$ or $\overline{IACK}$ will not be recognized until the next falling CLK.

Note 4 : If the set-up time is met (for consecutive cycles), the minimum hold-off time of one clock cycle will be obtained. If not met, the hold-off will be two clock cycles.

Note 5 : Although $\overline{CS}$ and $\overline{DTACK}$ are synchronized with the clock, the data out during a read cycle is asynchronous to the clock, relying only on CS for timing.

Note 6 : Spec. 30 applies to timer outputs TAO and TBO only.

Note 7 : The test shall be performed as specified in Generic Specification and its associated documents. The test voltages are as given in Table 6 for test 99.
Each terminal of the device under test shall be tested separately against all existing V_{CC} and V_{SS} terminals of the device which shall be shorted together for the test. The other untested terminals shall be unconnected during the test. One cycle consists of the application of the both limits as given in Table 6 for test 99.

5.4 - Test conditions specific to the device

5.4.1 - Loading network

The applicable loading network shall be as defined in column «Test conditions» of Table 7, refering to the loading network number as shown in Figures 5 and 6 below.

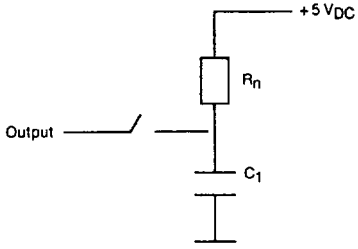


Figure 5 : Passive loads.

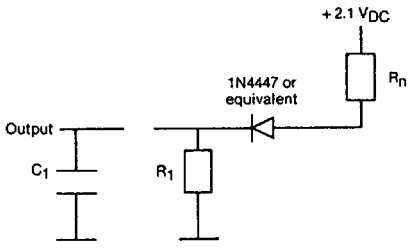
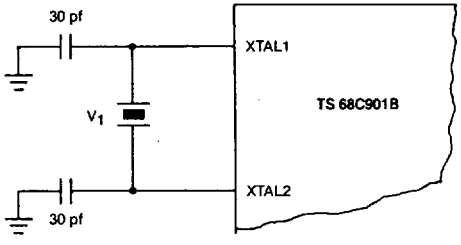


Figure 6 : Active loads.

Load NBR	Figure	R_1	R_n	C_1	Output application
1	5	—	2.25 k	100 pF	$\overline{IRQ}$
2	6	20 k	150	100 pF	All outputs except $\overline{DTACK}$
3	6	6 k	470	130 pF	$\overline{DTACK}$
Note : Equivalent loading may be simulated by the tester.					



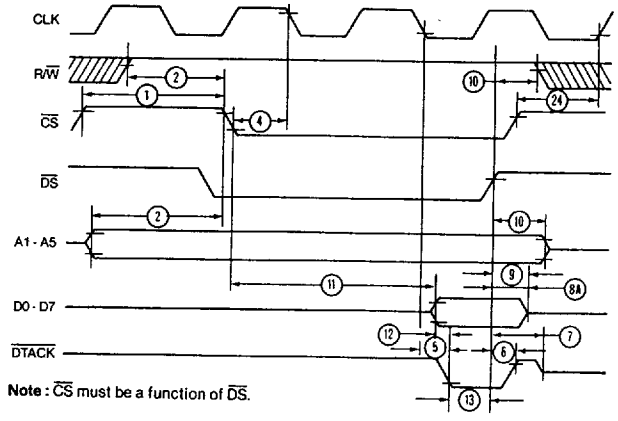
Crystal Parameters :

Parallel resonance, fundamental mode AT cut
R_L = < 150 Ω (Fr = 2.8 – 8.0 MHz) ;
R_L = < 300 Ω (Fr = 2.0 – 2.7 MHz) ;
C_L = 18 pF ; C_M = 0.02 pF ; C_h = 5 pF ; L_M = 96 mH
F_R (type) = 2.4676 MHz

Figure 7 : TS 68C901B MFP external oscillator components.

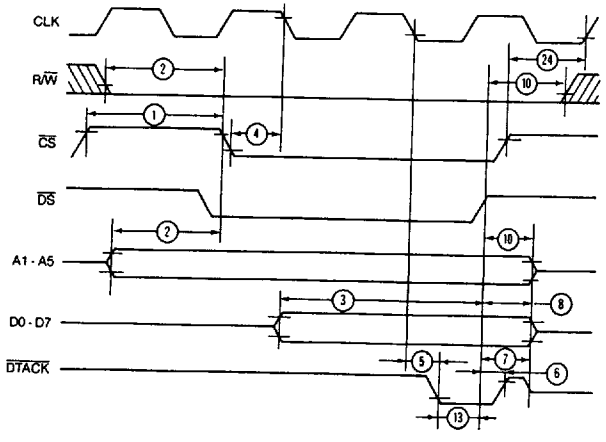
5.4.2 - Time definitions

The times specified in Table 7, as dynamic characteristics are defined in Figures 8 to 20 below by a reference number given in the column «Method» of the tables together with the relevant figure number.



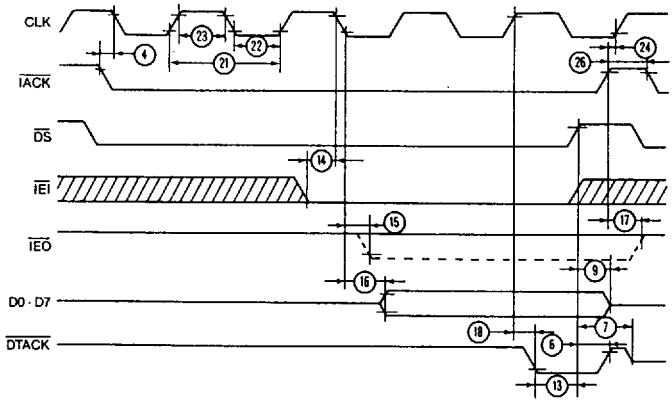
Note : $\overline{CS}$ must be a function of $\overline{DS}$.

Figure 8 : Read cycle timing.



Note : $\overline{CS}$ must be a function of $\overline{DS}$.

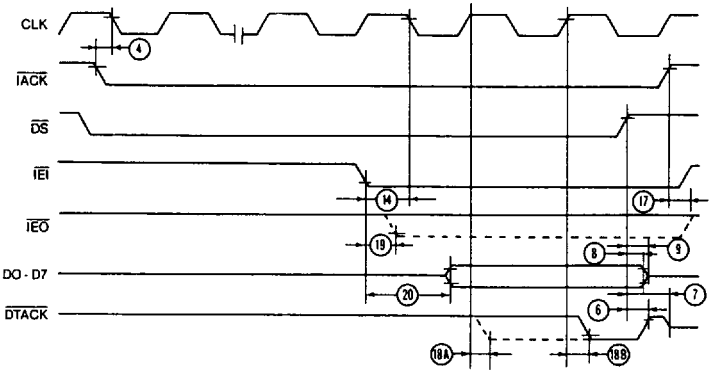
Figure 9 : Write cycle timing.



Note 1 : IEO only goes low if no acknowledgeable interrupt is pending. If IEO goes low, DTACK and the data bus remain in the high impedance state.

Note 2 : IACK must be a function of DS.

Figure 10 : Interrupt acknowledge cycle (IEI low).



Note 1 : IEO only goes low if no acknowledgeable interrupt is pending. If IEO goes low, DTACK and the data bus remain in the high impedance state.

Note 2 : DTACK will go low at A if specification number 14 is met. Otherwise DTACK will go low at 8.

Note 3 : IACK must be a function of DS.

Figure 11 : Interrupt acknowledge cycle (IEI high).

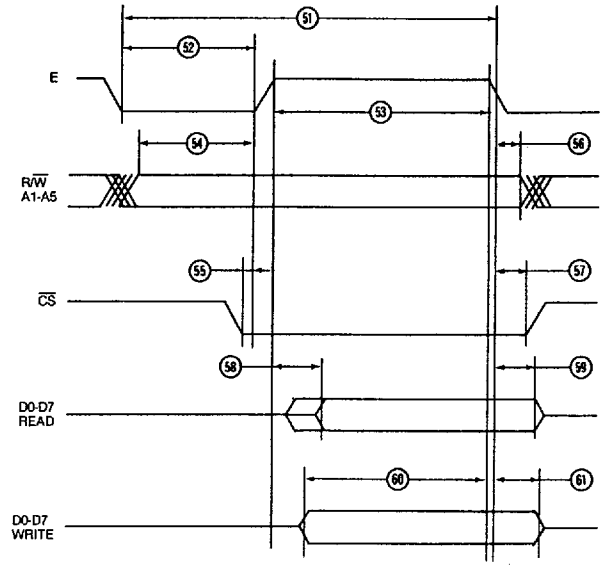


Figure 12 : 6800 interfacing timing.

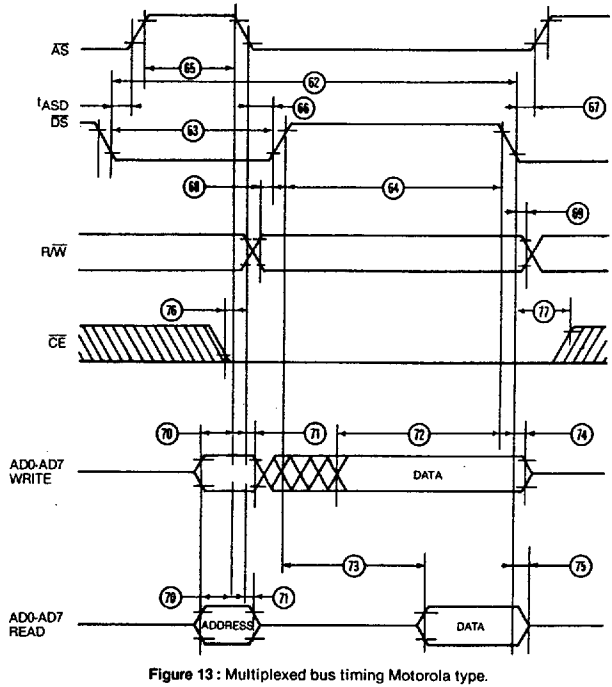


Figure 13 : Multiplexed bus timing Motorola type.

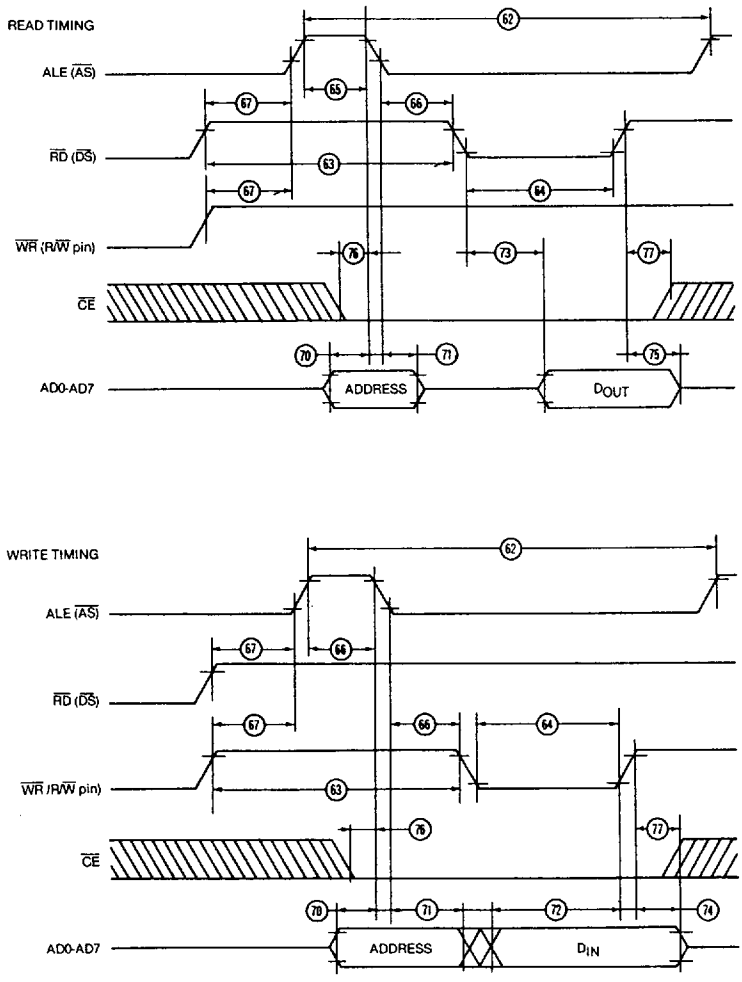
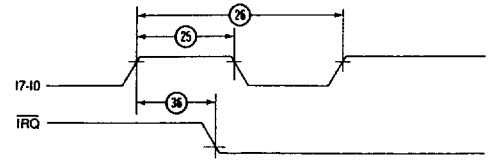


Figure 14 : Multiplexed bus timing - Intel type.



Note : Active edge is assumed to be the rising edge.

Figure 15 : Interrupt timing.

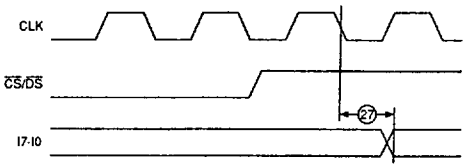


Figure 16 : Port timing.

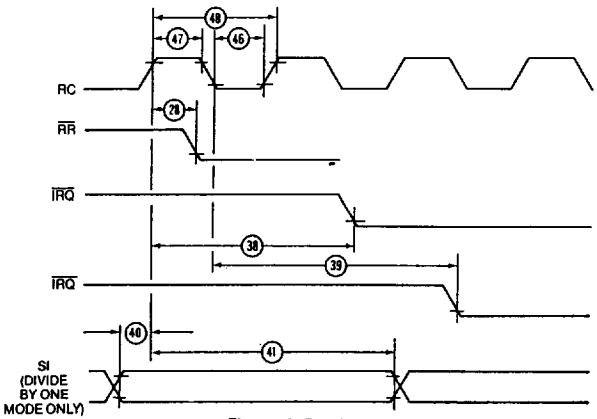


Figure 17 : Receiver timing.

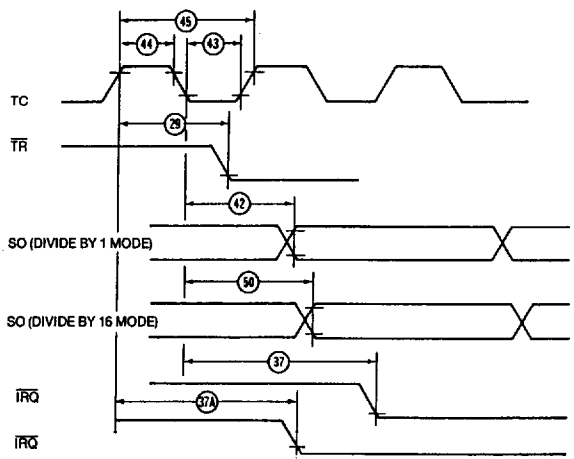


Figure 18 : Transmitter timing.

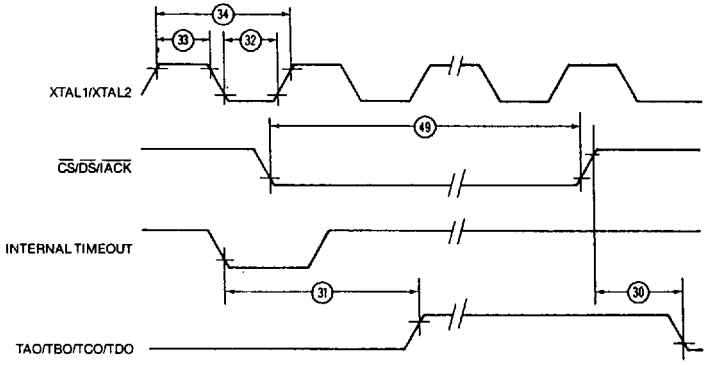


Figure 19 : Timer timing.

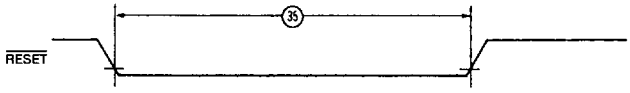


Figure 20 : Reset timing.

5

5.4.3 - Input and output signals for dynamic measurements

a) Input pulse characteristics
Where input pulse generator is loaded by 90 ohms resistor, the input pulse characteristics shall be as shown in Figure 21.

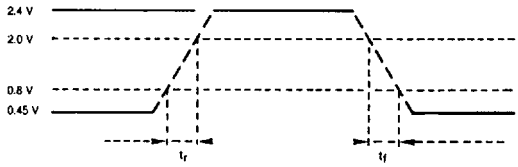


Figure 21 : Input pulse characteristics.

b) Time measurement input voltage references
Input voltages which are taken as reference for time measurement shall be :
V_{IL} = 0.8 V
V_{IH} = 2.0 V

c) Time measurement output voltage reference for time valid state output
Where output is (or becomes to) valid state, the output voltages which are taken as reference for time measurements shall be as shown in Figure 22.

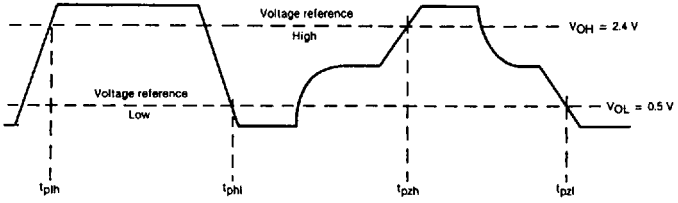


Figure 22 : Output voltage references for timing measurement.

5.4.4 · Timer AC characteristics

Definitions :

Error = Indicated time value - actual time value,
t_{psc} = t_{CLK}* Prescale value.

Internal Timer Mode :

Single Interval Error (Free Running) (See Note 2) ..... ± 100 ns
Cumulative Internal Error 0
Error Between Two Timer Reads ..... ± (t_{psc} − 4 t_{CLK})
Start Timer to Stop Timer Error ..... 2 t_{clk} + 100 ns to − (t_{psc} + 6 t_{CLK} + 100 ns)
Start Timer to Read Timer Error ..... 0 to − (t_{psc} + 6 t_{CLK} + 400 ns)
Start Timer to Interrupt Request Error (See Note 3) ..... 2 t_{CLK} to −(4 t_{CLK} + 800 ns)

Pulse Width Measurement Mode :

Measurement Accuracy (See Note 1) ..... 2 t_{CLK} to (t_{psc} + 4 t_{CLK})
Minimum Pulse Width ..... 4 t_{CLK}

Event Counter Mode :

Minimun Active Time of TAI and TBI ..... 4 t_{CLK}

Note 1 : Error may be cumulative if repetitively performed.
Note 2 : Error with respect to t_{out} or IRQ if Note 3 is true.
Note 3 : Assuming it is possible for the timer to make an interrupt request immediately.

5.5 · Additional information

Additional information shall not be for any inspection purposes.

5.5.1 · Additional electrical characteristics

The following additional characteristics, which are obtained from circuit design, are given for information only.

Unless otherwise stated, for dynamic additional characteristics, the given reference numbers refer to Figures 8 to 20 and loading number refer to Figures 5 and 7 (see § 5.4 of this specification).

The given limits should be valid for all operating temperature ranges as defined in § 3.3.2.2 of this specification.

Table 8 · Additional electrical characteristics TS 68C901B-4, 5 and 8 MHz (see Figures 5 and 6)
$-55°C \leq T_C \leq +125°C$; $V_{CC} = 5.0\,V_{DC} \pm 10\,\%$; $GND = 0\,V_{DC}$

Test Nbr	Symbol	Parameter	Fig. / Ref. (*)	Test Conditions	4 MHz Limits		5 MHz Limits		8 MHz Limits		Unit
					Min	Max	Min	Max	Min	Max	
17	t_{plz} (T_{SHDZ})	$\overline{CS}$/$\overline{DS}$/ or $\overline{IACK}$ high to $\overline{DTACK}$/ three state	Fig. 9 Ref. 7			100		100		100	ns
19	t_{phz} (T_{SHDAZ})	$\overline{CS}$/$\overline{DS}$/ or $\overline{IACK}$/ high to data three state	Fig. 8 - 10 - 11 Ref. 9			50		50		50	ns
31	t_{cy} (T_{CT})	CLK cycle time	Fig. 8 Ref. 21			1000		1000		1000	ns
41	t_{plh} (T_{VIT})	T_{out} valid from internal time-out (Note 2)	Fig. 19 Ref. 31			2 TCLK + 300		2 TCLK + 300		2 TCLK + 300	ns
44	t_{cy}	Timer CLK cycle time	Fig. 19 Ref. 34	See test 11		1000		1000		1000	ns
55	t_{cy} (T_{TACC})	Transmitter CLK cycle time	Fig. 18 Ref. 45			DC		DC		DC	
58	t_{cy} (T_{RCC})	Receiver CLK cycle time	Fig. 17 Ref. 48			DC		DC		DC	

* Measurement method : see § 5.4.
Refered notes are given after Table 7.

6 - FUNCTIONAL DESCRIPTION

6.1 - Bus operation

The following paragraphs explain the control signals and bus operation during data transfer operations and reset.

6.1.1 - Data transfer operations

Transfer of data between devices involves the following pins :

Register Select Bus – RS1 through RS5

Data Bus – D0 through D7

Control Signals

The address and data buses are separate parallel buses used to transfer data using an asynchronous bus structure. In all cycles, the bus master assumes responsibility for deskewing all signals it issues at both the start and end of a cycle. Additionally, the bus master is responsible for deskewing the acknowledge and data signals from the peripheral devices.

READ CYCLE. To read a CMFP register, $\overline{CS}$ and $\overline{DS}$ must be asserted, and R/$\overline{W}$ must be high. The CMFP will place the contents of the register which is selected by the register select bus (RS1 through RS5) on the data bus (D0 through D7) and then assert $\overline{DTACK}$. The register addresses are shown in Figure 27.

After the processor has latched the data, $\overline{DS}$ is negated. The negation of either $\overline{CS}$ or $\overline{DS}$ will terminate the read operation. The CMFP will drive $\overline{DTACK}$ high and place it in the high-impedance state. Also, the data bus will be in the high-impedance state. The timing for a read cycle is shown in Figure 23. Refer to for actual numbers.

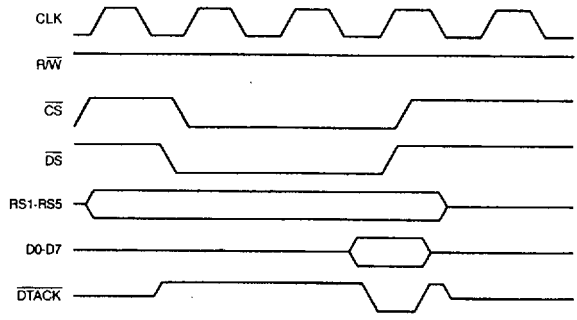


Figure 23 : Read cycle timing.

WRITE CYCLE. To write a register, $\overline{CS}$ and $\overline{DS}$ must be asserted, and R/$\overline{W}$ must be low. The CMPF will decode the address bus to determine which register is selected (the register map is shown in Figure 27). Then the register will be loaded with the contents of the data bus and $\overline{DTACK}$ will be asserted.

When the processor recognizes $\overline{DTACK}$, $\overline{DS}$ will be negated. The write cycle is terminated when either $\overline{CS}$ or $\overline{DS}$ is negated. The CMFP will drive $\overline{DTACK}$ high and place it in the high-impedance state. The timing for a write cycle is shown in Figure 24 Refer to for actual numbers.

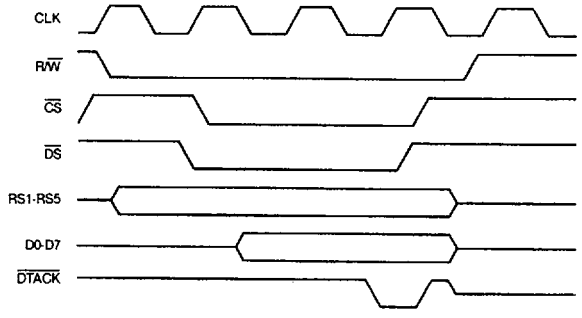


Figure 24 : Write cycle timing.

Interrupt acknowledge operation

The CMFP has 16 interrupt sources, eight internal sources, and eight external sources. When an interrupt request is pending, the CMFP will assert $\overline{IRQ}$. In a vectored interrupt sheme, the processor will acknowledge the interrupt request by performing an interrupt acknowledge cycle. $\overline{IACK}$ and $\overline{DS}$ will be asserted. The CMFP responds to the $\overline{IACK}$ signal by placing a vector number on the lower eight bits of the data bus. This vector number corresponds to the $\overline{IRQ}$ handler for the particular interrupt requesting service. The format of this vector number is given in Figure 28.

When the CMFP asserts $\overline{DTACK}$ to indicate that valid data is on the bus, the processor will latch the data and terminate the bus cycle by negating $\overline{DS}$. When either $\overline{DS}$ or $\overline{IACK}$ are negated, the CMFP will terminate the interrupt acknowledge operation by driving $\overline{DTACK}$ high and placing it in the high-impedance state. Also, the data bus will be placed in the high-impedance state. $\overline{IRQ}$ will be negated as a result of the $\overline{IACK}$ cycle unless additional interrupts are pending.

The CMFP can be part of a daisy-chain interrupt structure which allows multiple CMFPs to be placed at the same interrupt level by sharing a common $\overline{IACK}$ signal. A daisy-chain priority scheme is implemented with signals $\overline{IEI}$ and $\overline{IEO}$. IEI indicates that no higher priority device is requesting interrupt service. $\overline{IEO}$ signals lower priority devices that neither this device nor any higher priority device is requesting service.

To daisy-chain CMFPs, the highest priority CMFP has its IEI tied low and successive CMFPs have their $\overline{IEI}$ connected to the next higher priority device's $\overline{IEO}$. Note that when the daisy-chain interrupt structure is not implemented, the IEI of all CMFPs must be tied low. Refer to § 6.2.3 for additional information.

When the processor initiates an interrupt acknowledge cycle by driving $\overline{IACK}$ and $\overline{DS}$, the CMFP whose $\overline{IEI}$ is low may respond with a vector number if an interrupt is pending. If this device does not have a pending interrupt, $\overline{IEO}$ is asserted which allows the next lower priority device to respond to the interrupt acknowledge. When an CMFP propagates $\overline{IEO}$, it will not drive the data bus nor $\overline{DTACK}$ during the interrupt acknowledge cycle. The timing for an $\overline{IACK}$ cycle is shown in Figure 25. Refer to for further information.

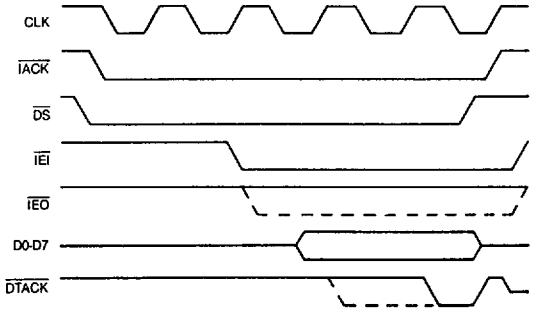


Figure 25 : IACK cycle timing.

Reset operation

The reset operation will initialize the CMFP to a known state. The reset operation requires that the $\overline{RESET}$ input be asserted for a minimum of two microseconds. During a device reset condition, all internal CMFP registers are cleared except fot the timer data registers (TADR, TBDR, TCDR, and TDDR), the USART data register (UDR), the transmitter status register (TSR) and the interrupt vector register. All timers are stopped and the USART receiver and transmitter are disabled. The interrupt channels are also disabled and any pending interrupts are cleared.

In addition, the general purpose interrupt I/O lines are placed in the high-impedance input mode and the timer outputs are driven low. External CMFP signals are negated. The interrupt vector register is initialized to a $0F.

Non multiplexed mode

In this mode the MPX input must be set to zero, and the TS 68C901B can be used with a 68000 processor type or a 6800 processor type. Refer to figure for the electrical characteristics.

With a 6800 processor type the $\overline{DS}$ pin is connected to the E signal of the processor, the $\overline{DTACK}$ signal is not used and the CLK must be zeroed.

Multiplexed mode

The CMFP can be used either on a MOTOROLA or INTEL bus type. In this case the MPX pin is connected to Vcc. The following table gives the signification of the different signals used. A dummy access to the TS 68C901B has to be done before any valid access in order to set up the internal logic of sampling.

LCCC pin out	DIL pin out	MOTOROLA 68000 type	MOTOROLA Multiplexed	INTEL
52	48	$\overline{CS}$	$\overline{CS}$	$\overline{CS}$
51	47	$\overline{DS}$	$\overline{DS}$	RD
2	1	R/$\overline{W}$	R/$\overline{W}$	WR
40	36	V_{SS}	AS	ALE

6.1.2 · DMA operation

USART error conditions are only valid for each character boundary. When the USART performs block data transfers by using the DMA handshake lines $\overline{RR}$ (Receiver Ready) and $\overline{TR}$ (Transmitter Ready), errors must be saved and checked at the end of a block. This is accomplished by enabling the error channel for channel for the receiver or transmitter and by masking interrupts for this channel. Once the transfer is complete, interrupt pending register A is read. Any pending receiver or transmitter error indicates an error in the data transfer.

6.2 · Interrupt structure

In a 68000 system, the CMFP will be assigned to one fo the seven possible interrupt levels. All interrupt service requests from the CMFP's 16 interrupt channels will be presented at this level. Although, as an interrupt controller, the CMFP will internally prioritize its 16 interrupt sources. Additional interrupt sources may be placed at the same interrupt level by daisy-chaining multiple CMFPs. The CMFPs will be prioritized by their position in the chain.

6.2.1 · Interrupt processing

Each CMFP provides individual interrupt capability for its various functions. When an interrupt is received on one of the external interrupt channels or from one of the eight internal sources, the CMFP will request interrupt service. The 16 interrupt channels are assigned a fixed priority so that multiple pending interrupts are serviced according to their relative importance. Since the CMFP can internally generate 16 vector numbers, the unique vector number which corresponds to the highest priority channel that has a pending interrupt is presented to the processor during an interrupt acknowledge cycle. This unique vector number allows the processor to immediately begin execution of the interrupt handler for the interrupting source, decreasing interrupt latency time.

5

Address						Abbreviation	Register name
Hex	Binary						
	RS5	RS4	RS3	RS2	RS1		
01	0	0	0	0	0	GPIP	General purpose I/O register
03	0	0	0	0	1	AER	Active edge register
05	0	0	0	1	0	DDR	Data direction register
07	0	0	0	1	1	IERA	Interrupt enable register A
09	0	0	1	0	0	IERB	Interrupt enable register B
0B	0	0	1	0	1	IPRA	Interrupt pending register A
0D	0	0	1	1	0	IPRB	Interrupt pending register B
0F	0	0	1	1	1	ISRA	Interrupt in-service register A
11	0	1	0	0	0	ISRB	Interrupt in-service register B
13	0	1	0	0	1	IMRA	Interrupt mask register A
15	0	1	0	1	0	IMRB	Interrupt mask register B
17	0	1	0	1	1	VR	Vector register
19	0	1	1	0	0	TACR	Timer A control register
1B	0	1	1	0	1	TBCR	Timer B control register
1D	0	1	1	1	0	TCDCR	Timers C and D control register
1F	0	1	1	1	1	TADR	Timer A data register
21	1	0	0	0	0	TBDR	Timer B data register
23	1	0	0	0	1	TCDR	Timer C data register
25	1	0	0	1	0	TDDR	Timer D data register
27	1	0	0	1	1	SCR	Synchronous character register
29	1	0	1	0	0	UCR	USART control register
2B	1	0	1	0	1	RSR	Receiver status register
2D	1	0	1	1	0	TSR	Transmitter status register
2F	1	0	1	1	1	UDR	USART data register

Note : Hex addresses assume that RS1 connects with A1, RS2 connects with A2, etc... and that DS is connected to LDS on the 68000 or DS is connected to DS on the 68008.

Figure 26 : Register MAP.

6.2.1.1 - Interrupt channel prioritization

The 16 interrupt channels are prioritized as shown in Figure 27 general purpose interrupt 7 (I7) is the highest priority interrupt channel and 10 is the lowest priority channel. Pending interrupts are presented to the CPU in order of priority unless they have been masked off. By selectively masking interrupts, the channels are in effect re-prioritized.

Priority	Channel	Description
Highest	1111	General purpose interrupt 7 (I7)
	1110	General purpose interrupt 6 (I6)
	1101	Timer A
	1100	Receiver buffer full
	1011	Receive error
	1010	Transmit buffer empty
	1001	Transmit error
	1000	Timer B
	0111	General purpose interrupt 5 (I5)
	0110	General purpose interrupt 4 (I4)
	0101	Timer C
	0100	Timer D
	0011	General purpose interrupt 3 (I3)
	0010	General purpose interrupt 2 (I2)
	0001	General purpose interrupt 1 (I1)
Lowest	0000	General purpose interrupt 0 (I0)

Figure 27 : Interrupt prioritization.

6.2.1.2 - Interrupt vector number format

During an interrupt acknowledge cycle, a unique 8-bit vector number is presented to the system which corresponds to the specific interrupt source which is requesting service. The format of the vector is shown in Figure 28. The most significant four bits of the interrupt vector number are user programmable. These bits are set by writing the upper four bits of the vector register which is shown in Figure 29. The low order bits are generated internally by the TS 68C901B. Note that the binary channel number shown in Figure 27 corresponds to the low order bits of the vector number associated with each channel.

7	6	5	4	3	2	1	0
V7	V6	V5	V4	IV3	IV2	IV1	IV0

V7-V4 : The four most significant bits are copied from the vector register.

IV3-IV0 : These bits are supplied by the CMFP. They are the binary channel number of the highest priority channel that is requesting interrupt service.

Figure 28 : Interrupt vector format.

	7	6	5	4	3	2	1	0
Address 17 (Hex)	V7	V6	V5	V4	S	★	★	★

★ Unused are read as zero.

V7-V4 : The upper four bits of the vector register are written by the user. These bits become the most significant four bits of the interrupt vector number.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset (VR must be written at least once by MPU, if not, low order bits remain 1111).

S : In-Service Register Enable. When the S bit is zero, the CMFP is in the automatic end-of-interrupt mode and the in-service register bits are forced low. When the S bit is a one, the CMFP is in the software end-of-interrupt mode and the in-service register bits are enabled. Refer to § 6.2.4.2 and § 6.2.4.3 for additionnal information.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

Figure 29 : Vector register format (VR).

6.2.2 · *Daisy-chaining CMFPs*

As an interrupt controller, the TS 68C901B CMFP will support eight external interrupt sources in addition to its eight internal interrupt sources. When a system requires more than eight external interrupt sources to be placed at the same interrupt level, sources may be added to the prioritized structure by daisy-chaining CMFPs. Interrupt sources are prioritized internally within each CMFP and the CMFPs are prioritized by their position in the chain. Unique vector numbers are provided for each interrupt source.

The $\overline{IEI}$ and $\overline{IEO}$ signals implement the daisy-chained interrupt structure. The $\overline{IEI}$ of the highest priority CMFP is tied low and the $\overline{IEO}$ output of this device is tied to the next highest priority CMFP's $\overline{IEI}$. The $\overline{IEI}$ and $\overline{IEO}$ signals are daisy-chained in this manner for all CMFPs in the chain, with the lowest priority CMFP's $\overline{IEO}$ left unconnected. A diagram of an interrupt daisy-chain is shown in Figure 30.

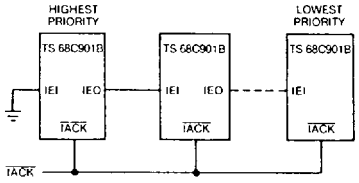


Figure 30 : Daisy-chained interrupt structure.

Daisy-chaining requires that all parts in the chain have a common $\overline{IACK}$. When the common $\overline{IACK}$ is asserted during an interrupt acknowledge cycle, all parts will prioritize interrupts in parallel. When the $\overline{IEI}$ signal to a CMFP is asserted, the part may respond to the $\overline{IACK}$ cycle if it requires interrupt service. Otherwise, the part will assert $\overline{IEO}$ to the next lower priority device. Thus, priority is passed down the chain via $\overline{IEI}$ and $\overline{IEO}$ until a part which has a pending interrupt is reached. The part with the pending interrupt passes a vector number to the processor and does not propagate $\overline{IEO}$.

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6.2.3 · *Interrupt control registers*

CMFP interrupt processing is managed by the interrupt enable registers A and B, interrupt pending registers A and B, and interrupt mask registers A and B. These registers allow the programmer to enable or disable individual interrupt channels, mask individual interrupt channels, and access pending interrupt status information. In-service registers A and B allow interrupts to be nested as described in. The interrupt control registers are shown in figure.

6.2.3.1 · *Interrupt enable registers*

The interrupt channels are individually enabled or disabled by writing a one or zero, respectively, to the appropriate bit of interrupt enable register A (IERA) or interrupt enable register B (IERB). The processor may read theses registers at any time.

When a channel is enabled, interrupts received on the channel will be recognized by the CMFP and $\overline{IRQ}$ will be asserted to the processor, indicating that interrupt service is required. On the other hand, a disabled channel is completely inactive ; interrupts received on the channel are ignored by the CMFP.

Writing a zero to a bit of interrupt enable register A or B will cause the corresponding bit of interrupt pending register A or B to cleared. This will terminate all interrupt service request for the channel and also negate $\overline{IRQ}$, unless interrupts are pending from other sources. Disabling a channel, however, does not affect the corresponding bit in interrupt in-service registers A or B. So, if the CMFP is in the software end-of-interrupt mode (see) and an interrupt is in service when a channel is disabled, the in-service status bit for that channel will remain set until cleared by software.

(a) Interrupt Enable Registers (IERA and IERB)

	7	6	5	4	3	2	1	0
Address 07 (Hex)	GPIP7	GPIP6	Timer A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	Timer B
Address 09 (Hex)	GPIP5	GPIP4	Timer C	Timer D	GPIP3	GPIP2	GPIP1	GPIP0

When a bit is zero the associated interrupt channel is disabled. When a bit is a one the associated interrupt channel is enabled.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

(b) Interrupt Pending Registers (IPRA and IPRB)

	7	6	5	4	3	2	1	0
Address 0B (Hex)	GPIP7	GPIP6	Timer A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	Timer B
Address 0D (Hex)	GPIP5	GPIP4	Timer C	Timer D	GPIP3	GPIP2	GPIP1	GPIP0

When a bit is a zero, no interrupt is pending on the associated interrupt channel. When a bit is a one, an interrupt is pending on the associated interrupt channel.
SET a) Interrupt is received on an enabled interrupt channel.
CLEARED a) Interrupt vector for the associated interrupt channel is passed during an $\overline{IACK}$ cycle.
b) Associated interrupt channel is disabled.
c) MPU writes a zero.
d) Reset.

(c) Interrupt In-Service Registers (ISRA and ISRB)

	7	6	5	4	3	2	1	0
Address 0F (Hex)	GPIP7	GPIP6	Timer A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	Timer B
Address 11 (Hex)	GPIP5	GPIP4	Timer C	Timer D	GPIP3	GPIP2	GPIP1	GPIP0

When a bit is a zero, no interrupt processing is in progress for the associated interrupt channel. When a bit is a one, interrupt processing is in progress for the associated interrupt channel.
SET a) Interrupt vector number for the associated, interrupt channel is passed during an $\overline{IACK}$ cycle and the S bit of the vector register is set.
CLEARED a) Interrupt service is completed for the associated interrupt channel.
b) The S bit of the vector register is a zero.
c) MPU writes a zero.
d) Reset.

(d) Interrupt Mask Registers (IMRA and IMRB)

	7	6	5	4	3	2	1	0
Address 13 (Hex)	GPIP7	GPIP6	Timer A	RCV Buffer Full	RCV Error	XMIT Buffer Empty	XMIT Error	Timer B
Address 15 (Hex)	GPIP5	GPIP4	Timer C	Timer D	GPIP3	GPIP2	GPIP1	GPIP0

When a bit is a zero, interrupts are masked for the associated interrupt channel. When a bit a one, interrupts are not masked for the associated interrupt channel.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

Figure 31 : Interrupt control registers.

6.2.3.2 - Interrupt pending registers

When an interrupt is received on an enabled, the corresponding interrupt pending bit is set in interrupt pending register A or B (IPRA or IPRB). In a vectored interrupt scheme, this bit will be cleared when the processor acknowledges the interrupting channel and the CMFP responds with a vector number. In a polled interrupt system, the interrupt pending registers must be read to determine the interrupting channel and then the interrupt pending bit is cleared by the interrupt handling routine without performing an interrupt acknowledge sequence.

A single bit of the interrupt pending registers is cleared in software by writing ones to all bit positions except the bit to be cleared. This allows any one bit to be cleared, without altering any other bits, simply by writing all ones except for the bit position to be cleared to IPRA or IPRB. Thus a fully polled interrupt scheme is possible. Note that writing ones to IPRA and IPRB has no effect on the contents of the register. A single bit of the interrupt pending registers is also cleared when the corresponding channel is disabled by writing a zero to the appropriate bit of IERA or IERB.

6.2.3.3 - Interrupt mask registers

Interrupts are masked for a channel by clearing the appropriate bit in interrupt mask register A or B (IMRA or IMRB). Even though an enabled channel is masked, the channel will recognize subsequent interrupts and set its interrupt pending bit. Howevern, the channel is prevented from requesting interrupt service (IRQ to the processor) as long as the mask bit for that channel is cleared.

If a channel is requesting interrupt service at the time that its corresponding bit in IMRA or IMRB is cleared, the request will cease and IRQ will be negated, unless another channel is requesting interrupt service. Later, when the mask bit is set, any pending interrupt on the channel will be processed according to the channel's assigned priority. IMRA and IMRB may be read at any time.

6.2.4 - Nesting CMFP interrupts

In a 68000 vectored interrupt system, the CMFP is assigned to one of seven possible interrupt levels. When an interrupt is received from the CMFP, an interrupt acknowledge for that level is initiated. Once an interrupt is recognized at a particular level, interrupts at that same level or below are masked by 68000. As long as the processor's interrupt mask is unchanged, the 68000 interrupt structure will prohibit the nesting of interrupts at the same interrupt level. However, additional interrupt requests from the CMFP can be recognized before a previous channel's interrupt level within the interrupt handler.

5

When nesting CMFP interrupts it may be desirable to permit interrupts on any CMFP channel, regardless of its priority, to preempt or delay interrupt processing of an earlier channel's interrupt service request. Or, it may be desirable to only allow subsequent higher priority interrupt requests. The CMFP interrupt structure provides this flexibility by offerinG two end-of-interrupt options for vectored interrupt schemes. Note that the end-of-interrupt modes are not active in a polled interrupt schema.

6.2.4.1 - Selecting the end-of-interrupt mode

In a vectored interrupt scheme, the CMFP may be programmed to operate in either the automatic end-of-interrupt mode of the software end-of-interrupt mode. The mode is selected by writing the S bit of the vector register (see Figure 29).

When the S bit is programmed to a one, the CMFP is placed in the software end-of-structure mode and when the S bit is a zero, all channels operate in the automatic end-of-interrupt mode.

6.2.4.2 - Automatic end-of-interrupt

When an interrupt vector number is passed to the processor during an interrupt acknowledge cycle, the corresponding channel's interrupt pending bit is cleared. In the automatic end-of-interrupt mode, no further history of the interrupt remains in the CMPF. The in-service bits of the interrupt in-service registers (ISRA and ISRB) are force low. Subsequent interrupts which are received on any CMFP channel will generate an interrupt request to the processor, even if the current interrupt's service routine has not been completed.

6.2.4.3 - Software end-of-interrupt

In the software end-of-interrupt mode, the channel's associated interrupt pending bit is cleared and in addition, the channel's in-service bit of in-service register A or B is set when its vector number is passed to the processor during an IACK cycle. A higher priority channel may subsequently request interrupt service and be acknowledged, but as long as the channel's in-service bit is set, no lower priority channel may request interrupt service nor pass its vector during an interrupt acknowledge sequence.

While only higher priority channels may request interrupt service, any channel can receive an interrupt and set its interrupt pending bit. Even the channel whose in-service bit is set can receive a second interrupt. However, no interrupt service request is made until its in-service bit is cleared.

The in-service bit for a particular channel can be cleared by writing a zero to its corresponding bit in ISRA or ISRB and ones to all other bit positions. Since bits in the in-service registers can only be cleared in software and not set, writing ones to the registers does not alter their contents. ISRA and ISRB may be read at any time.

6.3 - General purpose input/output interrupt port

The general purpose interrupt input/output (I/O) port (GPIP) provides eight I/O lines (10 through 17) that may be oprerated as either inputs or outputs under software control. In addition, these lines may optionally generate an interrupt on either a positive transition or a negative transition of the input signal. The flexibility of the GPIP allows it to be configured as an 8-bit I/C port or for bit I/O. Since interrupts are enabled on an bit-by-bit basis, a subset of the GPIP could be programmed as handshake lines or the port could be connected to as many as eight external interrupt sources, which would be prioritized by the CMFP interrupt controller for interrupt service.

6.3.1 - 6800 interrupt controller

The CMFP interrupt controller is particularly useful in a system which has many 6800-type devices. Typically, in a vectored 68000 system, 6800-type peripherals use the autovector which corresponds to their assigned interrupt level since they do not provide a vector number in response to an IACK cycle. The autovector interrupt handler must then poll all 6800-type devices at that interrupt level to determine which device is requesting service. However, by tying the IRQ output from a 6800-type device to the general purpose I/O interrupt port (GPIP) of a CMFP, a unique vector number will be provided to the processor during an interrupt acknowledge cycle. This interrupt structure will significantly reduce interrupt latency for 6800-type devices and other peripheral devices which do not support vector-by-device.

6.3.2 - GPIP control registers

The GPIP is programmed via three control registers shown in Figure 32. These registers control the data direction, provide user access to the port and specify the active edge for each bit of the GPIP which will produce an interrupt. These registers are described in detail in the following paragraphs.

6.3.2.1 - GPIP data register

The general purpose I/O data register is used to input or output data to the port. When data is written to the GPIP data register, those pins which are defined as inputs will remain in the high-impedance state. Pins which are defined as outputs will assume the state (high or low) of their corresponding bit in the data register. When the GPIP is read, data will be passed directly from the bits of the data register for pins which are defined as outputs. Data from pins defined as inputs will come from the input buffers.

6.3.2.2 - Active edge register

The active edge register (AER) allows each of the GPIP lines to produce an interrupt on either a one-to-zero or a zero-to-one transition. Writing a zero to the appropriate edge bit of the active edge register causes the associated input to generate an interrupt on the one-to-zero transition of the corresponding GPIP line.

(a) GPIP Data Register (GPIP)

	7	6	5	4	3	2	1	0
Address 01 (Hex)	GPIP7	GPIP6	GPIP5	GPIP4	GPIP3	GPIP2	GPIP1	GPIP0

SET a) MPU writes a one.
CLEARED a) MPU writes a zero.

(b) Active Edge Register (AER)

	7	6	5	4	3	2	1	0
Address 03 (Hex)	GPIP7	GPIP6	GPIP5	GPIP4	GPIP3	GPIP2	GPIP1	GPIP0

When a bit is a zero, interrupts will be generated on the falling edge of the associated input signal. When a bit is a one, interrupts will be generated on the rising edge of the associated input signal.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

(c) Data Direction Register (DDR)

	7	6	5	4	3	2	1	0
Address 05 (Hex)	GPIP7	GPIP6	GPIP5	GPIP4	GPIP3	GPIP2	GPIP1	GPIP0

When a bit is a zero, the associated I/O line is defined to be an input. When a bit is a one, the associated I/O line is defined to be an output.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

Figure 32 : GPIP control registers.

Note : The transition detector is an exclusive-OR gate whose inputs are the edge bit and the input buffer. As a result, writing the AER may cause an interrupt-producing transition, depending upon the state of the input. So, the AER should be configured before enabling interrupts via the interrupt enable registers (IERA and IERB). Also, changing the edge bit while interrupts are enabled may cause an interrupt on the corresponding channel.

6.3.2.3 - Data direction register

The data direction register (DDR) allows the programmer to define 10 through 17 as inputs or outputs by writing the corresponding bit. When a bit of the data direction register is written as a zero, the corresponding interrupt I/O pin will be a high-impedance input. Writing a one to any bit of the data direction register will cause the corresponding pin to be configured as a push-pull output.

6.4 - Timers

The CMFP contains four 8-bit timers which provide many functions typically required in microprecessor systems. The timers can supply the baud rate clocks for the on-chip serial I/O channel, generate periodic interrupts, measure elapsed time, and count signal transitions. In addition, two timers have waveform generation capability.

All timers are prescaler/counter timers with a common independent clock input (XTAL1 or XTAL2) and are not required to be operated from the system clock. Each timer's output signal toggles when the timer's main counter times out. Additionally, timers A and B have auxiliary control signals which are used in two of the operation modes. An interrupt channel is assigned to each timer and when the auxiliary control signals are used, a separate interrupt channel will respond to transitions on these inputs.

6.4.1 - Operation modes

Timers A and B are full function timers which, in addition to the delay mode, operate in the pulse width measurement mode and the event count mode. Timers C and D are delay timers only. A brief discussion of each of the timer modes follows.

6.4.1.1 - Delay mode operation

All timers may operate in the delay mode. In this mode the prescaler is always active. The prescaler specifies the number of timer clock cycles which must elpase before a count pulse is applied to the main counter. A count pulse causes the main counter to decrement by one. When the timer has decremented down to 01 (hexadecimal), the next count pulse will cause the main counter to be reloated from the timer's interrupt channel time out pulse also causes the timer output pin to toggle. The output will remain in this new state until the next time out pulse occurs.

For example, if delay mode with a divide-by-10 prescaler is selected and the timer data register is loaded with 100 (decimal), the main counter will decrement once every 10 timer clock cycles. After 1,000 timer clocks, a time out pulse will be produced. This time out pulse will generate an interrupt if the channel is enabled (IERA, IERB) and in addition the timer's output line will toggle. The output line will complete one full periode every 2,000 cycles of the timer clock.

The main counter is an 8-bit binary down counter. It may be read at any time by reading the Timer Data Register. The information read is the information last clocked into the timer read register when the $\overline{DS}$ pin had last gone high prior to the current read cycle. When written, data is loaded into the Timer Data Register, and the main counter, if the timer is stopped. If the Timer Data Register is written while the timer is running, the new word is not loaded into the timer until it counyer through H«01». Howerver, if the timer is written while it is counting through H«01», an indeterminate value will be written into the timer constant register. This may be circumvented by ensuring that the data register is not written when the count is H«01».

If the prescaler value is changed while the timer is enabled, the first time out pulse will occur at an indeterminate time no less than one nor more than 200 timer clock cycles. Subsequent time out pulses will then occur at the correct interval.

If the main counter is loaded with 01 (hexadecimal), a time out pulse will occur every time the prescaler presents a count pulse to the main counter. If the main counter is loaded with 00, a time out pulse will occur every 256 count pulses.

6.4.1.2 - Pulse width measurement operation

Besides the delay mode, timers A and B may be programmed to operate in the pulse width measurement mode. In this mode an auxiliary control input is required ; timers A and B auxiliary input are TAI and TBI. Also, in the pulse width measurement mode, interrupt channels normally associated with 14 and 13 will respond to transitions on TAI and TBI, respectively. General purpose lines 13 and 14 may still be used for I/O. A conceptual circuit of the timers in the pulse width measurement mode is shown in Figure 33.

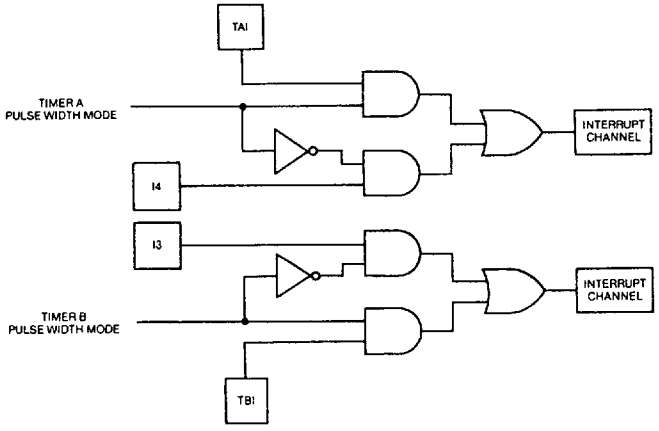

Figure 33 : Conceptual circuit of timers A and B in pulse width measurement mode.

The pulse width measurement mode functions similarly to the delay mode, with the auxiliary control signal acting as an enable to the timer. When the control signal is active, the prescaler and main counter are allowed to operate. When the control signal is negated, the timer is stopped. So, the width of the active pulse on TAI or TBI is measured by the number of timer counts which occur wile the timer is allowed to operate.

The active state of the auxiliary input line is defined by the associated interrupt channel's edge bit in the active edge register (AER). GPIP4 of the AER is the edge bit associated with TAI and GPIP3 is associated with TBI. When the edge bit is a one, the auxiliary input will be active high, enabling the timer while the input signal is at a high level. If the edge bit is low, the auxiliary input will be active low and the timer will operate while the input signal is at a low level.

The state of the active edge bit also specifies whether a zero to-one transition or a one-to-zero transition of the auxiliary input pin will produce an interrupt when the interrupt channel is enabled. In normal operation, programming the active edge bit to a zero will produce an interrupt on the one-to-zero transition of the input signal. However, in the pulse width measurement mode, the interrupt generated by a transition on TAI or TBI will occur on the opposite transition as that normally defined by the edge bit.

For example, in the pulse width measurement mode, if the edge bit is a one, the timer will be allowed to run while the auxiliary input TAI is high. When TAI transitions from high to low, the timer will stop and, if the interrupt channel is enabled, an interrupt will occur. By having the interrupt occur on the one-to-zero transition instead of the zero-to-one transition, the processor will be interrupted when the pulse being measured has terminated and the width of the pulse is available from the timer. Therefore, the timers act like a divide-by-prescaler that can be programmed by the timer data register and the timer's A and B control register.

After reading the contents of the timer, the main counter must be reinitialized by writing to the timer data register to allow consecutive pulses to be measured. If the timer is written after the auxiliary input signal is active, the timer will count from the previous contents of the timer data register until it counts through 01 (hexadecimal). At that time, the main counter is loaded with the new value from the timer data register, a time out pulse is generated which will toggle the timer output, and an interrupt may be optionally generated on the timer interrupt channel. Note that the pulse width measured will include counts from before the main counter was reloaded. If the timer data register is written while the pulse is transtioning to the active state, an indeterminate value may be written into the main counter.

Once the timer is reprogrammed for another mode, interrupts will again occur as normally defined by the edge bit. Note that an interrupt may be generated as the result of placing the timer into the pulse width measurement mode or by reprogramming the timer for another mode. Also, an interrupt may be generated by changing the stae of the edge bit while in the pulse width measurement mode.

6.4.1.3 - Event count mode operation

In addition to the delay mode and the pulse width measurement mode, timers A and B may be programmed to operate in the event count mode. Like the pulse width measurement mode, the event count mode also requires an auxiliary input signal, TAI or TBI, and the interrupt channels normally associated with 14 and 13 will respond to transitions on TAI and TBI, respectively. General purpose lines 13 and 14 still function normally.

In the event count mode the prescaler is disabled, allowing each active transition on TAI and TBI to produce a count pulse. The count pulse causes the main counter to decrement by one. When the timer counts through 01 (hexadecimal), a time out pulse is generated which will cause the output signal to toggle and may optionally produce an interrupt via the associated timer interrupt channel. The timer's main counter is also reloated from the timer clock periods. For this reason, the input signal must have a maximum frequency equal to one-fourth that of the timer clock.

The active edge of the auxiliary input signal is defined by the associated interrupt channel's edge bit. GPIP4 of the AER specifies the active edge for TAI and GPIP3 defines the active edge for TBI. When the edge bit is programmed to a one, a count pulse will be generated on the zero-to-one transition of the auxiliary input signal. When the edge bit is programmed to a zero, a count pulse will be generated on the one-to-zero transition. Also, note that changing the state of the edge bit while the timer is in the event count mode may produce a count pulse.

Besides generating a count pulse, the active transition of the auxiliary input signal will also produce an interrupt on the 13 or 14 interrupt channel, if the interrupt channel is enabled. Typically, in the event count mode, these channels are not enabled since the timer is automatically counting transitions on the input signal. If the interrupt channel were enabled, the number of transitions could be counted in the interrupt routine without requiring the use of the timer.

6.4.2 · Timer registers

The four timers are programmed via three control registers and four timer data registers. Control registers TACR and TBCR and timer data registers TADR and TBDR (refer to figure are associated with timers A and B respectively. Timers C and D are controlled by the control register TCDCR and the data registers TCDR and TDDR (refer to Figure 34).

(a) Timer A Data Register (TADR)

	7	6	5	4	3	2	1	0
Address 1F (Hex)	D7	D6	D5	D4	D3	D2	D1	D0

SET a) MPU writes a one.
CLEARED a) MPU writes a zero.

(b) Timer B Data Register (TBDR)

	7	6	5	4	3	2	1	0
Address 21 (Hex)	D7	D6	D5	D4	D3	D2	D1	D0

SET a) MPU writes a one.
CLEARED a) MPU writes a zero.

(c) Timer C Data Register (TCDR)

	7	6	5	4	3	2	1	0
Address 23 (Hex)	D7	D6	D5	D4	D3	D2	D1	D0

SET a) MPU writes a one.
CLEARED a) MPU writes a zero.

(d) Timer D Data Register (TDDR)

	7	6	5	4	3	2	1	0
Address 25 (Hex)	D7	D6	D5	D4	D3	D2	D1	D0

SET a) MPU writes a one.
CLEARED a) MPU writes a zero.

Figure 34 : Timer data registers.

6.4.2.1 - Timer data registers

Each timer's main counter is an 8-bit binary down counter. The value of the main counter may be read at any time by reading the timer's data register. The information read is the value of the counter which was captured on the last low-to-high transition of the DS pin.

The main counter is initialized by writing to the timer's data register. If the timer is stopped, data is loaded simultaneously into both the timer data register and the main counter. If the timer data register is written while the timer is enabled, the value is not loaded into the timer until the timer counts through 01 (hexadecimal). Writing the timer data register while the timer is counting through 01 (hexadecimal) will cause an indeterminate value to be loaded into the timer's main counter. The four data registers are shown in Figure 34.

6.4.2.2 - Timer control registers

Bits in the timer control registers select the operation mode, select the prescale value, and disable the timers. Timer control registers TACR and TBCR also have bits which allow the programmer to reset output lines TAO and TBO. These control registers are shown in Figure 35.

(a) Timer A Control Register (TACR)

	7	6	5	4	3	2	1	0
Address 19 (Hex)	★	★	★	Reset TA0	AC3	AC2	AC1	AC0

★ Unused bits read as zero.

(b) Timer B Control Register (TBCR)

	7	6	5	4	3	2	1	0
Address 1B (Hex)	★	★	★	Reset TB0	BC3	BC2	BC1	BC0

★ Unused bits read as zero.

Reset TAO/TBO : Timer's A and B output lines (TAO and TBO) may be forced low at any time by writing a one the reset location in TACR and TBCR respectively. The output will be held low only during the write operation at the conclusion of the operation the output will be allowed to toggle in response to a time-out pulse. When resetting TAO and TBO, the remaining bits in the control register must be written with their previous value to avoid altering the operating mode.
SET a) End of write cycle which clears the bit.
CLEARED a) MPU writes a zero.
b) Reset.

AC3-AC0, BC3-BC0 : These bits are decoded to determine the timer operation mode.

AC3 BC3	AC2 BC2	AC1 BC1	AC0 BC0	Operation Mode
0	0	0	0	Timer Stopped*
0	0	0	1	Delay Mode, + 4 Prescaler
0	0	1	0	Delay Mode, + 10 Prescaler
0	0	1	1	Delay Mode, + 16 Prescaler
0	1	0	0	Delay Mode, + 50 Prescaler
0	1	0	1	Delay Mode, + 64 Prescaler
0	1	1	0	Delay Mode, + 100 Prescaler
0	1	1	1	Delay Mode, + 200 Prescaler
1	0	0	0	Event Count Mode
1	0	0	1	Pulse Width Mode, + 4 Prescaler
1	0	1	0	Pulse Width Mode, + 10 Prescaler
1	0	1	1	Pulse Width Mode, + 16 Prescaler
1	1	0	0	Pulse Width Mode, + 50 Prescaler
1	1	0	1	Pulse Width Mode, + 64 Prescaler
1	1	1	0	Pulse Width Mode, + 100 Prescaler
1	1	1	1	Pulse Width Mode, + 200 Prescaler

* Regardless of the operation mode, counting is inhibited when the timer is stopped. The contents of the timer's main counter is not affected, althought any residual count in the prescaler is lost.

SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

(c) Timers C and D Control Register (TCDCR)

	7	6	5	4	3	2	1	0
Address 1D (Hex)	★	CC2	CC1	CC0	★	DC2	DC1	DC0

★ Unused bits read as zero.

CC2 - CC0 DC2 - DC0 : The bits are decoded to determine the timer operation mode.

CC2 DC2	CC1 DC1	CC0 DC0	Operation Mode
0	0	0	Timer Stopped*
0	0	1	Delay Mode, + 4 Prescaler
0	1	0	Delay Mode, + 10 Prescaler
0	1	1	Delay Mode, + 16 Prescaler
1	0	0	Delay Mode, + 50 Prescaler
1	0	1	Delay Mode, + 64 Prescaler
1	1	0	Delay Mode, + 100 Prescaler
1	1	1	Delay Mode, + 200 Prescaler

* When the timer is stopped, counting is inhibited. The contents of the timer's main counter is not affected, although any residual count in the prescaler is lost.

SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

Figure 35 : Timer control registers.

6.5 · Universal synchronous/asynchronous receiver-transmitter

The universal synchronous/asynchronous receiver-transmitter (USART) is a single full-duplex serial channel with a double-buffered receiver and transmitter. There are separate receive and transmit clocks and separate receive and transmit status and data bytes. The receive and transmit sections are also assigned separate interrupt channels. Each section has both a normal condition interrupt channel and an error condition interrupt channel. These channels can be optionally disabled from interrupting the processor and instead, DMA transfers can be performed using the receiver ready and transmitter ready external CMFP signals.

6.5.1 · Character protocols

The CMPFP USART supports asynchronous and with the aid of a polynomial generator checker (PGC) supports byte synchronous character formats. These formats are selected independently of the divide-by-one and divide-by-16 clock modes.

When the divide-by-one clock mode is selected, synchronization must be accomplished externally. The receiver will sample the serial data on the rising edge of the receiver clock. In the divide-by-16 clock mode, the data is sampled at mid-bit time to increase transient noise rejection.

Also, when the divide-by-16 clock is selected, the USART resynchronization logic is enabled. This logic increases the channel's clock skew tolerance. When a valid transition is detected, an internal counter is reset to state zero. Transition checking is then inhibited until state four. Then at state eight, the previous state of the transition checking logic is clocked into the receive shift register.

6.5.1.1 · Asynchronous format

Variable word length and start/stop bit configurations are available under software control for asynchronous operation. The word length can be five to eight bits and one, one and one-half, or two stop bits can be selected. The user can also slect odd, even, or no parity. For character lengths of less than eight bits, the assembled character will consist of the required number of data bits followed by zeros in the unused bit positions and a parity bit, if parity is enabled.

In the asynchronous format, start bit detection is always enabled. New data is not shifted into the receive shift register until a zero bit is received. When the divide-by-16 clock mode is selected, the false start bit logic is also active. Any transition must be stable for three positive receive clock edges to be considered valid. Then a valid zero-to-one transition must not occur for at least eight additional positive clock edges.

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6.5.1.1.1 · Wake-up feature

In a typical serial loop multiprocessor configuration, the software protocol will usually identify the addresse(s) at the beginning of the message. In order to permit uninterested MPUs to ignore the remainder of the message, wade-up feature is included whereby all further USART receiver flag (and interrupt) processing can be inhibited until its data line goes idle. An USART receiver is re-enabled by an idle string of ten consecutive ones of during reset. Software must provide for the required idle string between consecutive messages and prevent it within messages.

6.5.1.2 · Synchronous format

When the synchronus character format is selected, the 8-bit synchronous character loaded into the synchronous character register is compared to received serial data until a match is found. Once synchronization is established, incoming data is clocked into the receiver. The synchronous word will be continuously transmitted during an underrun condition. All synchronous characters can be optionally stripped from the receive buffer. Figure 36 shows the synchronous character register.

	7	6	5	4	3	2	1	0
Address 27 (Hex)	D7	D6	D5	D4	D3	D2	D1	D0

Figure 36 : Synchronous character register (SCR).

The synchronous character is typically written after the data word length is selected, since unused bits in the synchronous character register are zeroed out. When parity is enabled, synchronous word length is the data word length plus one. The CMFP will compute and append the parity bit for the synchronous word when a word length of eight is selected. However, if the word length is less than eigth, the user must determine the synchronous word parity and write it into the synchronous character register along with the synchronous character. The CMFP will then transmit the extra bit in the synchronous word as a parity bit.

6.5.1.3 · USART control register

The USART control register (UCR) selects the clock mode and the character format for the receive and transmit sections. This register is shown in Figure 37.

6.5.2 · Receiver

As data is received on the serial input line (S1), it is clocked into an internal 8-bit shift register until the specified number of data bits have been assembled. This character will then be transferred to the receive buffer, assuming that the last word in the receiver buffer has been read. This transfert produces a buffer full interrupt to the processor.

Reading the receive buffer satisfies the buffer full condition and allows a new data word to be transferred to the receive buffer when it is assembled. The receive buffer is accessed by reading the USART data register (UDR). The UDR is simply an 8-bit data register used when transferring data from the CMFP and the CPU.

Each time a word is transferred to the receive buffer, its status information is latched into the receiver status register (RSR). The RSR is not updated again until the data word in the receive buffer has been read. When a buffer full condition exists, the RSR should always be read before the receive buffer (UDR) to maintain the correct correspondance between data and flags. Otherwise, it is possible that after reading the UDR and prior to reading the RSR, a new word could be received and transferred to the receive buffer. Its associated flags would ba latched into the RSR overwriting the flags for the previous data word. Then when the RSR were read to access the status information for the first data word, the flags for the new word would be retrieved.

	7	6	5	4	3	2	1	0
Address 29 (Hex)	CLK	WL1	WL0	ST1	ST0	PE	E/O	WU

CLK : Clock Mode. When this bit is zero, data will be clocked into and out of the receiver and transmitter at the frequency of their respective clocks. When this bit is a one, data will be clocked into and out of the receiver and transmittor at one sixteenth the frequency of their respective clocks. Also, the receiver data transition resynchronization logic will be enabled.
SET + 16 a) MPU writes a one.
CLEARED + 1 a) MPU writes a zero.
b) Reset.

WL0, WL1 : Word Length. These two bits specify the length of the data word exclusive of start bits, stop bits, and parity.

WL1	WL0	Word Length
0	0	8 Bits
0	1	7 Bits
1	0	6 Bits
1	1	5 Bits

SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

ST0, ST1 : Start/Stop Bit and format control. These two bits select the number of start and stop bits and also specify the character format.

ST1	ST0	Start Bits	Stop Bits	Format
0	0	0	0	Synchronous
0	1	1	1	Asynchronous
1	0	1	1 1/2	Asynchronous*
1	1	1	2	Asynchronous

* Only used with divide-by-16 clock mode.

SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

PE : Parity Enable. When this bit is zero, no parity check will be made and no parity bit will be computed for transmission. When this bit is a one, parity will be checked by the receiver and parity will be calculated and inserted during data transmission. Note that parity is not automatically appended to the synchronous character for word lengths of less than eight bits in this case, the parity should be written into the synchronous character register along with the synchronous word.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

E/O : Even/Odd Parity. When this bit is zero, odd parity is selected. When this bit is a one, even parity is selected.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

WU : Bit 0 «Wake-up» in idle line. When set, WU enables the wake-up function ; it is cleared by ten consecutive ones or during reset. WU will not be set if the line is idle. Refer to § 6.5.1.1.1.

Figure 37 : Usart control register (UCR).

6.5.2.1 - Receiver interrupt channels

The USART receive section, is assigned two interrupt channels. One indicates the buffer full condition, while the other channel indicates an error condition. Error conditions include overrun, parity error, synchronous found, and break. These interrupting conditions correspond to the BF, OE, PE, and F/S or B bits of the receiver status register. These flags will function as described in § 6.5.2.2 whether the receiver interrupt channels are enabled or disabled.

While only one interrupt is generated per character received, two dedicated interrupt channels allow separate vector numbers to be assigned for normal and abnormal receiver conditions. When a received word has an error associated with it and the error interrupt channel is enabled, an interrupt will be generated on the error channel only. However, if the error channel is disabled, an interrupt for an error condition will be generated on the buffer full interrupt channel along with interrupts produced by the buffer full condition. The receiver status register must always be read to determine which error condition produced the interrupt.

6.5.2.2 - Receiver status register

The receiver status contains the receive buffer full flag, the synchronous strip enable, the receiver enable, and various status information associated with the data word in the receive buffer. The RSR is latched each time a data word is transferred to the receive buffer. RSR flags cannot change again until the data word has been read. The exception is the character in progress flag which monitors when a new word is being assembled in the asynchronous character format. The receiver status register is shown on Figure 38.

Address 28	BF	OE	PE	FE	F/S or B	M/CIP	SS	RE

BF : Buffer Full. This bit is set when a received word is transferred ot the receive buffer. This bit is cleared when the receive buffer is read by accessing the USART data register (UDR) this bit is read only.
SET a) Received word transferred to buffer.
CLEARED a) Receive buffer read.
b) Reset.

OE : Overrun Error. An overrun error occurs when a received word is due to be transferred to the receive buffer, but the receive buffer is full. Neither the receive buffer not the RSR is overwritten. The OE bit is set after the receive buffer full condition is satisfied by reading the UDR. This error condition will generate an interrupt to the processor. The OE bit is cleared by reading the RSR. New data words will not be assembled until the RSR is read.
SET a) Incoming word received and receive buffer full.
CLEARED a) Receiver status register read.
b) Reset.

PE : Parity Error. This bit is set when the word transferred to the receive buffer has a parity error. This bit is cleared when the word transferred to the receive buffer does not have a parity error.
SET a) Word in receive buffer has a parity error.
CLEARED a) Word in receive buffer does not have a parity error.
b) Reset.

FE : Frame Error. A frame error exists when a non-zero data word is not followed by a stop bit in the asynchronous character format. The FE bit is set when the word transferred to the receive buffer has a frame erro. The FE bit is cleared when the word transferred to the receive buffer does not have a frame error.
SET a) Word in receive buffer has a frame error.
CLEARED a) Word in receive buffer does not have a frame error.
b) Reset.

F/S or B : Found/Search or Break Detect. In the synchronous character format this bit can be set or cleared in software. When the bit is a zero, the USART receiver is placed in the search mode. The incoming data is compared to the synchronous character register (SCR) and the word length counter is disabled. The F/S bit will automatically be set when a match is found and the word length counter will be enabled. An interrupt will also be produced on the receive error channel.
SET a) Incoming word matches synchronous character.
CLEARED a) MPU writes a zero.
b) Incoming word does not match synchronous character.
c) Reset.

In the asynchronous character format, this flag indicates a break condition. A break is detected when an all zero data word with no stop bit is received. The break condition continues until a non-zero data bit is received. The B bit is set when the word transferred to the receive buffer is a break indication. A break condition generates an interrupt to the processor. This bit is cleared when a non-zero data bit is received and the break condition has been acknowledged by reading the RSR at least once. An end of break interrupt will be generated when the bit is cleared.
SET a) Word in receive buffer is a break.
CLEARED a) Break terminates and receiver status register read since beginning of break condition.
b) Reset.

M or CIP : Match/Character in Progress. In the synchronous character format, this flag indicates that a synchronous character has been received. The M bit is set when the word transferred to the receive buffer matches the synchronous character register. The M bit is cleared when the word transferred to the receive buffer does not match the synchronous character register.
SET a) Word transferred to receive buffer matches the synchronous character.
CLEARED a) Word transferred to receive buffer does match synchronous character.
b) Reset.

In the asynchronous character format, this flag indicates that a word is being assembled. The CIP bit is set when a start bit is detected. The CIP bit is cleared when the final stop bit has been received.
SET a) Start bit is detected.
CLEARED a) End of word detected.
b) Reset.

SS : Synchronous Strip Enable. When this bit is a one, data words that match the synchronous character register will not be loaded into the receive buffer and no buffer full condition will be produced. When this bit is a zero, data words that match the synchronous character register will be transferred to the receive buffer and a buffer full condition will be produced.
SET a) MPU writes a one.
CLEARED a) MPU writtes a zero.
b) Reset.

RE : Receiver Enable. When this bit is a zero, the receiver will be immediately disabled. All flags will be cleared. When this bit is a one, normal receiver operation is enabled. This bit should not be set to a one until the receiver clock is active.
SET a) MPU writes a one.
b) Transmitter is disabled in auto-turnaround mode.
CLEARED a) MPU writes a zero.
b) Reset.

Figure 38 : Receiver status register (RSR).

6.5.2.3 · Special receive considerations

Certain receive conditions relating to the overrun error flag and the break detect flag require further explanation. Consider the following examples :

1) A break is received while the receive buffer is full. This does not produce an overrun condition. Only the B flag will be set after the receiver buffer is read.

2) A new word is received and the receive buffer is full. A break is received before the receive buffer is read. Both the B and OE flags wil be set when the buffer full condition is satisfied.

6.5.3 · Transmitter

The transmit buffer is loaded by writing to the USART data register (UDR). The data word will be transferred to an internal 8-bit shift register when the last word in the shift register has been transmitted. This will produce a buffer empty condition. If the transmitter completes the transmission of the word in the shift register before a new word is written to the transmit buffer, an underrun error will occur. In the asynchronous character format, the transmitter will send a mark until the transmit buffer is written. In the synchronous character format, the transmitter will continuously send the synchronous character.

The transmit buffer can be loaded prior to enabling the transmitter. After the transmitter is enabled, there is a delay before the first bit is output. The serial output line (SO) should be programmed to be high, low, or high impedance when the transmitter is enabled to force the output line to the desired state until the transmitted prior to the word in the transmit shitf register when the transmitter is first enabled.

When the transmitter is disabled, any word currently being transmitted will continue to completion. Howerver, any word in the transmit buffer will not be transmitted and will remain in the buffer. So, no buffer empty condition will occur. If the buffer is empty when the transmitter is disabled, the buffer empty condition will remain, but no underrun condition will be generated when the word in transmission is completed. If no word is being transmitted when the transmitter is disabled, the transmitter will stop at the next rising edge of the internal shift clock.

In the asynchronous character format, the transmitter can be programmed to send a break. The break will be transmitted once the word currently in the shift register has been sent. If the shift register is empty, the break command will be effective immediately. An END interrupt will be generated at every normal character boundary to aid in timing the break transmission. The break will continue until the break command is cleared.

Any character in the transmit buffer at the start of a break will be transmitted when the break is terminated. If the transmit buffer is empty at the start of a break, it may be written at any time during the break. If the buffer is still empty at the end of the break, an underrun condition will exist.

Disabling the transmitter during a break condition causes the transmitter to cease transmission of the break character at the end of the current character. No end of break stop bit will be transmitted. Even if the transmit buffer is empty, no buffer empty condition will occur nor will an underrun condition occur. Also, any word in the transmit buffer will remain.

6.5.3.1 · Transmitter interrupt channels

The USART transmit sectin is assigned two interrupt channels. One channel indicates a buffer empty condition and the other channel indicates an underrun or end condition. These interrupting conditions correspond to the BE, UE, and END flag bits of the transmitter status register (TCR). The flag bits will function as described in § 6.5.3.2 whether their associated interrupt channel is enabled or disabled.

6.5.3.2 · Transmitter status register

The transmitter status register contains various transmitter error flags and transmitter control bits for selecting autoturnaround and loopback mode. The TSR is shown in Figure 39.

	7	6	5	4	3	2	1	0
Address 2D (Hex)	BE	UE	AT	END	B	H	L	TE

BE : Buffer Empty. This bit is set when the word in the transmit buffer is transferred to the transmit shift register. This bit is cleared when the transmit buffer is reloaded by writing to the USART data register (UDR).
SET a) Transmit buffer contents transferred to transmit shift register.
CLEARED a) Transmit buffer written.

UE : Underrun Error. This bit is set when the would in the transmit shift register has been transmitted before a new word is loaded into the transmit buffer. This bit is cleared by reading the TSR or by disabling the transmitter. This bit does not need to be cleared before writing to the UDR.
SET a) Transmit shift register contents transmitted before transmit buffer written.
CLEARED a) Transmitter status register read.
b) Transmitter disabled.

AT : Auto Turnaround. When this bit is set, the receiver will be enabled automatically after the transmitter has been disabled and the last character being transmitted is completed.
SET a) MPU writes a one.
CLEARED a) Transmitter disabled.

END : End of Transmission. When the transmitter is disabled while a character is being transmitted, the END with be set after the character transmission is complete. If no word is being transmitted when the transmitter is disabled, the END bit will be set immediately. The END bit is cleared by reenabling the transmitter.
SET a) Transmitter disabled.
CLEARED a) Transmitter enabled.

B : Break. This bit has no function in the synchronous character format. In the asynchronous character format, when this bit is set to a one, a break will be transmitted upon the completion of the transmission of any word in the transmit shift register. A break consists of an all zero data word with no stop bit. When this bit is cleared by software, the break indication will cease and normal transmission will resume. Note that when B is set, BE cannot be set.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.

H, L : High and Low. These control bits configure the transmitter output (SO) when the transmitter is disabled. These bits also force the transmitter output after the transmitter is enabled until END is cleared.

H	L	Output State
0	0	High Impedance
0	1	Low
1	0	High
1	1	Loopback Mode

Loopback mode internally connects the transmitter output to the receiver input and the transmitter clock to the receiver clock internally. The receiver clock (RC) and the serial input (SI) are not used. When the transmitter is disabled. SO is forced high.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.

TE : Transmitter Enable. When this bit is cleared, the transmitter is disabled. The UE will be cleared and the END bit will be set. When this bit is set, the transmitter is enabled. The transmitter output will be driven according to the H and L bits until transmission begins. A one bit will be transmitted before the transmission of the word in the transmit shift register is begun.
SET a) MPU writes a one.
CLEARED a) MPU writes a zero.
b) Reset.

Figure 39 : Transmitter status register (TSR).

7 · PREPARATION FOR DELIVERY

7.1 · Packaging

Microcircuits are prepared for delivery in accordance with MIL-M-38510 or CECC 90000.

7.2 · Certificate of compliance

TCS offers a certificate of compliances with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or CECC 90000 and guarantying the parameters not tested at temperature extremes for the entire temperature range.

8 · HANDLING

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended :

a) Devices should be handled on benches with conductive and grounded surfaces.

b) Ground test equipment, tools and operator.

c) Do not handle devices by the leads.

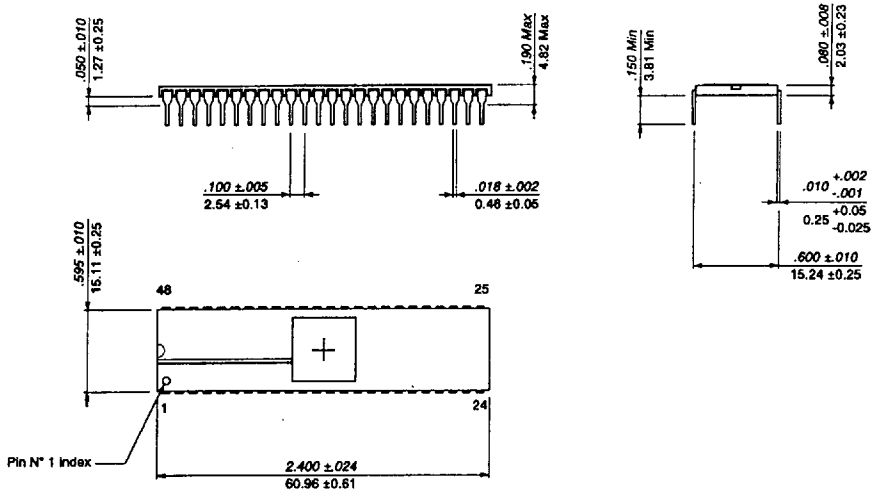
d) Store devices in conductive foam or carriers.

e) Avoid use of plastic, rubber, or silk in MOS areas.

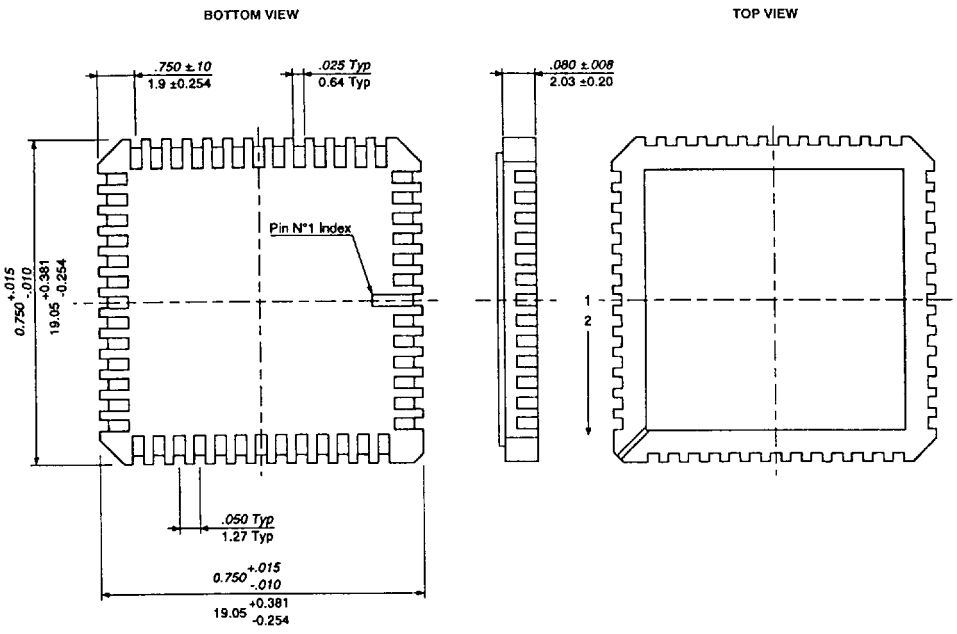
f) Maintain relative humidity above 50 percent if practical.

9 · PACKAGE MECHANICAL DATA

9.1 · 48 Pins · Ceramic DIL



9.2 - 52 Pins - Leadless ceramic chip carrier



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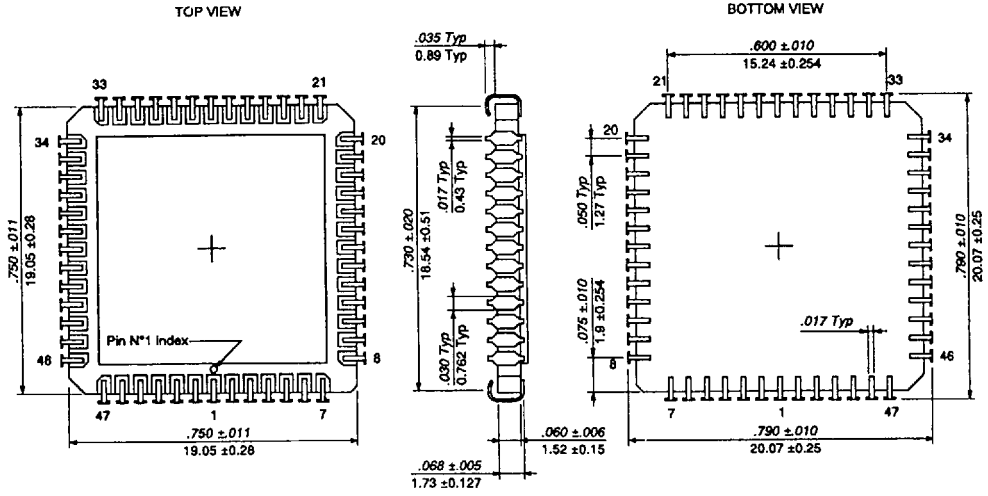
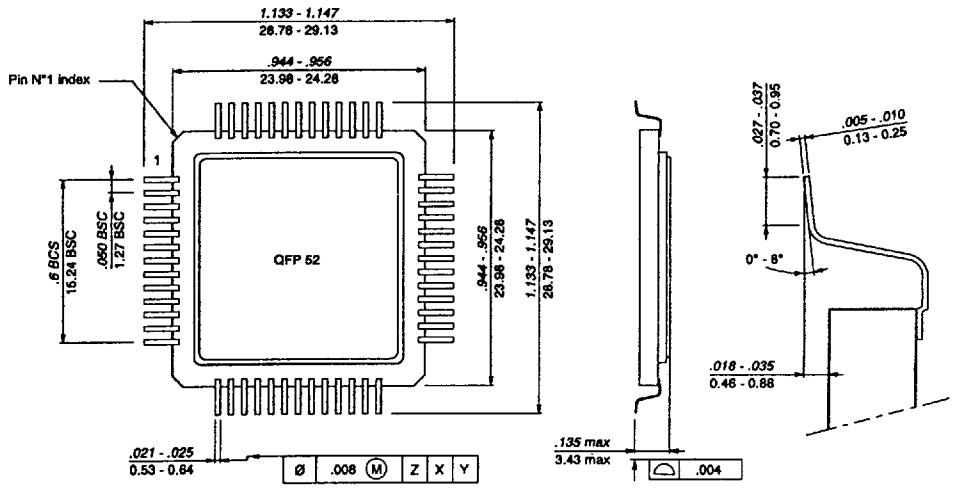
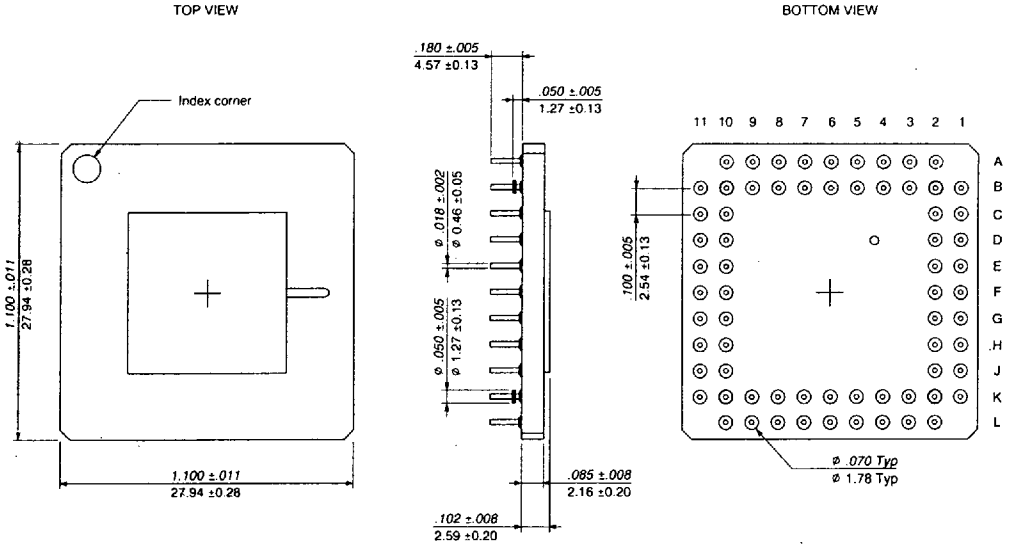
9.3 - 52 Pins - Leaded ceramic chip carrier (on request only)



9.4 - 52 Pins - Ceramic quad flat pack

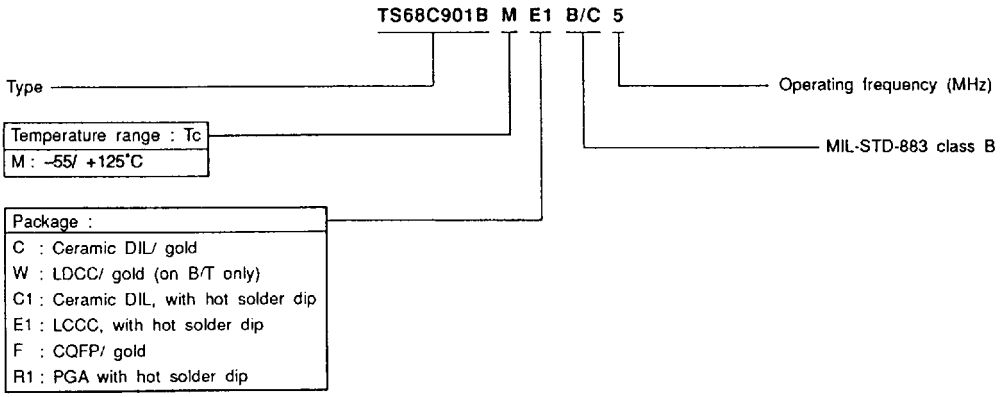


9.5 - 68 Pins - Pin Grid Array



10 · ORDERING INFORMATION

10.1 · MIL-STD-883 C



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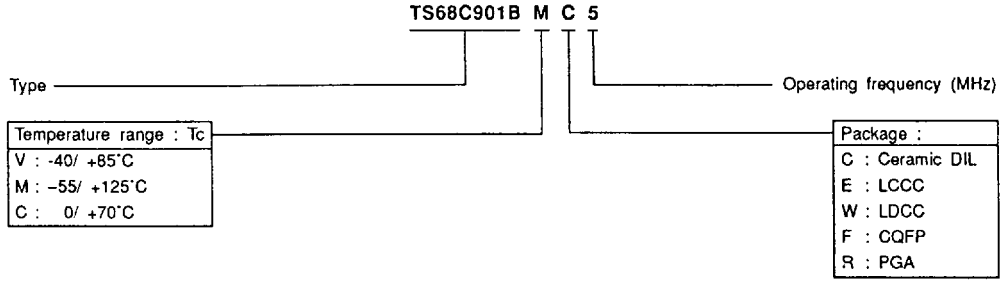
10.2 · Standard product



10.3 · Detailed TS 68C901B part list

10.3.1 · Hi-REL product

Commercial TCS part number (see Note)	Norms	Package	Temperature range T_{case} (°C)	Frequency (MHz)	Drawing number
TS68C901BMCB/C4	MIL-STD-883	DIL 48	– 55 / + 125	4	TCS data sheet
TS68C901BMCB/C5	MIL-STD-883	DIL 48	– 55 / + 125	5	TCS data sheet
TS68C901BMCB/C8	MIL-STD-883	DIL 48	– 55 / + 125	8	TCS data sheet
TS68C901BME1B/C4	MIL-STD-883	LCCC 52	– 55 / + 125	4	TCS data sheet
TS68C901BME1B/C5	MIL-STD-883	LCCC 52	– 55 / + 125	5	TCS data sheet
TS68C901BME1B/C8	MIL-STD-883	LCCC 52	– 55 / + 125	8	TCS data sheet
TS68C901BMWB/T4	MIL-STD-883	LDCC 52	– 55 / + 125	4	on request only
TS68C901BMWB/T5	MIL-STD-883	LDCC 52	– 55 / + 125	5	on request only
TS68C901BMWB/T8	MIL-STD-883	LDCC 52	– 55 / + 125	8	on request only
TS68C901BMFB/C8	MIL-STD-883	CQFP 52	– 55 / + 125	8	TCS data sheet
TS68C901BDESC01XA	DESC	DIL 48	– 55 / + 125	4	5962-9086401XA
TS68C901BDESC02XA	DESC	DIL 48	– 55 / + 125	5	5962-9086402XA
TS68C901BDESC03XA	DESC	DIL 48	– 55 / + 125	8	5962-9086403XA
TS68C901BDESC01YA	DESC	LCCC 52 + hot solder dip	– 55 / + 125	4	5962-9086401YA
TS68C901BDESC02YA	DESC	LCCC 52 + hot solder dip	– 55 / + 125	5	5962-9086402YA
TS68C901BDESC03YA	DESC	LCCC 52 + hot solder dip	– 55 / + 125	8	5962-9086403YA
TS68C901BMFB/C4	MIL-STD-883	CQFP 52	– 55 / + 125	4	TCS data sheet
TS68C901BMFB/C5	MIL-STD-883	CQFP 52	– 55 / + 125	5	TCS data sheet
TS68C901BMFB/C8	MIL-STD-883	CQFP 52	– 55 / + 125	8	TCS data sheet

Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.

10.3.2 · Standard product

Commercial TCS part number (see Note)	Norms	Package	Temperature range T_{case} (°C)	Frequency (MHz)	Drawing number
TS68C901BVC4	TCS standard	DIL 48	−40 / +85	4	TCS data sheet
TS68C901BVC5	TCS standard	DIL 48	−40 / +85	5	TCS data sheet
TS68C901BVC8	TCS standard	DIL 48	−40 / +85	8	TCS data sheet
TS68C901BMC4	TCS standard	DIL 48	−55 / +125	4	TCS data sheet
TS68C901BMC5	TCS standard	DIL 48	−55 / +125	5	TCS data sheet
TS68C901BMC8	TCS standard	DIL 48	−55 / +125	8	TCS data sheet
TS68C901BME4	TCS standard	LCCC 52	−55 / +125	4	TCS data sheet
TS68C901BME5	TCS standard	LCCC 52	−55 / +125	5	TCS data sheet
TS68C901BME8	TCS standard	LCCC 52	−55 / +125	8	TCS data sheet
TS68C901BMW4	TCS standard	LDCC 52	−55 / +125	4	on request only
TS68C901BMW5	TCS standard	LDCC 52	−55 / +125	5	on request only
TS68C901BMW8	TCS standard	LDCC 52	−55 / +125	8	on request only
TS68C901BMF4	TCS standard	CQFP 52	−55 / +125	4	TCS data sheet
TS68C901BMF5	TCS standard	CQFP 52	−55 / +125	5	TCS data sheet
TS68C901BMF8	TCS standard	CQFP 52	−55 / +125	8	TCS data sheet
Note : THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES.					

5

APPLICATION NOTE (July 1992)

TIMERS USE FOR TS 68C901B IN POLLING MODE

Due to the use of high speed processors, the user can have some trouble with the timers of the TS 68C901B (CMFP).

The problem occurs when polling is made on the timer data registers (TxDR) for the 4 timers of the CMFP if different clock sources are used for CLK input and timer clock (XTAL1/XTAL2).

Due to the fact that there is no phase relation between the 2 clock sources, the content of the TADR, TBDR, TCDR and TDDR (TxDR) can be modified when $\overline{\text{DTACK}}$ signal is asserted at low state.

This problem occurs because high speed CPU can perform lots of accesses to the CMFP during a short period of time. The TxDR are updated after a rising edge of DS signal plus a particular timer clock phase which is activated by a particular rising edge of XTAL1 signal. This TxDR update can occurs during a CPU access if there is no phase relation between XTAL1 and CLK.

Rem : If timers are only used to generate baud rate or are used as delay interrupt sources, there is no problem with the CMFP.

That means that if the TxDR are not read back when timer is running, the CMFP can be used as usualy.

Work around

To avoid this problem, 2 hardware solutions can be implemented. These solutions can be used only if XTAL1 signal is a logical signal (no crystal used for XTAL1/XTAL2). This means that it is possible to externally synchronize the 2 CMFP clocks (CLK and XTAL1).

This solution is usefull for XTAL1 at «high frequency» (min spec. is 1 MHz). The goal is to delay the $\overline{DTACK}$ signal as far as possible from a rising edge of the XTAL1 signal.

In that case, the worst access time is about one XTAL1 period (1/2 XTAL1 period plus CMFP access time) so it is about 1 μs worst case. This value must be considerated if a bus error detection is used in the application.

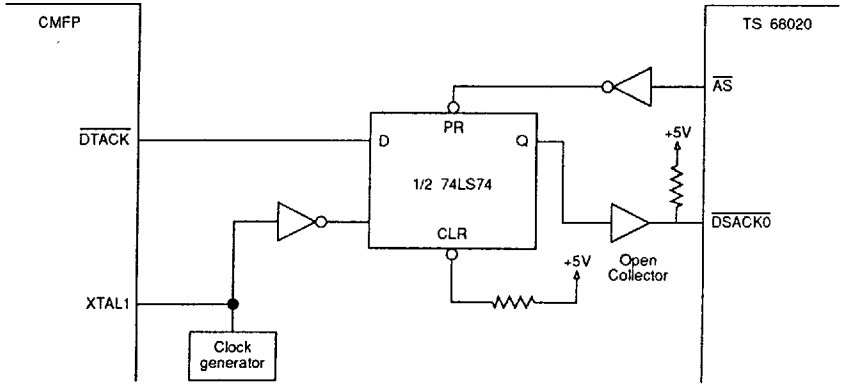


Figure 1 : Work around for «high frequency» clock.

This second solution must be considerate when the TAI or TBI inputs are used as «low frequency» timer clock. In that case, the event count input (TAI or TBI) can not toggles when the CMFP is selected ($\overline{CS}$ = 0) so no TxDR modification can occurs and the data bus is stable during the CMFP access from the CPU.

Do not forget that any toggle of TAI can not be detected during an CMFP access. The CMFP keeps a normal behaviour only if the time during $\overline{CS}$ = 0 is less than a TAI (TBI) period plus min. timer pulse width.

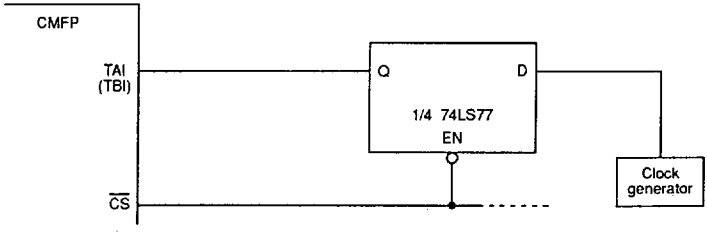


Figure 2 : Work around for «low frequency» clock.

- TS 68020 377
- TS 68040 409
- TS 68882 447
- TS 88100 483
- TS 88200 485
- TS 88915T 487