TRIPLE ELEMENT BIDIRECTIONAL THYRISTOR OVERVOLTAGE PROTECTOR

TISP7250H3SLL Overvoltage Protector

3-Pin Long Lead Through-Hole Package
– Compatible with TO-220AB Pin-Out

Ion-Implanted Breakdown Region
– Precise and Stable Voltage

Low Voltage Overshoot Under Surge

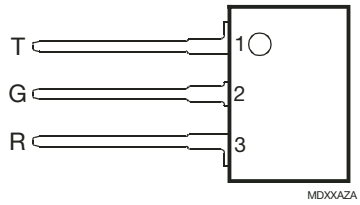
Device Name	V_{DRM} V	$V_{(BO)}$ V
TISP7250H3SLL	200	250

Rated for International Surge Wave Shapes
– Single and Simultaneous Impulses

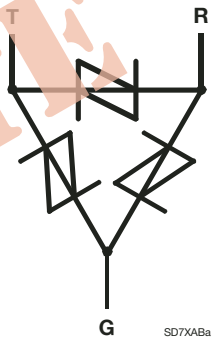
Wave Shape	Standard	I_{PPSM} A
2/10	GR-1089-CORE	500
8/20	IEC 61000-4-5	350
10/160	TIA-968-A	250
10/700	TIA-968-A ITU-T K.20/21	200
10/560	TIA-968-A	130
10/1000	GR-1089-CORE	100

..... UL Recognized Component

3-SIP (Long Lead) Package (Top View)



Device Symbol



Description

The TISP7250H3SLL limits overvoltages between the telephone line Ring and Tip conductors and Ground. Overvoltages are normally caused by a.c. power system or lightning flash disturbances which are induced or conducted on to the telephone line.

Each terminal pair, T-G, R-G and T-R, has a symmetrical voltage-triggered bidirectional thyristor protection characteristic. Overvoltages are initially clipped by breakdown clamping until the voltage rises to the breakover level, which causes the device to crowbar into a low-voltage on-state. This low-voltage on-state causes the current resulting from the overvoltage to be safely diverted through the device. The high crowbar holding current helps prevent d.c. latchup as the diverted current subsides.

These monolithic protection devices are fabricated in ion-implanted planar structures to ensure precise and matched breakover control and are virtually transparent to the system in normal operation. They are designed to voltage limit and withstand the listed international lightning surges in both polarities.

How To Order

Device	Package	Carrier	Order As	Marking Code	Std. Qty.
TISP7250H3SLL	3-SIP (Long Lead)	Tube	TISP7250H3SLL-S	SP7250H3	1000

*RoHS Directive 2002/95/EC Jan 27 2003 including Annex
FEBRUARY 2005 - REVISED MAY 2007
Specifications are subject to change without notice.
Customers should verify actual device performance in their specific applications.

Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit
Repetitive peak off-state voltage (see Note 1)	V_{DRM}	±200	V
Non-repetitive peak impulse current (see Notes 2 and 3)			
2/10 µs (GR-1089-CORE, 2/10 µs voltage wave shape)	I_{PPSM}	±500	A
8/20 µs (IEC 61000-4-5, 1.2/50 µs voltage wave shape, 8/20 current combination wave generator)		±350	
10/160 µs (TIA-968-A, 10/160 µs voltage wave shape)		±250	
4/250 µs (ITU-T K.20/21, 10/700 µs voltage waveshape, dual)		±225	
0.2/310 µs (CNET I 31-24, 0.5/700 µs voltage waveshape)		±200	
5/310 µs (ITU-T K.20/21, 10/700 µs voltage wave shape, single)		±200	
5/320 µs (TIA-968-A, 9/720 µs voltage wave shape)		±200	
10/560 µs (TIA-968-A, 10/560 µs voltage wave shape)		±130	
10/1000 µs (GR-1089-CORE, 10/1000 µs voltage wave shape)		±100	
Non-repetitive peak on-state current (see Notes 2, 3 and 4)			
20 ms, 50 Hz (full sine wave)	I_{TSM}	55	A
16.7 ms 60 Hz (full sine wave)		60	
1000 s, 50 Hz a.c.		0.9	
Initial rate of rise of on-state current, exponential current ramp, maximum ramp value < 200 A	di_T/dt	400	A/µs
Junction temperature	T_J	-40 to +150	°C
Storage temperature range	T_{stg}	-65 to +150	°C

NOTES: 1. Derate value at -0.13 %/°C for ambient temperatures below 25 °C.
2. Initially the device must be in thermal equilibrium with T_J = 25 °C.
3. These non-repetitive rated currents are peak values of either polarity. The rated current values may be applied to any terminal pair. Additionally, both R and T terminals may have their rated current values applied simultaneously (in this case the G terminal return current will be the sum of the currents applied to the R and T terminals). The surge may be repeated after the device returns to its initial conditions.
4. EIA/JESD51-2 environment and EIA/JESD51-3 PCB with standard footprint dimensions connected with 5 A rated printed wiring track widths. Derate current values at -0.61 %/°C for ambient tempeartures above 25 °C.

Electrical Characteristics for any Terminal Pair, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
I_{DRM}	Repetitive peak off-state current	$V_D = V_{DRM}$ T_A = 25 °C			±5	µA
		$V_D = V_{DRM}$ T_A = 85 °C			±10	
$V_{(BO)}$	Breakover voltage	dv/dt = ±750 V/ms, R_{SOURCE} = 300 Ω			±250	V
$V_{(BO)}$	Impulse breakover voltage	dv/dt ≤ ±1000 V/µs, Linear voltage ramp, Maximum ramp value = ±500 V di/dt = ±20 A/µs, Linear current ramp, Maximum ramp value = ±10 A			±261	V
$I_{(BO)}$	Breakover current	dv/dt = ±750 V/ms, R_{SOURCE} = 300 Ω	±100		±800	mA
V_T	On-state voltage	I_T = ±5 A, t_w = 100 µs			±5	V
I_H	Holding current	I_T = ±5 A, di/dt = ±30 mA/ms	±150		±600	mA
dv/dt	Critical rate of rise of off-state voltage	Linear voltage ramp, maximum ramp value < 0.85V_{DRM}	±5			kV/µs
I_D	Off-state current	V_D = ±50 V T_A = 85 °C			±10	µA
C_O	Off-state capacitance	f = 1 MHz, V_d = 1 V rms, V_D = 0 V			84	pF
		f = 1 MHz, V_d = 1 V rms, V_D = -1 V			67	
		f = 1 MHz, V_d = 1 V rms, V_D = -2 V			62	
		f = 1 MHz, V_d = 1 V rms, V_D = -50 V			28	
		f = 1 MHz, V_d = 1 V rms, V_D = -100 V			26	

Thermal Characteristics, T_A = 25 °C (Unless Otherwise Noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	EIA/JESD51-3 PCB, $I_T = I_{TSM(1000)}$ (see Note 5)			50	°C/W

NOTE: 5. EIA/JESD51-2 environment and PCB has standard footprint dimensions connected with 5 A rated printed wiring track widths.

Parameter Measurement Information

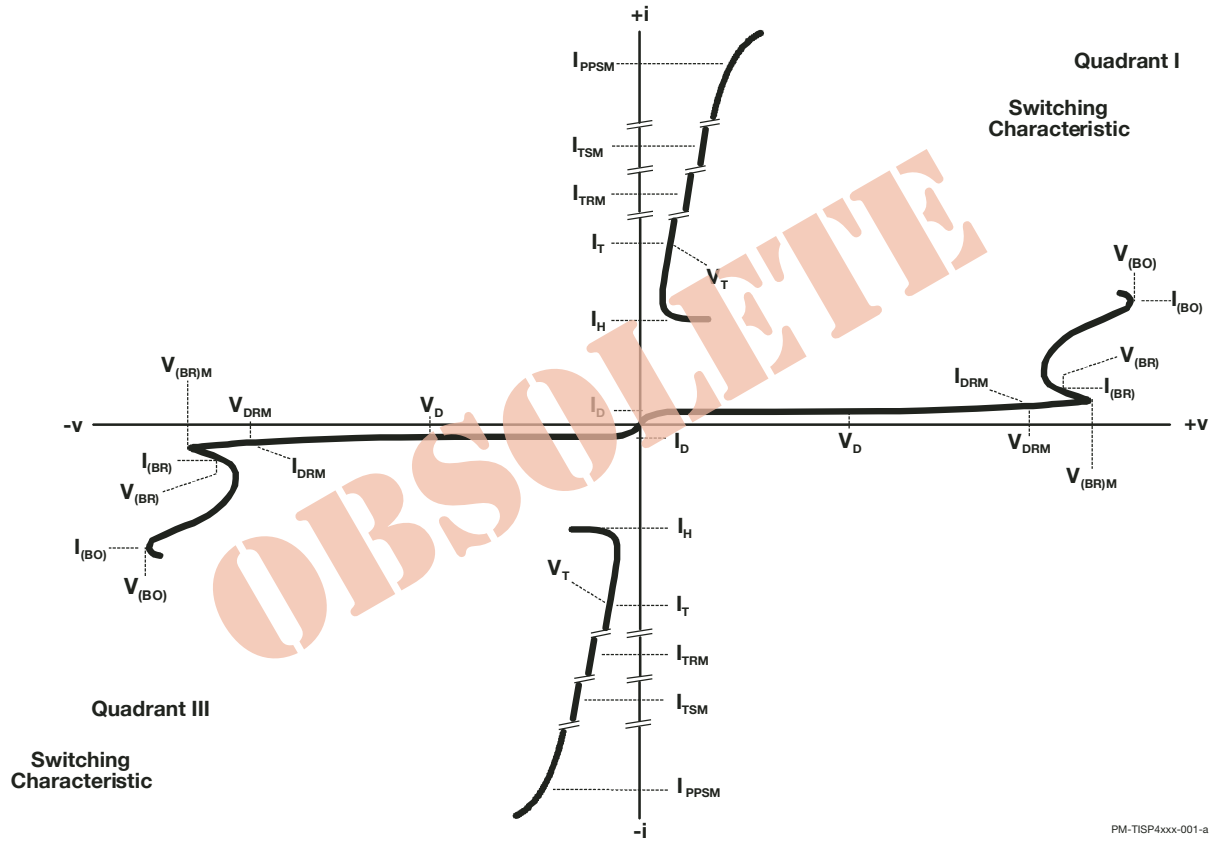


Figure 1. Voltage-Current Characteristic for Terminal Pairs

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