Austin Semiconductor, Inc.

UVEPROM
SMJ27C256
AS27C256

256K UVEPROM

UV Erasable Programmable
Read-Only Memory

AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-86063
- MIL-STD-883
- COTS-PEMS Version

FEATURES

- Organized 32,768 x 8
- Single +5V ±10% power supply
- Pin-compatible with existing 256K ROM's and EPROM's
- All inputs/outputs fully TTL compatible
- Power-saving CMOS technology
- Very high-speed SNAP! Pulse Programming
- 3-state output buffers
- 400-mV DC assured noise immunity with standarad TTL loads
- Latchup immunity of 250 mA on all input and output pins
- Low power dissipation (CMOS Input Levels)
  -Active - 165mW Worst Case
  -Standby - 1.7mW Worst Case (CMOS-input levels)

OPTIONS — MARKING

- **Timing**

150ns access	-15
170ns access	-17
200ns access	-20
250ns access	-25
300ns access	-30

- **Package(s)**

Ceramic DIP (600mils)	J	No. 110
Ceramic LCC (450 x 550 mils)	ECA	No. 208

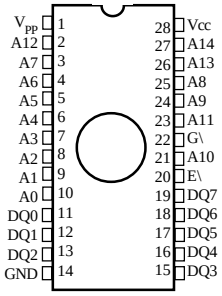
- **Operating Temperature Ranges**

Military (-55°C to +125°C)	M
Industrial (-40°C to +85°C)	I

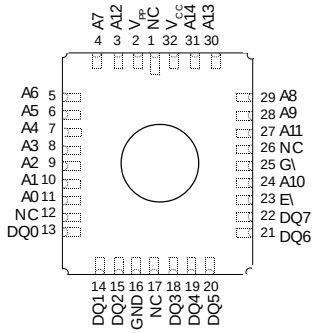
For more products and information please visit our web site at *www.austinsemiconductor.com*

PIN ASSIGNMENT
(Top View)

28-Pin DIP (J)
(600 MIL)



32-Pin LCC (ECA)
(450 x 550 mils)



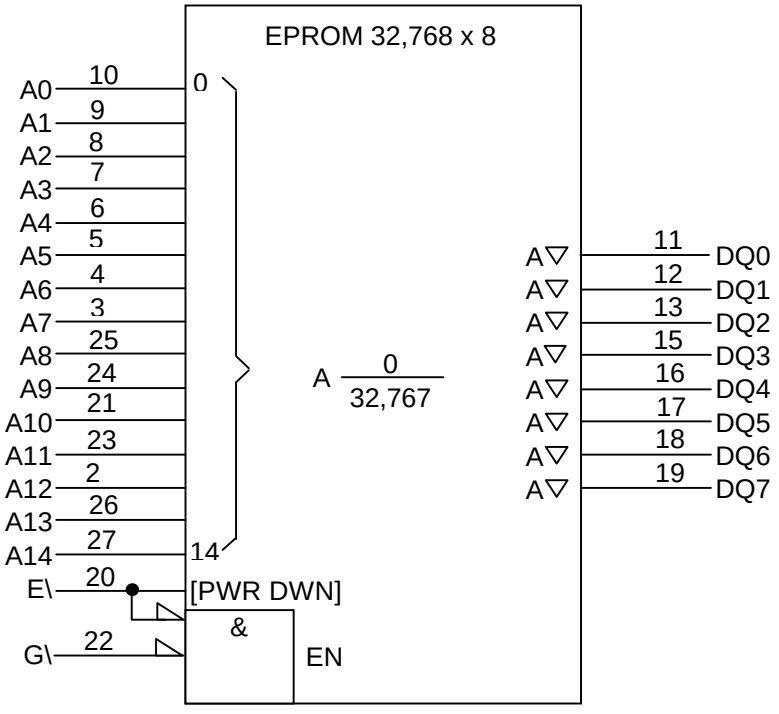
Pin Name	Function
A0 - A14	Address Inputs
DQ0-DQ7	Inputs (programming)/Outputs
E\	Chip Enable/Power Down
G\	Output Enable
GND	Ground
V_{CC}	5V Supply
V_{PP}	13V Programming Power Supply

GENERAL DESCRIPTION

The SMJ27C256 series is a set of 262,144 bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using power-saving CMOS technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 54 TTL circuits without the use of external pullup resistors. Each output can drive one Series 54 TTL circuit without external resistors. The data outputs are 3-state for connecting multiple devices to a common bus. The SMJ27C256 is pin-compatible with 28-pin 256K ROMs and EPROMs. It is offered in a 600mil dual-in-line ceramic package (J suffix) and a 450 x 550 mil ceramic LCC (ECA suffix) rated for operation from -55°C to 125°C.

Because this EPROM operates from a single 5V supply (in the read mode), it is ideal for use in microprocessor-based systems. One other supply (13V) is needed for programming. All programming signals are TTL level. This device is programmable by the SNAP! Pulse programming algorithm. The SNAP! Pulse programming algorithm uses a V_{PP} of 13V and a V_{CC} of 6.5V for a nominal programming time of four seconds. For programming outside the system, existing EPROM programmers can be used. Locations can be programmed singly, in blocks, or at random.

FUNCTIONAL BLOCK DIAGRAM*



* This symbol is in accordance with ANSI/IEEE std 91-1984 and IEC Publication 617-12.

OPERATION

The seven modes of operation for the SMJ27C256 are listed in Table 1. The read mode requires a single 5V supply. All inputs are TTL level except for V_{PP} during programming (13V for SNAP! Pulse), and (12V) on A9 for signature mode.

TABLE 1. OPERATION MODES

FUNCTION (PINS)	MODE*							
	READ	OUTPUT DISABLE	STANDBY	PROGRAMMING	VERIFY	PROGRAM INHIBIT	SIGNATURE MODE	
E\	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	
G\	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	X	V_{IL}	
V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{PP}	V_{PP}	V_{PP}	V_{CC}	
V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	
A9	X	X	X	X	X	X	V_{ID}	V_{ID}
A0	X	X	X	X	X	X	V_{IL}	V_{IH}
DQ0-DQ7	Data Out	High-Z	High-Z	Data In	Data Out	High-Z	CODE**	
							MFG	DEVICE
							97	04

NOTES:

* X can be V_{IL} or V_{IH}

** Die is Texas Instruments. User can program on benchtop programmer by selecting either TMS27C256 or SMJ27C256 from the device type selection menu.

READ/OUTPUT DISABLE

When the outputs of two or more SMJ27C256s are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the selected SMJ27C256, a low-level signal is applied to E\ and G\. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins DQ0 through DQ7.

LATCHUP IMMUNITY

Latchup immunity on the SMJ27C256 is a minimum of 250mA on all inputs and outputs. This feature provides latchup immunity beyond any potential transients at the printed circuit board level when the EPROM is interfaced to industry standard TTL or MOS logic devices. Input/output layout approach controls latchup without compromising performance or packing density.

POWER DOWN

Active I_{CC} supply current can be reduced from 25mA (SMJ27C256-15 through SMJ27C256-25) to 500µA (TTL-level inputs) or 300µA (CMOS-level inputs) by applying a high TTL/CMOS signal to the E\ pin. In this mode all outputs are in the high-impedance state.

ERASURE

Before programming, the SMJ27C256 is erased by exposing the chip through the transparent lid to a high-intensity ultra-violet light (wavelength 2537 Å). EPROM erasure before programming is necessary to ensure that all bits are in the logic-high state. Logic-lows are programmed into the desired locations. A programmed logic-low can be erased only by ultraviolet light. The recommended minimum exposure dose (UV intensity x exposure time) is 15W•s/cm^2. A typical 12mW/cm^2, filterless UV lamp erases the device in 21 minutes. The lamp should be located about 2.5cm above the chip during erasure. After erasure, all bits are in the high state. It should be noted that normal ambient light contains the correct wavelength for erasure; therefore, when using the SMJ27C256, the window should be covered with an opaque label.

SNAP! PULSE PROGRAMMING

The SMJ27C256 EPROM is programmed by using the SNAP! Pulse programming algorithm as illustrated by the flowchart in Figure 1. This algorithm programs the device in a nominal time of 4 seconds. Actual programming time varies as a function of the programmer used.

Data is presented in parallel (eight bits) on pins DQ0 to DQ7. Once addresses and data are stable, E\ is pulsed.

The SNAP! Pulse programming algorithm uses initial pulses of 100 microseconds (µs) followed by a byte-verification step to determine when the addressed byte has been successfully programmed. Up to ten 100µs pulses per byte are provided before a failure is recognized.

The programming mode is achieved when V_{PP} = 13V, V_{CC}= 6.5V, G\ = V_{IH}, and E\ = V_{IL}. More than one device can be programmed when the devices are connected in parallel. Locations can be programmed in any order. When the SNAP! Pulse programming routine is completed, all bits are verified with V_{CC} = V_{PP} = 5V.

PROGRAM INHIBIT

Programming can be inhibited by maintaining a high-level input on E\.

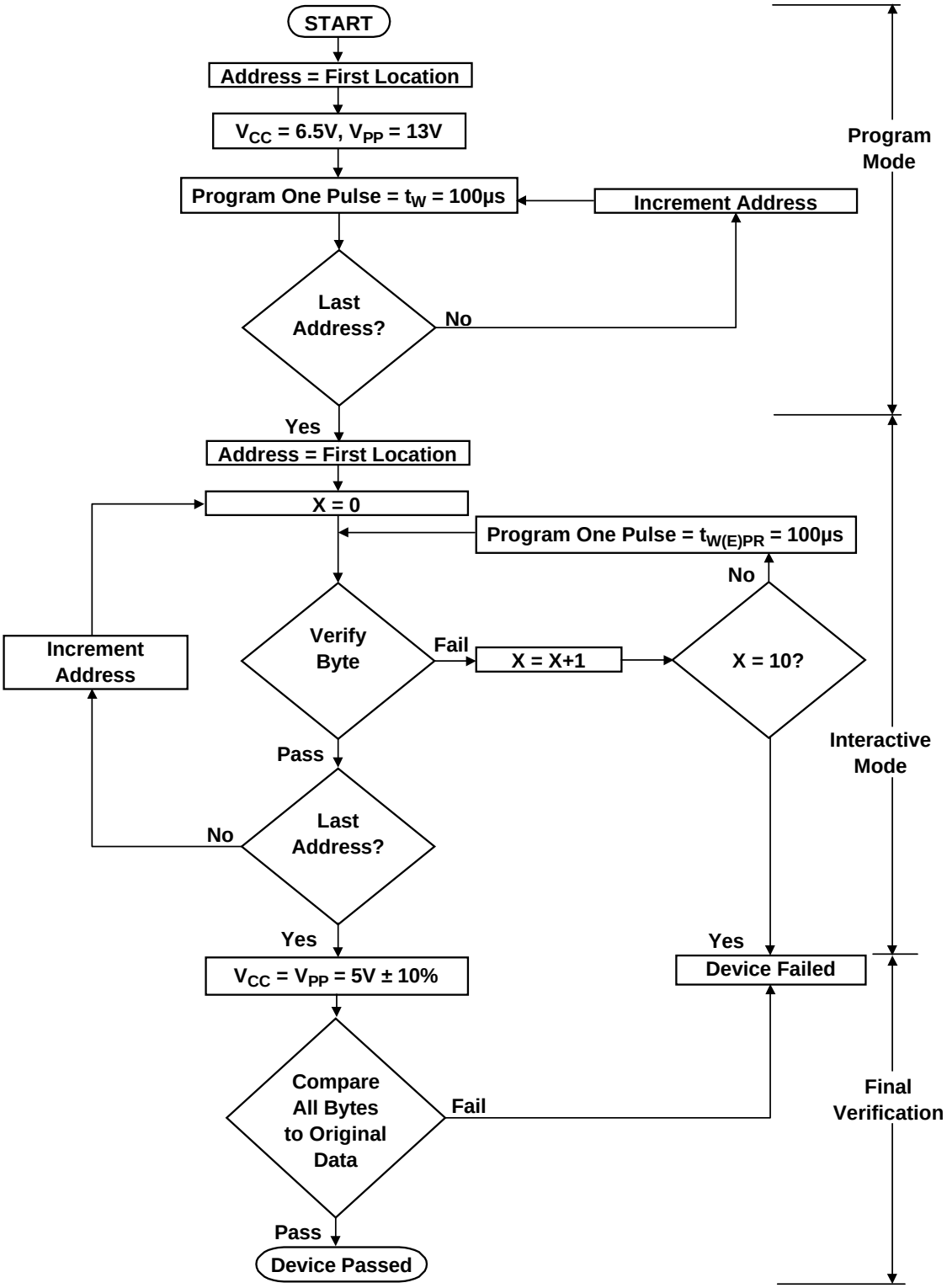
PROGRAM VERIFY

Programmed bits can be verified with V_{PP} = 13V when G\ = V_{IL}, and E\ = V_{IH}.

SIGNATURE MODE

The signature mode provides access to a binary code identifying the manufacturer and device type. This mode is activated when A9 is forced to 12V ±0.5V. Two identifier bytes are accessed by A0 (terminal 10); i.e., A0=V_{IL} accesses the manufacturer code, which is output on DQ0-DQ7; A0=V_{IH} accesses the device code, which is also output on DQ0-DQ7. All other addresses must be held at VIL. Each byte contains odd parity on bit DQ7. The manufacturer code for these devices is 97h and the device code is 04h.

FIGURE 1. SNAP! PULSE PROGRAMMING FLOW CHART



ABSOLUTE MAXIMUM RATINGS*

Supply Voltage Range, V_{CC}**.....-0.6V to +7.0V
Supply Voltage Range, V_{pp}**.....-0.6V to +14.0V
Input Voltage Range, All inputs except A9**..-0.6V to +6.5V
A9.....-0.6V to +13.5V
Output Voltage Range**.....-0.6V to V_{CC} +1V
Minimum Operating Free-air Temperature, T_A.....-55°C
Maximum Operating Case Temperature, T_C.....125°C
Storage Temperature Range, T_{stg}.....-65°C to 150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

** All voltage values are with respect to GND.

RECOMMENDED OPERATING CONDITIONS

				MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	Read Mode[1]		4.5	5	5.5	V
		SNAP! Pulse programming algorithm		6.25	6.5	6.75	V
V_{PP}	Supply Voltage	Read Mode[2]				V_{CC}-0.6	V
		SNAP! Pulse programming algorithm		12.75	13	13.25	V
V_{IH}	High-level input voltage		TTL inputs	2		V_{CC}+1	V
			CMOS inputs	V_{CC}-0.2		V_{CC}+1	V
V_{IL}	Low-level input voltage		TTL inputs	-0.5		0.8	V
			CMOS inputs	-0.5		0.2	V
V_{ID}	Voltage level on A9 for signature mode			11.5		13	V
T_A	Operating free-air temperature			-55			°C
T_C	Operating case temperature					+125	°C

NOTES:
1. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The deivce must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.
2. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC2} + I_{PP1}$.

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = -400µA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 2.1mA			0.4	V
I_I	Input current (leakage)		V_I = 0V to 5.5V			±1	µA
I_O	Output current (leakage)		V_O = 0V to V_{CC}			±1	µA
I_{PP1}	V_{PP} supply current		V_{PP} = V_{CC} = 5.5V			10	µA
I_{PP2}	V_{PP} supply current (during program pulse)[2]		V_{PP} = 13V		35	50	mA
I_{CC1}	V_{CC} supply current (standby)	TTL-Input Level	V_{CC} = 5.5V, E\=V_{IH}			500	µA
		CMOS-Input Level	V_{CC} = 5.5V, E\=V_{CC}			300	µA
I_{CC2}	V_{CC} supply current (active)	'27C256-15 '27C256-17 '27C256-20 '27C256-25	E\=V_{IL}, V_{CC}=5.5V t_{cycle} = minimum, outputs open		15	25	mA
I_{OS}	Output current (leakage)					100	mA

NOTES:
1. Typical values are at T_A=25°C and nominal voltages.
2. This parameter has been characterized at 25°C and is not tested.

CAPACITANCE OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, f = 1MHz*

PARAMETER		TEST CONDITIONS	TYP**	MAX	UNIT
C_i	Input capacitance	V_I = 0V	6	10	pF
C_o	Output capacitance	V_O = 0V	10	14	pF

* Capacitance measurements are made on a sample basis only.

** Typical values are at T_A = 25°C and nominal voltages.

SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE[1,2]

PARAMETER		TEST CONDITIONS[1, 2]	-15		-17		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	see Figure 2		150		170	ns
$t_{a(E)}$	Access time from E\			150		170	ns
$t_{en(G)R}$	Output enable time from G\			70		70	ns
t_{dis}	Disable time of output from G\ or E\, whichever occurs first[3]		0	55	0	55	ns
$t_{v(A)}$	Output data valid time after change of address, E\, or G\, whichever occurs first[3]		0		0		ns

PARAMETER		TEST CONDITIONS[1, 2]	-20		-25		-30		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	see Figure 2		200		250		300	ns
$t_{a(E)}$	Access time from E\			200		250		300	ns
$t_{en(G)R}$	Output enable time from G\			75		100		120	ns
t_{dis}	Disable time of output from G\ or E\, whichever occurs first[3]		0	60	0	60	0	105	ns
$t_{v(A)}$	Output data valid time after change of address, E\, or G\, whichever occurs first[3]		0		0		0		ns

NOTES:

1.Timing measurements are made at 2V for logic high and 0.8V for logic low (see figure 2).

2. Common test conditions apply for t_{dis} except during programming.

3. Value calculated from 0.5V delta to measured output level. This parameter is only sampled and not 100% tested.

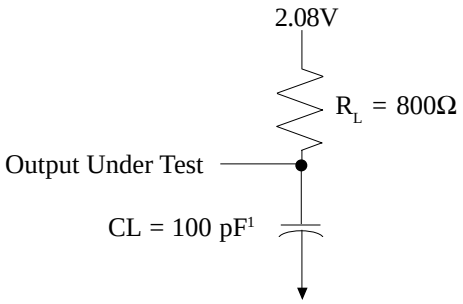
SWITCHING CHARACTERISTICS FOR PROGRAMMING: V_{CC} = 6.5V and V_{PP} = 13V (SNAP! Pulse), T_A = 25°C

PARAMETER		MIN	MAX	UNIT
$t_{dis(G)}$	Output disable time from G\	0	130	ns
$t_{en(G)W}$	Output enable time from G\		150	ns

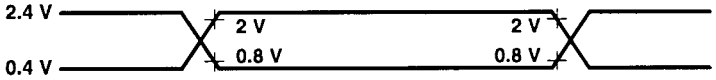
RECOMMENDED TIMING REQUIREMENTS FOR PROGRAMMING: V_{CC} = 6.5 and V_{PP} = 13 (SNAP! Pulse), T_A = 25°C (See Figure 2)

		MIN	TYP	MAX	UNIT
$t_{h(A)}$	Hold Time, Address	0			µs
$t_{h(D)}$	Hold Time, Data	2			µs
$t_{w(E)PR}$	Pulse Duration, Initial Program	95	100	105	µs
$t_{su(A)}$	Setup Time, Address	2			µs
$t_{su(G)}$	Setup Time, G\	2			µs
$t_{su(E)}$	Setup Time, E\	2			µs
$t_{su(D)}$	Setup Time, Data	2			µs
$t_{su(VPP)}$	Setup Time, V_{PP}	2			µs
$t_{su(VCC)}$	Setup Time, V_{CC}	2			µs

PARAMETER MEASUREMENT INFORMATION



NOTES:
1. C_L includes probe and fixture capacitance.



The AC testing inputs are driven at 2.4V for logic high and 0.4V for logic low. Timing measurements are made at 2V for logic high and 0.8V for logic low for both inputs and outputs.

FIGURE 2. LOAD CIRCUIT AND VOLTAGE WAVEFORMS

FIGURE 3. READ-CYCLE TIMING

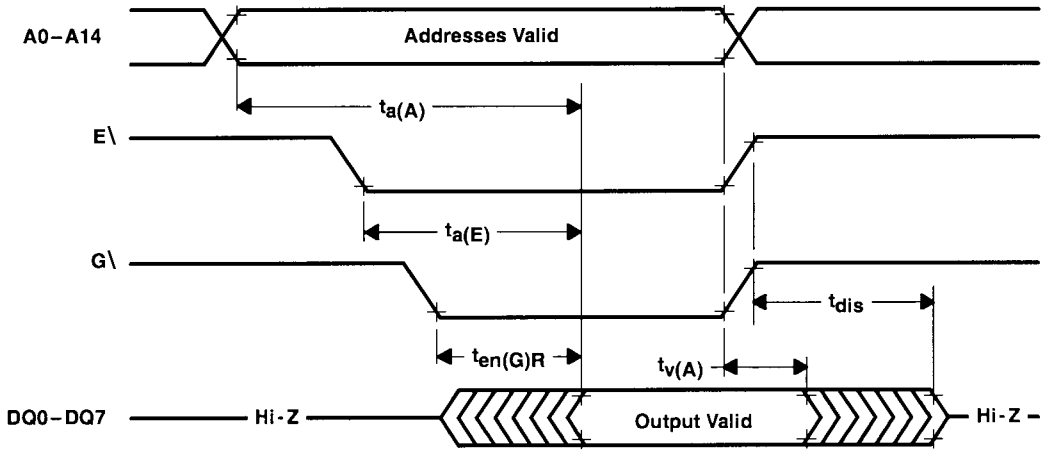
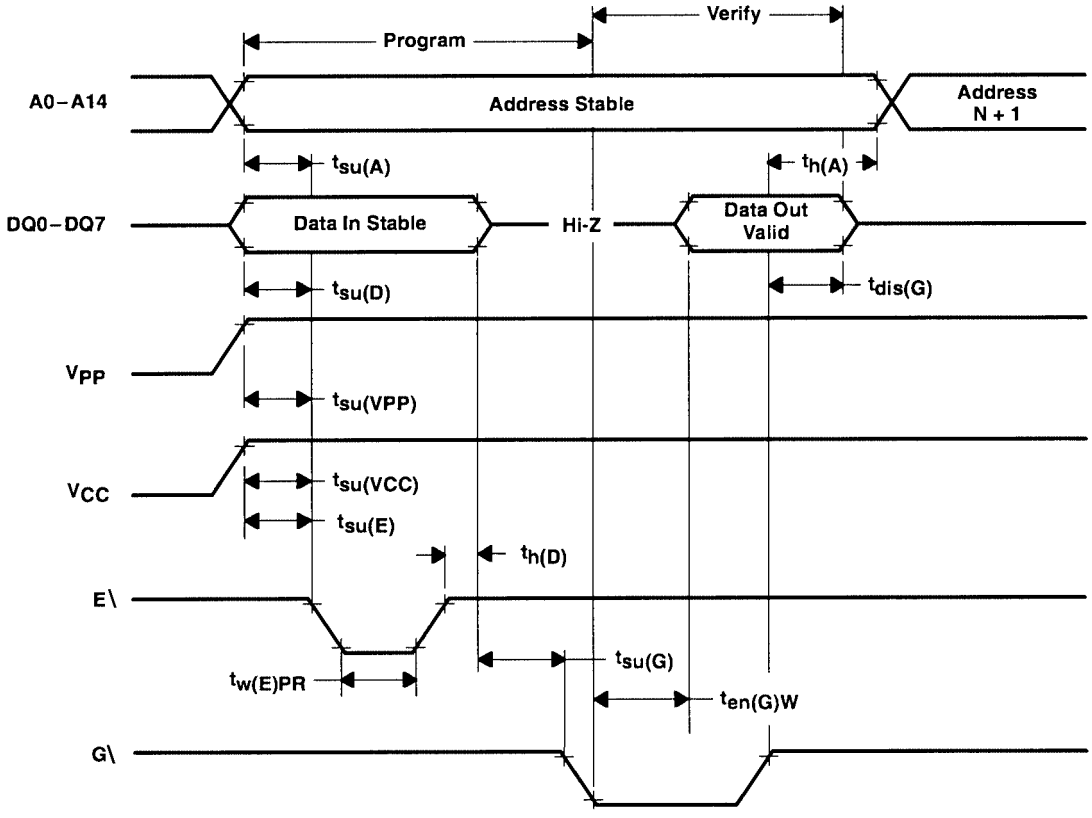
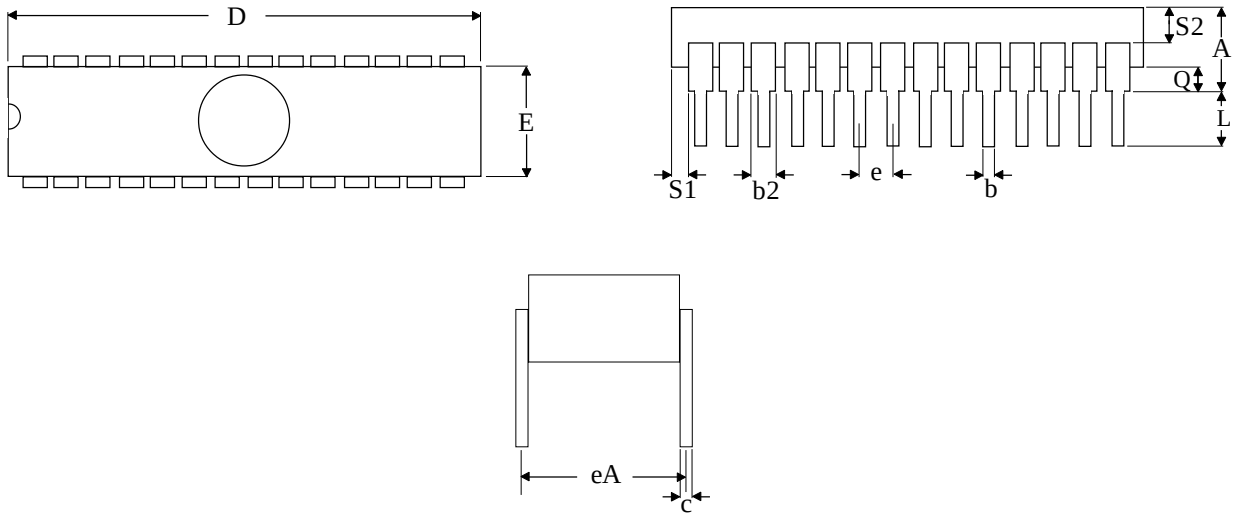


FIGURE 4. PROGRAM-CYCLE TIMING (SNAP! PULSE PROGRAMMING)



MECHANICAL DEFINITION*

ASI Case #110 (Package Designator J)
SMD 5962-86063, Case Outline X



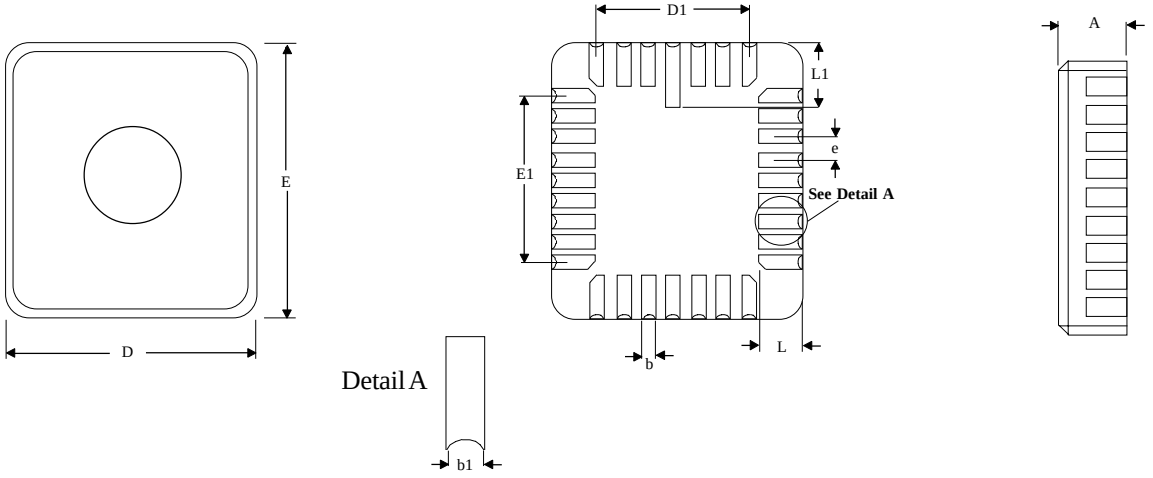
SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	---	0.232
b	0.014	0.026
b2	0.045	0.065
c	0.008	0.018
D	---	1.490
E	0.500	0.610
eA	0.600 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	---
S2	0.005	---

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

All measurements are in inches.

MECHANICAL DEFINITIONS*

ASI Case #208 (Package Designator ECA)
SMD 5962-86063, Case Outline Y



SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.060	0.120
b	0.022	0.028
b1	0.006	0.022
D	0.442	0.458
D1	0.300 BSC	
E	0.540	0.560
E1	0.400 BSC	
e	0.050 BSC	
L	0.045	0.055
L1	0.075	0.095

NOTE: *These dimensions are per the SMD. ASI's package dimensional limits may differ, but they will be within the SMD limits.*

All measurements are in inches.

ORDERING INFORMATION

EXAMPLE: SMJ27C256-30JM

Device Number	Speed ns	Package Type	Operating Temp.	Available Processes
SMJ27C256	-15	J	*	+
SMJ27C256	-17	J	*	+
SMJ27C256	-20	J	*	+
SMJ27C256	-25	J	*	+
SMJ27C256	-30	J	*	+

EXAMPLE: AS27C256-15ECAM/Q

Device Number	Speed ns	Package Type	Operating Temp.	Available Processes
AS27C256	-15	ECA	*	#
AS27C256	-17	ECA	*	#
AS27C256	-20	ECA	*	#
AS27C256	-25	ECA	*	#
AS27C256	-30	ECA	*	#

NOTES:

+ SMJ prefix, MIL-STD-883C processing
  SM prefix, commercial processing
  AS prefix, commercial or MIL-STD-883C processing
  (see note #)

*OPERATING TEMPERATURE

M = Extended Temperature Range -55°C to +125°C
I = Industrial Temperature Range -40°C to +85°C

AVAILABLE PROCESSES

/Q = For "AS" prefix part numbers only, indicates that part is processed to MIL-STD-883C.

Blank = For SMJ prefix part numbers, the /Q suffix is not used, as the SMJ prefix indicates MIL-STD-883C processing. Also blank for AS prefix part numbers indicating commercially (non MIL-STD-883C) processed parts.

ASI TO DSCC PART NUMBER CROSS REFERENCE*

ASI Package Designator J

TI Part #**	SMD Part #
SMJ27C256-15JM	5962-8606305XA
SMJ27C256-17JM	5962-8606304XA
SMJ27C256-20JM	5962-8606301XA
SMJ27C256-25JM	5962-8606302XA
SMJ27C256-30JM	5962-8606303XA

ASI Package Designator J

TI Part #**	SMD Part #
AS27C256-15ECAM/Q	5962-8606305YA
AS27C256-17ECAM/Q	5962-8606304YA
AS27C256-20ECAM/Q	5962-8606301YA
AS27C256-25ECAM/Q	5962-8606302YA
AS27C256-30ECAM/Q	5962-8606303YA

** ASI part number is for reference only. Orders received referencing the SMD part number will be processed per the SMD.*
*** Parts are listed on SMD under the old Texas Instruments part number. ASI purchased this product line in November of 1999.*