SL1521 Limiting R.F. Amplifier
SL1522 Dual Limiting R.F. Amplifiers (Parallel)
SL1523 Dual Limiting R.F. Amplifiers (Series)

DESCRIPTION

The **SL1521** A, B and C are wideband amplifiers intended for use in successive detection logarithmic I.F. strips operating at center frequencies up to 200MHz. The typical midband voltage gain of the SL1521 is 12 dB, and the A, B and C versions differ mainly in the tolerance of voltage gain.

The **SL1522** is a wideband amplifier intended for use as the first stage of a successive detection logarithmic I.F. strip, and operates at up to 200MHz. Consisting of a resistor network and two SL1521,s, the SL1522 improves the logging accuracy in the -20 to 0 dBm input range by summing additional video current from another stage.

The **SL1523** consists of two SL1521,s in series, and is intended to reduce the package count and improve the packaging density in logarithmic strips at frequencies up to 200 MHz.

ABSOLUTE MAXIMUM RATINGS (Non-Simultaneous)

The absolute maximum ratings are limiting values above which operating life may be shortened or satisfactory performance may be impaired.

Storage temperature range	−55°C to +175°C
Operating temperature	−55°C to +125°C
Chip operating temperature:	
Chip-to-ambient thermal resistance	300°C/W (SL1522,SL1523) 250°C/W (SL1521)
Chip-to-case thermal resistance	95° C/W (SL1522, SL1523) 80°C/W (SL1521)
Maximum instantaneous voltage at video output	+12 V
Supply voltage	+ 9 V

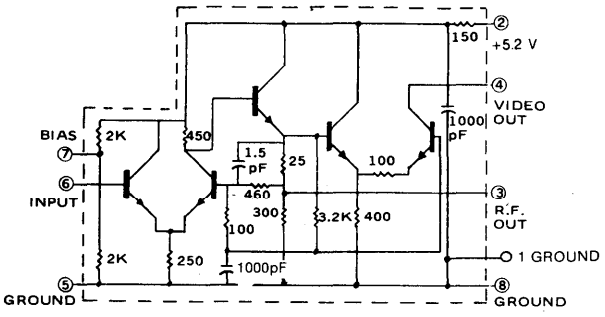


Fig 1: SL1521 circuit diagram

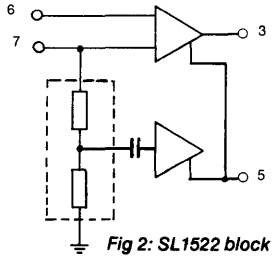


Fig 2: SL1522 block diagram

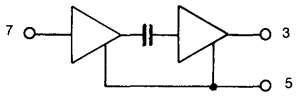


Fig 3: SL1523 block diagram

Electrical Characteristics

Test Conditions
Temperature = 22° ± 2°c
Supply voltage = +5.2V

		SL1521				
Characteristic		A	B	C	Units	Test Conditions
/oltage gain:	(Min)	11.5	11.2	10.8	dB	F=120MHz, 7mV rms
	(Max)	12.5	12.8	13.1	dB	input, 50 ohms source
						8pF load + 500 ohms
Voltage gain:	(Min)	11.2	11.0	10.6	dB	F=160MHz, 7mV rms
	(Max)	12.8	13.0	13.4	dB	input, 50 ohms source
						8pF load + 500 ohms
Upper cut-off	(Min)	315	315	300	MHz	50 ohms source
frequency	(Max)	350	350	350	MHz	50 phms source
Lower cut-off	(Min)	6	6	6	MHz	50 ohms source
frequency	(Max)	10	10	10	MHz	50 ohms source
Propagation delay	**(Typ)	0.6	0.6	0.6	n sec	
Maximum rectified video	(Min)	0.95	0.90	0.90	mA	F=120MHz, 0.5 V rms
output current	(Max)	1.05	1.10	1.20	mA	input, 8pF load + 500 ohms
Variation of gain with supply voltage	**(Typ)	1.0	1.0	1.0	dB/V	
Variation of maximum rectified output current with supply voltage	**(Typ)	30	30	30	%/V	
Maximum inoput signal before overload	* **(Typ)	1.5	1.5	1.5	V rms	
Noise figure	**(Typ)	9.5	9.5	9.5	dB	F=120MHz, source resistance 50Ω
Supply current	(Min)	10.0	10.0	10.0	mA	
	(Typ)	15.0	15.0	15.0	mA	
	(Max)	20.0	20.0	20.0	mA	
Maximum R.F. output voltage	**(Typ)	1.0	1.0	1.0	Vp-p	F=120 MHz

NOTE: * Overload occurs when the input signal reaches a level sufficient to forward bias the base collector junction on T1 on peak.

** All typical values are given for design information, and are not 100% tested.

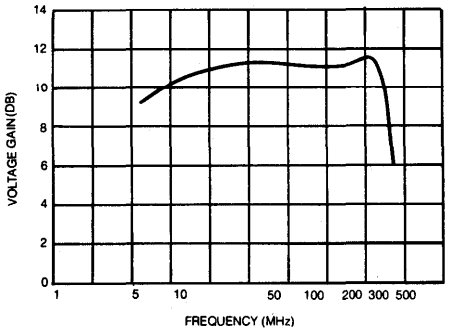


Fig 4: SL1521 Voltage gain vs. frequency.

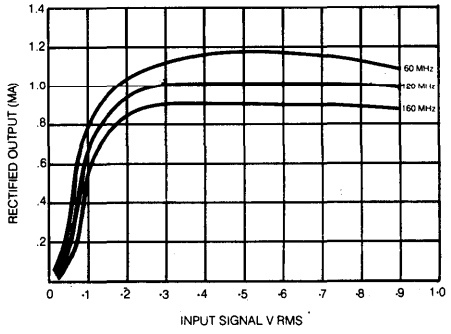


Fig 5: SL1521 rectified output current vs. input signal

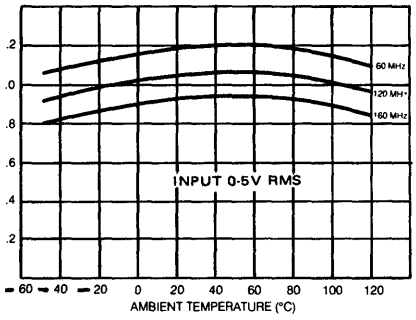
Electrical Characteristics

Test Conditions
Temperature = 22° ± 2°c
Supply voltage = +5.2V

Characteristic		SL1522 A	SL1522 B	SL1522 C	Units	Test Conditions
Voltage gain:	(Min)	11.2	10.8	10.2	dB	F=120MHz, 7mV rms
	(Max)	12.8	13.1	13.9	dB	input, 50 ohms source 8pF load + 500 ohms
Voltage gain:	(Min)	11.0	10.6	10.0	dB	F=160MHz, 7mV rms
	(Max)	13.0	13.4	14.3	dB	input, 50 ohms source 8pF load + 500 ohms
Upper cut-off frequency	(Min)	315	315	300	MHz	50 ohms source
	(Max)	350	350	350	MHz	50 ohms source
Lower cut-off frequency	(Min)	6	6	6	MHz	50 ohms source
	(Max)	10	10	10	MHz	50 ohms source
Propagation delay	**(Typ)	0.6	0.6	0.6	n sec	
Maximum rectified video output current	(Min)	1.6	1.5	1.4	mA	F=120MHz, 0.5 V rms
	(Max)	1.8	1.9	2.0	mA	input, 8pF load + 500 ohms
Variation of gain with supply voltage	**(Typ)	2.0	2.0	2.0	dB/V	
Variation of maximum rectified output current with supply voltage	**(Typ)	30	30	30	%/V	
Maximum input signal before overload	* **(Typ)	1.5	1.5	1.5	v rms	
Noise figure	**(Typ)	9.5	9.5	9.5	dB	F=120MHz, source resistance 50Ω
Supply current	(Min)	20	20	20	mA	
	(Typ)	30	30	30	mA	
	(Max)	40	40	40	mA	
Maximum R.F. output voltage	**(Typ)	1.0	1.0	1.0	Vp-p	F=120MHz

NOTE: * Overload occurs when the input signal reaches a level sufficient to forward bias the base collector junction on T1 on peak.

** All typical values are given for design information, and are not 100% tested.



6: SL1521 maximum rectified output current vs. temperature

ERATING NOTES

The amplifiers are intended for use directly ıpled, as shown in Fig. 8 (This figure shows the -5 version).

The seventh stage in an untuned cascade will giving virtually full output on noise.

Noise may be reduced by inserting a single ed circuit between in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The choice of network is also controlled by the need to avoid distorting the logarithmic law; the network must give unity voltage transfer at resonsnce. A suitable network is shown in Fig. 9. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit.

A simple capacitor may not be suitable for decoupling the output line if many stages and fast rise times are required.

Values of positive supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in hihg frequency tuned cascades.

	Number of Stages			
	6 or more	5	4	3
Minimum capacitance	30nF	10nF	3nF	1nF

The amplifiers have been provided with two earth leads to avoid the introduction of common earth lead inductance between input and output circuits.

Electrical Characteristics

Test Conditions
Temperature = 22° ± 2°c
Supply voltage = +5.2V

Characteristic		SL1523 A	SL1523 B	SL1523 C	Units	Test Conditions
Voltage gain:	(Min)	23	22	21	dB	F=120MHz, 7mV rms
	(Max)	25	26	27	dB	input, 50 ohms source 8pF load + 500 ohms
Voltage gain:	(Min)	22	21	20	dB	F=160MHz, 7mV rms
	(Max)	25	26	27	dB	input, 50 ohms source 8pF load + 500 ohms
Upper cut-off frequency	(Min)	230	230	230	MHz	50 ohms source
	(Max)	280	280	280	MHz	50 ohms source
Lower cut-off frequency	(Min)	6	6	6	MHz	50 ohms source
	(Max)	10	10	10	MHz	50 ohms source
Propagation delay	**(Typ)	0.6	0.6	0.6	n sec	
Maximum rectified video output current	(Min)	1.9	1.8	1.7	mA	F=120MHz, 0.5 V rms
	(Max)	2.1	2.2	2.3	mA	input, 8pF load + 500 ohms
Variation of gain with supply voltage	**(Typ)	2.0	2.0	2.0	dB/V	
Variation of maximum rectified output current with supply voltage	**(Typ)	30	30	30	%/V	
Maximum input signal before overload	* **(Typ)	1.5	1.5	1.5	V rms	
Noise figure	**(Typ)	9.5	9.5	9.5	dB	F=120MHz, source resistance 50Ω
Supply current	(Min)	20	20	20	mA	
	(Typ)	30	30	30	mA	
	(Max)	40	40	40	mA	
Maximum R.F. output voltage	**(Typ)	1.0	1.0	1.0	Vp-p	F=120MHz

NOTE: * Overload occurs when the input signal reaches a level sufficient to forward bias the base collector junction on T1 on peak.
** All typical values are given for design information, and are not 100% tested.

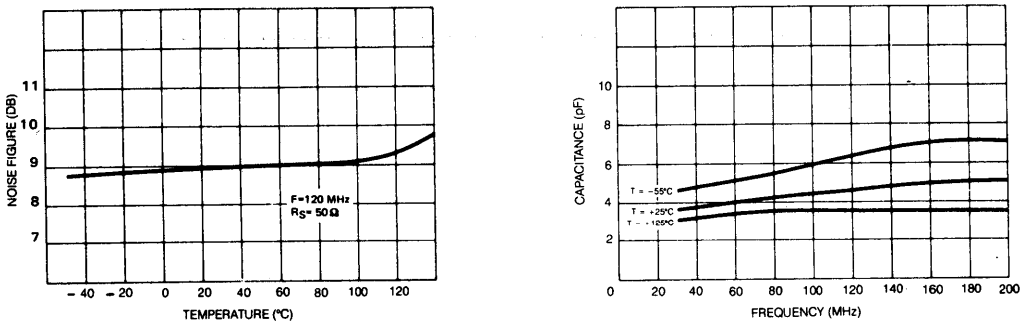


Fig 7: SL1521 input admittance with open-circuit output.

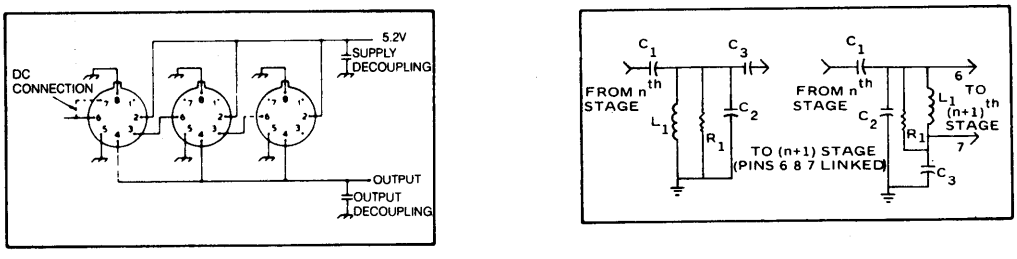


Fig. 9: Interstage filter designs (including damping resistors)