SED1560 Series

■ DESCRIPTION

The SED1560 Series are intelligent CMOS LCD driver-controllers with the ability to drive alphanumeric and graphic displays. The SED1560 Series communicates with a high-speed microprocessor, such as the Intel 80XX family or the Motorola 68XX family, through either a serial or an 8-bit parallel interface. It stores the data sent from the microprocessor in the built-in display data RAM (166 × 65 bits) and generates an LCD drive signal. These devices incorporate an internal DC/DC converter to generate the negative voltage needed for LCD contrast. The controllers feature software contrast adjustment by command setting.

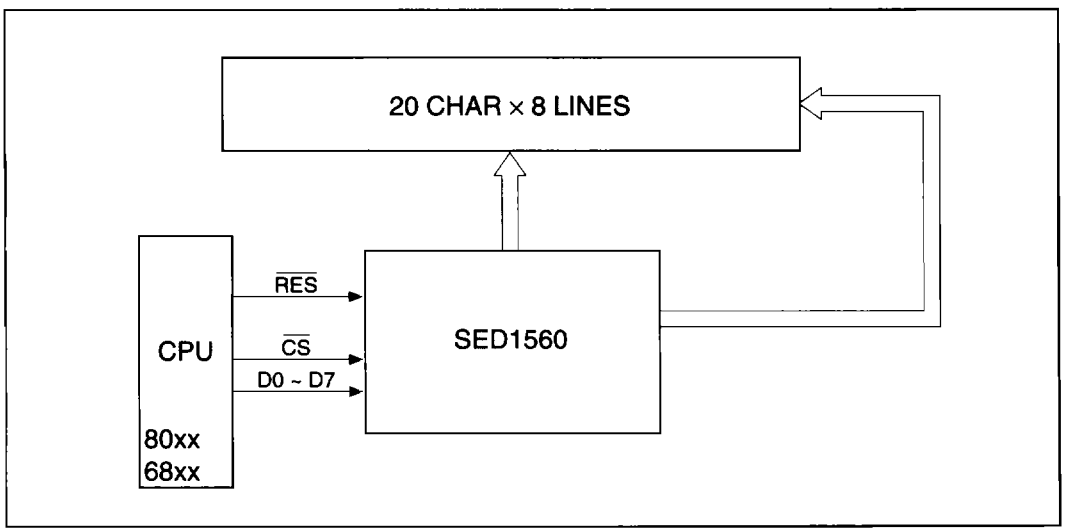
The three different versions of the SED1560 Series support the following duty ratios and display sizes:

Model	Duty Ratio	SEG × COM
SED1560	1/65, 1/64, 1/49, 1/48	102 × 65
SED1561	1/33, 1/32, 1/25, 1/24	134 × 33
SED1562	1/17, 1/16	150 × 17

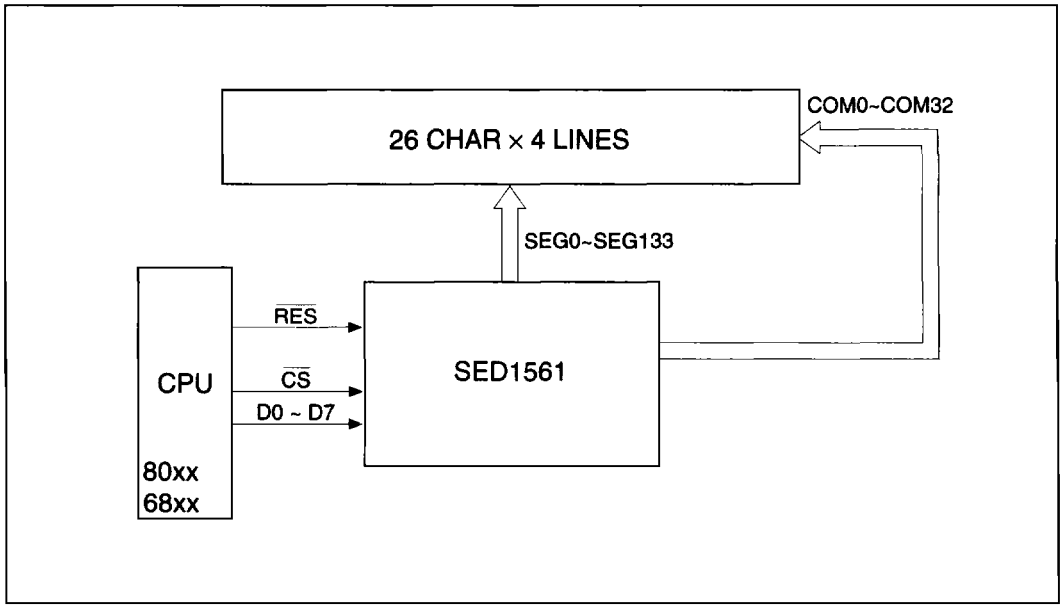
■ FEATURES

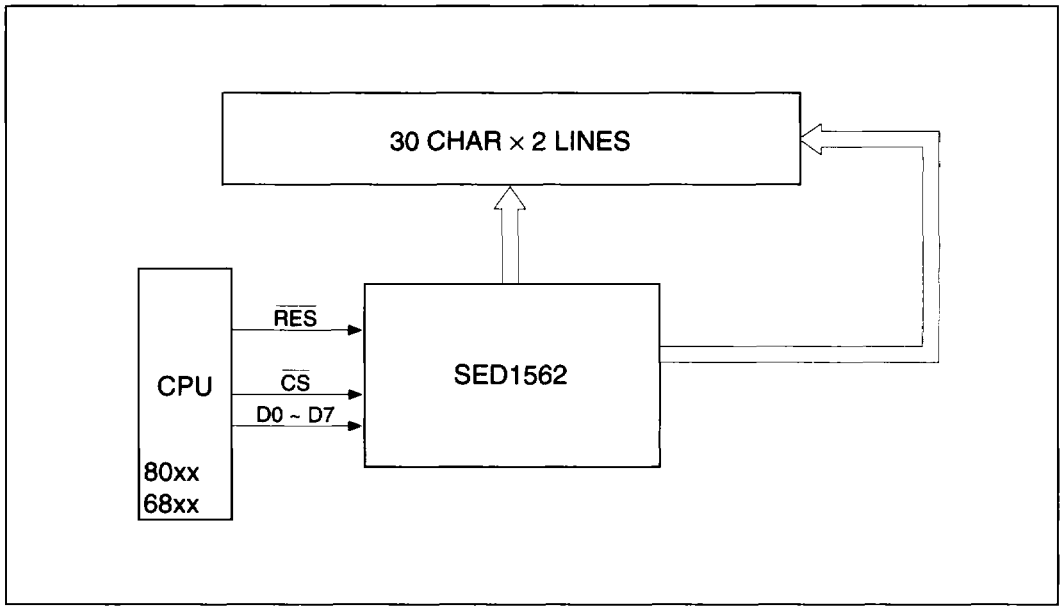
- Low-power operation: 8 µA @ 1 kHz, 6V LCD
- 350 µA current consumption during CPU access @ 200 kHz
- Direct interface to both 80XX and 68XX, 5 MHz, zero wait-state
- On-chip display data RAM (166 × 65 bits)
- On-chip DC/DC converter for LCD voltage
- On-chip voltage regulator and low-power voltage follower
- –.17% / °C temperature gradient
- On-chip oscillator with external resistor
- 32 levels of contrast adjustment by software
- Supports master/slave operation
- Selectable output configuration
- 2.4V to 6.0V supply voltage
- 3.5V to 16V LCD voltage
- Package: TAB ..... (TOB — 2-sided)
  (TQA — 4-sided)

■ SYSTEM BLOCK DIAGRAMS

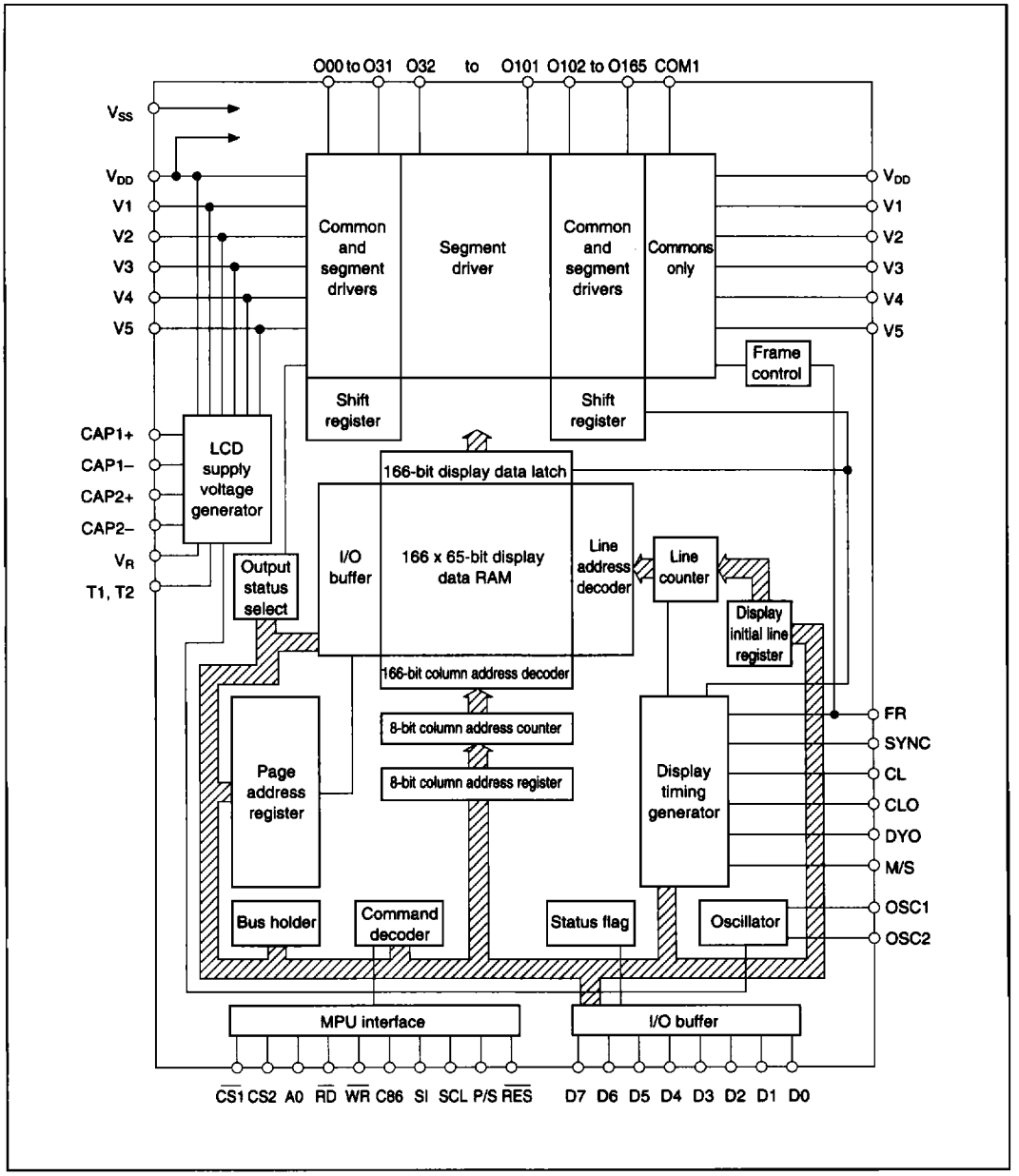


■ **SYSTEM BLOCK DIAGRAMS (continued)**





■ BLOCK DIAGRAM



■ PIN DESCRIPTION

● Power Supply

<table>
<tr><th>Number of Pins</th><th>I/O</th><th>Name</th><th>Description</th></tr>
<tr><td>2</td><td>Supply</td><td>VDD</td><td>Common to MPU power supply pin VCC</td></tr>
<tr><td>2</td><td>Supply</td><td>VSS</td><td>Ground</td></tr>
<tr><td>11</td><td>Supply LCD voltage</td><td>V1 to V5</td><td>LCD driver supply voltages. The voltage determined by the LCD cell is impedance-converted by a resistive divider or an operational amplifier for application. Voltage levels are based on VDD. The voltages must satisfy the following relationship:
VDD ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5
Master mode select: bias voltages are generated on-chip.
<table>
<tr><th></th><th>SED1560</th><th>SED1561</th><th>SED1562</th></tr>
<tr><td>V1</td><td>1/9 V5</td><td>1/7 V5</td><td>1/5 V5</td></tr>
<tr><td>V2</td><td>2/9 V5</td><td>2/7 V5</td><td>2/5 V5</td></tr>
<tr><td>V3</td><td>7/9 V5</td><td>5/7 V5</td><td>3/5 V5</td></tr>
<tr><td>V4</td><td>8/9 V5</td><td>6/7 V5</td><td>4/5 V5</td></tr>
</table>
</td></tr>
</table>

● LCD Driver Power Supplies

<table>
<tr><th>Number of Pins</th><th>I/O</th><th>Name</th><th>Description</th></tr>
<tr><td>1</td><td>O</td><td>CAP1+</td><td>DC/DC voltage converter capacitor 1 positive connection</td></tr>
<tr><td>1</td><td>O</td><td>CAP1−</td><td>DC/DC voltage converter capacitor 1 negative connection</td></tr>
<tr><td>1</td><td>O</td><td>CAP2+</td><td>DC/DC voltage converter capacitor 2 positive connection</td></tr>
<tr><td>1</td><td>O</td><td>CAP2−</td><td>DC/DC voltage converter capacitor 2 negative connection</td></tr>
<tr><td>1</td><td>O</td><td>VOUT</td><td>DC/DC voltage converter output</td></tr>
<tr><td>1</td><td>I</td><td>VR</td><td>Voltage adjustment pin. Applies voltage between VDD and V5 using a resistive divider.</td></tr>
<tr><td>2</td><td>I</td><td>T1, T2</td><td>Liquid crystal power control terminals
<table>
<tr><th>T1</th><th>T2</th><th>Boosting Circuit</th><th>Voltage Regulation Circuit</th><th>V/F Circuit</th></tr>
<tr><td>L</td><td>L</td><td>Valid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>L</td><td>H</td><td>Valid</td><td>Valid</td><td>Valid*</td></tr>
<tr><td>H</td><td>L</td><td>Invalid</td><td>Valid</td><td>Valid</td></tr>
<tr><td>H</td><td>H</td><td>Invalid</td><td>Invalid</td><td>Valid</td></tr>
</table>
Note: * V/F circuit current capacity enhancement</td></tr>
</table>

● Microprocessor Interface

<table>
<tr><th>Number of Pins</th><th>I/O</th><th>Name</th><th>Description</th></tr>
<tr><td>8</td><td>I/O</td><td>D0 to D7</td><td>Data is transferred between the controller and MPU via these pins</td></tr>
<tr><td>1</td><td>I</td><td>A0</td><td>Control/display data flag input. This is connected to the LSB of the microprocessor address bus.
• When LOW, the data on D0 to D7 is command data
• When HIGH, the data on D0 to D7 is display data</td></tr>
<tr><td>1</td><td>I</td><td>$\overline{RES}$</td><td>Reset input. Setting this pin low initializes the SED156X.</td></tr>
<tr><td>2</td><td>I</td><td>$\overline{CS1}$,
CS2</td><td>Chip select inputs. Data input/output is enabled when CS1 is LOW and CS2 is HIGH.</td></tr>
<tr><td>1</td><td>I</td><td>$\overline{RD}$</td><td>Read enable input. See note 1.</td></tr>
<tr><td>1</td><td>I</td><td>$\overline{WR}$</td><td>Write enable input. See note 2.</td></tr>
<tr><td>1</td><td>I</td><td>C86</td><td>Microprocessor interface select input.
• LOW when interfacing to 8080-series
• HIGH when interfacing to 6800-series</td></tr>
<tr><td>1</td><td>I</td><td>SI</td><td>Serial data input</td></tr>
<tr><td>1</td><td>I</td><td>SCL</td><td>Serial clock input. Data is read on the rising edge of SCL and converted to 8-bit parallel data.</td></tr>
<tr><td>1</td><td>I</td><td>P/S</td><td>Parallel/serial data input select
<table>
<tr><th>P/S</th><th>Operating Mode</th><th>Chip Select</th><th>Data/ com-mand</th><th>Data I/O</th><th>Read/ write</th><th>Serial Clock</th></tr>
<tr><td>HIGH</td><td>Parallel</td><td>$\overline{CS1}$, CS2</td><td>A0</td><td>D0 to D7</td><td>RD, WR</td><td>—</td></tr>
<tr><td>LOW</td><td>Serial</td><td>$\overline{CS1}$, CS2</td><td>A0</td><td>SI</td><td>Write only</td><td>SCL</td></tr>
</table>
In serial mode, data cannot be read from the RAM, and D0 to D7, HZ, $\overline{RD}$ and $\overline{WR}$ must be HIGH or LOW. In parallel mode, SI and SCL must be HIGH or LOW.</td></tr>
</table>

Notes:

1. When interfacing to 8080-series microprocessors, $\overline{RD}$ is active-LOW. When interfacing to 6800-series microprocessors, they are active-HIGH.
2. When interfacing to 8080-series microprocessors, $\overline{WR}$ is active-LOW. When interfacing to 6800-series microprocessors, read mode is selected when $\overline{WR}$ is HIGH, and write mode is selected when $\overline{WR}$ is LOW.

● **Oscillator and Display Timing Control**

<table>
<tr><th>Number of Pins</th><th>I/O</th><th>Name</th><th>Description</th></tr>
<tr><td>2</td><td>I</td><td>OSC1</td><td>Using internal oscillator when M/S = "H", connect resistor Rf to the OSC1 and OSC2 pins. The OSC2 pin is used for output of the oscillator amplifier.</td></tr>
<tr><td>2</td><td>I/O</td><td>OSC2</td><td>When M/S = "L": the OSC2 pin is used for input of oscillation signal. The OSC1 pin should be left open. Fix the CL pin to the VSS level when using the internal oscillator circuit as the display clock.</td></tr>
<tr><td>1</td><td>I</td><td>CL</td><td>Display clock input. The line counter increments on the rising edge of CL, and the display pattern is output on the falling edge. When using the external display clock, OSC1 = "H", OSC2 = "L", and reset this LSI by $\overline{RES}$ pin.</td></tr>
<tr><td>1</td><td>O</td><td>CLO</td><td>Display clock output. When using the internal oscillator, the clock signal is output on this pin. Connect CLO to YSCL on the common driver.</td></tr>
<tr><td>1</td><td>I</td><td>M/S</td><td>Master/slave select input. Master produces signals for display, and slave receives them. This is for display synchronization.
<table>
<tr><th>Device</th><th>M/S</th><th>Operating Mode</th><th>Internal Oscillator</th><th>Power Supply</th><th>FR</th><th>SYNC</th><th>OSC1</th><th>OSC2</th><th>DYO</th></tr>
<tr><td rowspan="2">156X</td><td>LOW</td><td>Slave</td><td>OFF</td><td>OFF</td><td>I</td><td>I</td><td>Open</td><td>I</td><td>O</td></tr>
<tr><td>HIGH</td><td>Master</td><td>ON</td><td>ON</td><td>O</td><td>O</td><td>I</td><td>O</td><td>O</td></tr>
</table>
Note: I = input mode O = output mode</td></tr>
<tr><td>1</td><td>I/O</td><td>FR</td><td>LCD AC drive signal input/output. Output is selected when M/S is HIGH, and input is selected when M/S is LOW.</td></tr>
<tr><td>1</td><td>I/O</td><td>SYNC</td><td>Display sync input/output. Output is selected when M/S is HIGH, and input is selected when M/S is LOW.</td></tr>
<tr><td>1</td><td>O</td><td>DYO</td><td>Start-up output for common driver. Connect to DIO of the common driver, such as the SED1630.</td></tr>
</table>

* SED1630 has a DIO input.

● **LCD Driver Outputs**

<table>
<tr><th>Number of Pins</th><th>I/O</th><th>Name</th><th>Description</th></tr>
<tr><td>166</td><td>O</td><td>O0 to O165</td><td>LCD driver outputs. O0 to O31 and O102 to O165 are selectable segment or common outputs, determined by a selection command. O32 to O101 are segment outputs only.
For segment outputs, the ON voltage level is given as shown in the following table:
<table>
<tr><th rowspan="2">RAM Data</th><th rowspan="2">FR</th><th colspan="2">LCD ON Voltage</th></tr>
<tr><th>Normal Display</th><th>Inverse Display</th></tr>
<tr><td rowspan="2">LOW</td><td>LOW</td><td>V3</td><td>V5</td></tr>
<tr><td>HIGH</td><td>V2</td><td>VDD</td></tr>
<tr><td rowspan="2">HIGH</td><td>LOW</td><td>V5</td><td>V3</td></tr>
<tr><td>HIGH</td><td>VDD</td><td>V2</td></tr>
</table>
For common outputs, the ON voltage is given as shown in the following table:
<table>
<tr><th>Scan Data</th><th>FR</th><th>LCD ON Voltage</th></tr>
<tr><td rowspan="2">LOW</td><td>LOW</td><td>V4</td></tr>
<tr><td>HIGH</td><td>V1</td></tr>
<tr><td rowspan="2">HIGH</td><td>LOW</td><td>VDD</td></tr>
<tr><td>HIGH</td><td>V5</td></tr>
</table></td></tr>
<tr><td>1</td><td>O</td><td>COM1</td><td>LCD driver common output. Common outputs when the “DUTY + 1” command is executed are as follows:
<table>
<tr><th>Device</th><th>“DUTY + 1” ON</th><th>“DUTY + 1” OFF</th></tr>
<tr><td>SED1560</td><td>COM64, COM48</td><td>V1 or V4</td></tr>
<tr><td>SED1561</td><td>COM32, COM24</td><td>V1 or V4</td></tr>
<tr><td>SED1562</td><td>COM16</td><td>V1 or V4</td></tr>
</table>
Common output special for the indicator.</td></tr>
</table>

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{SS}	−7.0 to 0.03	V
		−6.0 to 0.3 (when triple voltage conversion)	
Driver supply voltage range (1)	V5	−18.0 to 0.3	V
Driver supply voltage range (2)	V1, V2, V3, V4	V5 to 0.3	V
Input voltage range	V_{IN}	V_{SS} − 0.3 to 0.3	V
Output voltage range	V0	V_{SS} − 0.3 to 0.3	V
Operating temperature range	T_{opr}	−30 to 85	°C
Storage temperature range (TCP)	T_{str}	−55 to 125	°C

Notes:

1. The voltages shown are based on V_{DD} = 0V.
2. Always keep the condition $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ for voltages V1, V2, V3 and V4.
3. If devices are used over the absolute maximum rating, the LSIs may be destroyed permanently. It is desirable to use them under the electrical characteristic conditions for general operation. Otherwise, a malfunction of the LSI may be caused and LSI reliability may be affected.
4. For operating temperatures below −30°C, please consult an S-MOS engineer.

■ DC CHARACTERISTICS

V_{DD} = 0V, V_{SS} = −5 ± 10%, T_a = −30 to +85°C unless otherwise noted.

Parameter		Symbol	Condition		Min	Typ	Max	Unit	Pin
Power voltage (1)	Recommended operation	Vss			−5.5	−5.0	−4.5	V	Vss
	Operational				−6.0	—	−2.4		Vss *1
Operating voltage (2)	Operational	V5			−16.0	—	−3.5	V	V5 *2
	Operational	V1, V2			0.4 × V5	—	V_{DD}	V	V1, V2
	Operational	V3, V4			V5	—	0.6 × V5	V	V3, V4
High-level input voltage		V_{IHC1}			0.3 × Vss	—	V_{DD}	V	*3
		V_{IHC2}			0.15 × Vss	—	V_{DD}	V	*4
		V_{IHC1}	Vss = −2.7V		0.2 × Vss	—	V_{DD}	V	*3
		V_{IHC2}	Vss = −2.7V		0.15 × Vss	—	V_{DD}	V	*4
Low-level input voltage		V_{ILC1}			Vss	—	0.7 × Vss	V	*3
		V_{ILC2}			Vss	—	0.85 × Vss	V	*4
		V_{ILC1}	Vss = −2.7V		Vss	—	0.8 × Vss	V	*3
		V_{ILC2}	Vss = −2.7V		Vss	—	0.85 × Vss	V	*4
High-level output voltage		V_{OHC1}		I_{OH} = −1 mA	0.2 × Vss	—	V_{DD}	V	*5
		V_{OHC2}		I_{OH} = −120 µA	0.2 × Vss	—	V_{DD}	V	OSC2
		V_{OHC1}	Vss = −2.7V	I_{OH} = −0.5 mA	0.2 × Vss	—	V_{DD}	V	*5
		V_{OHC2}	Vss = −2.7V	I_{OH} = −50 µA	0.2 × Vss	—	V_{DD}	V	OSC2
Low-level output voltage		V_{OLC1}		I_{OL} = 1 mA	Vss	—	0.8 × Vss	V	*5
		V_{OLC2}		I_{OL} = 120 µA	Vss	—	0.8 × Vss	V	OSC2
		V_{OLC1}	Vss = −2.7V	I_{OL} = 0.5 mA	Vss	—	0.8 × Vss	V	*5
		V_{OLC2}	Vss = −2.7V	I_{OL} = 50 µA	Vss	—	0.8 × Vss	V	OSC2
Input leakage current		I_{LI}	V_{IN} = V_{DD} or Vss		−1.0	—	1.0	µA	*6
Output leakage current		I_{LO}			−3.0	—	3.0	µA	*7
LCD driver ON resistance		R_{ON}	T_a = 25°C	V5 = −14.0V	—	2.0	3.0	kΩ	O0 ~ O166
				V5 = −8.0V	—	3.0	4.5	kΩ	*8
Static power consumption		I_{SSQ}			—	0.00	5.0	µA	Vss
		I_{5Q}	V5 = −18.0V		—	0.01	15.0	µA	V5
Input terminal capacity		C_{IN}	T_a = 25°C	f = 1 MHz	—	5.0	8.0	pF	*3 *4
Oscillator frequency		fosc	R_f = 1MΩ±2%	Vss = −5V	15	18	22	kHz	*9
				Vss = −2.7V	11	16	21		

Reset time	t_R		1.0	—	—	µs	*10
Reset "L" pulse width	t_{RW}		10	—	—	µs	*11

Built-in power circuit	Input voltage	Vss		−6.0	—	−2.4	V	*12
	Amplified output voltage	Vout	If amplified 3 times	−18.0	—	—	V	Vout
	Voltage regulator circuit operation voltage	Vout		−18.0	—	−6.0	V	Vout
	Voltage follower operation voltage	V5 ①	Supplied to SED1560	−16.0	—	−6.0	V	*13
		V5 ②	Supplied to SED1561	−16.0	—	−5.0	V	
		V5 ③	Supplied to SED1562	−16.0	—	−4.5	V	
	Reference voltage	V_{REG}	Ta = 25°C	−2.35	−2.5	−2.65	V	

Notes: * See Notes below.

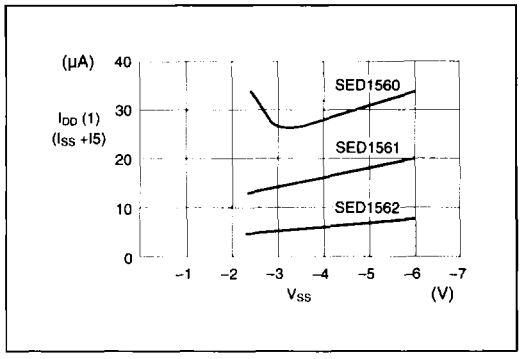
● **When dynamic current consumption (I) is displayed; the built-in power supply is on and T1 = T2 = Low**

Test conditions, unless otherwise specified: V_{DD} = 0V, V_{SS} = –5V ±10%, T_a = –30 to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Remarks
SED1560	I_{DD} (1)	V5 = –12.5V; 3 times amplified	—	169	340	µA	*16
SED1561		V5 = –8.0V; 3 times amplified	—	124	250	µA	
SED1562		V5 = –6.0V; 2 times amplified	—	53	110	µA	
		V_{SS} = –2.7V; 3 times amplified V5 = –6.0V	—	66	130	µA	

● **Typical current consumption characteristics**

○ **Dynamic current consumption (I), if an external clock and an external power supply are used**



Conditions: The built-in power supply is off but the external one is used.

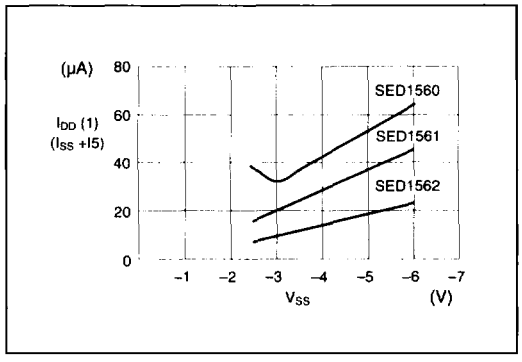
SED1560	V5	=	–12.5V
SED1561	V5	=	–8.0V
SED1562	V5	=	–6.0V

External clock:

SED1560	f_{CL}	=	4 kHz
SED1561	f_{CL}	=	2 kHz
SED1562	f_{CL}	=	1 kHz

Remarks: *14

○ **Dynamic current consumption (I), if the built-in oscillator and the external power supply are used**



Conditions: The built-in power supply is off but the external one is used.

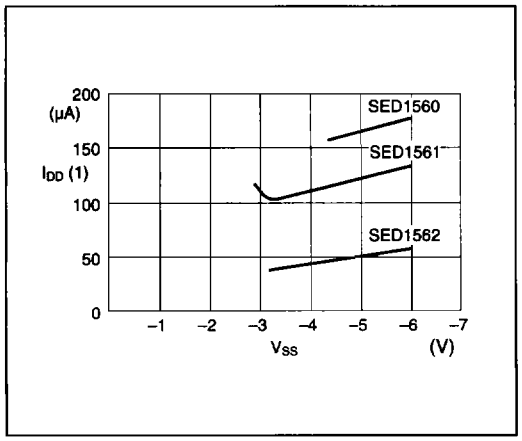
SED1560	V5	=	–12.5V
SED1561	V5	=	–8.0V
SED1562	V5	=	–6.0V

Internal oscillation:

SED1560	R_f	=	1 MΩ
SED1561	R_f	=	1 MΩ
SED1562	R_f	=	1 MΩ

Remarks: *15

○ **Dynamic current consumption (I), if the built-in power supply is used.**



Conditions: The built-in power supply is on and T1 = T2 = Low.

SED1560 V5 = –12.5V; 3 times amplified

SED1561 V5 = –8.0V; 3 times amplified

SED1562 V5 = –6.0V; 2 times amplified

Internal oscillation:

SED1560 Rf = 1 MΩ
SED1561 Rf = 1 MΩ
SED1562 Rf = 1 MΩ

Remarks: *16

Notes:

*1. Although the wide range of operating voltage is guaranteed, a spike voltage change during access to the MPU is not guaranteed.

*2. The operating voltage range of the VSS and V5 systems. The operating voltage range is applied if an external power supply is used.

*3. Pins A0, D0 to D7, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, FR, SYNC, M/S, C86, SI, P/S, T1 AND T2.

*4. Pins CL, SCL, and $\overline{RES}$.

*5. Pins D0 to D7, FR, SYNC, CL0, and DY0

*6. Pins A0, $\overline{RD}$ (E), $\overline{WR}$ (R/$\overline{W}$), $\overline{CS1}$, CS2, CL, M/S, $\overline{RES}$, C86, SI, SCL, P/S, T1, and T2.

*7. Applied if pins D0 to D7, FR, and SYNC are high impedance.

*8. The resistance when the 0.1 -volt voltage is applied between the "On" output terminal and each power terminal (V1, V2, V3 or V4). It must be within the operating voltage (2).

*9. The relationship between the oscillation frequency, frame and Rf value.

10. "tr" (reset time) indicates the period between the time when the $\overline{RES}$ signal rises and when the internal circuit has been reset. Therefore, the SED156 is usually operable after "tr" time.

*11. Specifies the minimum pulse width of $\overline{RES}$ signal. The Low pulse greater than "tRW" must be entered for reset.

*12. If the voltage is amplified three times by the built-in power circuit, the primary power Vss must be used within the input voltage range.

*13. The V5 voltage can be adjusted within the voltage follower operating range by the voltage regulator circuit.

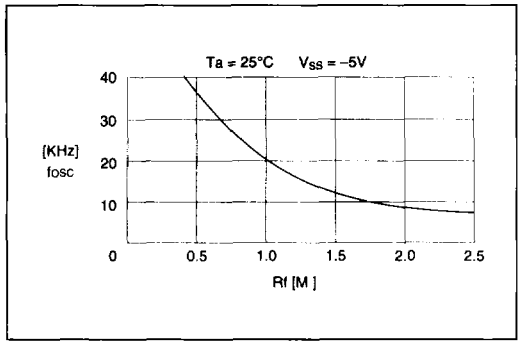
*14, 15, 16. Indicates the current consumed by the separate IC. The current consumption due to the LCD panel capacity and wiring capacity is not included.

The current consumption is shown if the checker is used, the display is turned on, the output status of Case 6 is selected, and the SED1560 is set to 1/64 duty, the SED1561 is set to 1/32 duty, and the SED1562 is set to 1/64 duty.

*14. Applied if an external clock is used and if not accessed by the MPU.

*15. Applied if the built-in oscillation circuit is used and if not accessed by the MPU.

*16. Applied if the built-in oscillation circuit and the built-in power circuit are used (T1 = T2 = Low) and if not accessed by the MPU.

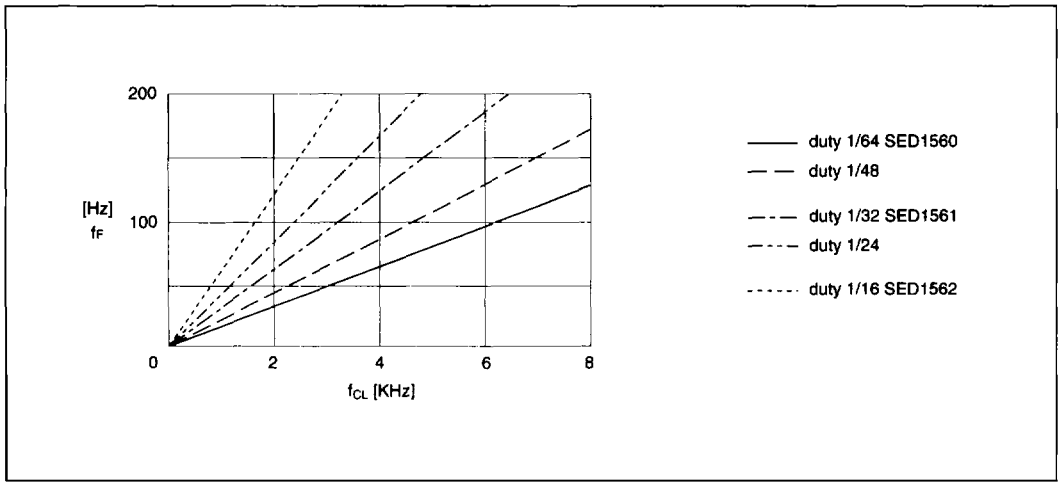


Oscillator frequency vs. frame vs. Rf
[SED156X]

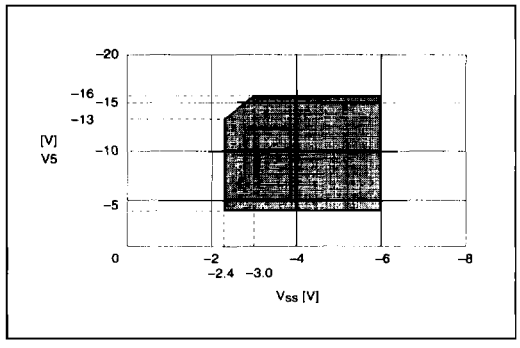
The relationship between oscillator frequency fosc and LCD frame frequency fF is obtained from the following expression:

Device	Duty	fF
SED1560	1/64	fosc/256
	1/48	fosc/192
SED1561	1/32	fosc/256
	1/24	fosc/192
SED1562	1/16	fosc/256

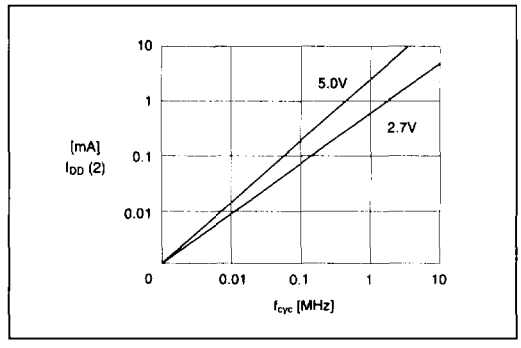
(fF indicates not fF signal cycle but cycle of LCD AC.)



External clock (fCL) vs. frame frequency [SED156X]



Operating voltage range for Vss and V5

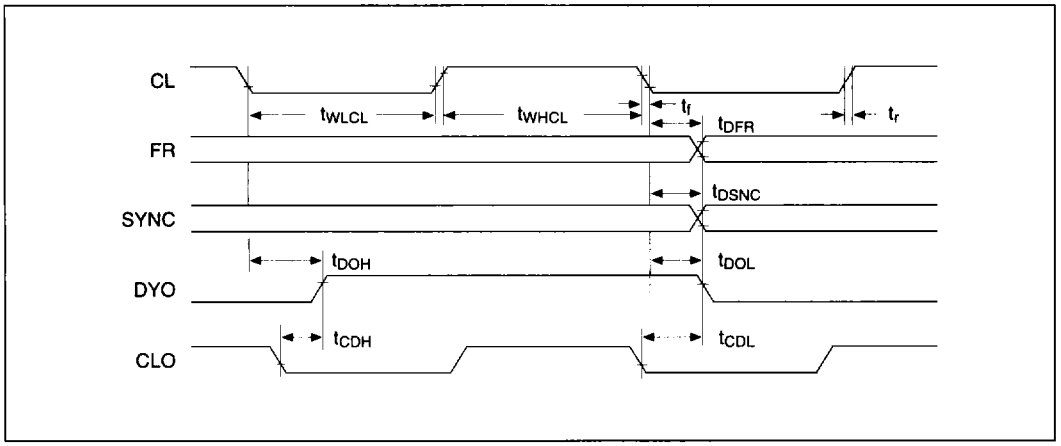


Power consumption during CPU access cycle
(IDD [2])

■ RESET

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reset time	t_R	t_R is measured from the rising edge of $\overline{RES}$. The SED156X resumes normal operating mode after a reset.	1.0	—	—	µs
Reset LOW-level pulsewidth	t_{RW}		1.0	—	—	µs

■ DISPLAY CONTROL TIMING



● Display Control Input Timing

V_{SS} = –5.5 to –4.5V, T_a = –30 to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CL LOW-level pulsewidth	t_{WLCL}		35	—	—	µs
CL HIGH-level pulsewidth	t_{WHCL}		35	—	—	µs
CL rise time	t_r		—	30	—	ns
CL fall time	t_f		—	30	—	ns
FR delay time	t_{DFR}		–1.0	—	1.0	µs
SYNC delay time	t_{DSNC}		–1.0	—	1.0	µs

V_{SS} = –4.5 to –2.7V, T_a = –30 to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
CL LOW-level pulsewidth	t_{WLCL}		35	—	—	µs
CL HIGH-level pulsewidth	t_{WHCL}		35	—	—	µs
CL rise time	t_r		—	40	—	ns
CL fall time	t_f		—	40	—	ns
FR delay time	t_{DFR}		–1.0	—	1.0	µs
SYNC delay time	t_{DSNC}		–1.0	—	1.0	µs

Notes: 1. Effective only when the SED156X is in the master mode.

2. The FR/SYNC delay time input timing is provided in the slave operation.
   The FR/SYNC delay time output timing is provided in the master operation.

3. Each timing is based on 20% and 80% of V_{SS}.

- **Display Control Output Timing**

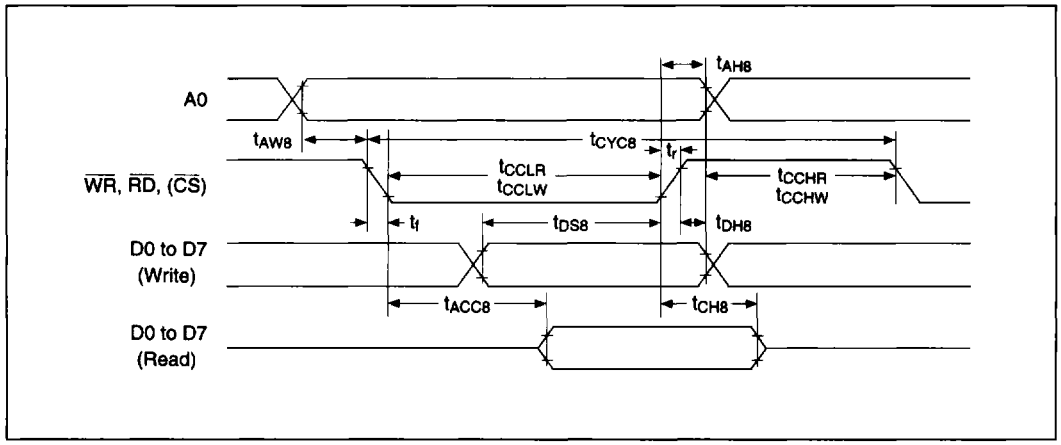
V_{SS} = –5.5 to –4.5V, T_a = –30 to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
FR delay time	t_{DFR}	C_L = 50 pF	—	60	150	ns
SYNC delay time	t_{DSNC}	C_L = 100 pF	—	60	150	ns
DYO LOW-level delay time	t_{DOL}		—	70	160	ns
DYO HIGH-level delay time	t_{DOH}		—	70	160	ns
CLO to DYO LOW-level delay time	t_{CDL}	SED156X operating in master mode only	—	40	100	ns
CLO to DYO HIGH-level delay time	t_{CDH}	SED156X operating in master mode only	—	40	100	ns

V_{SS} = –4.5 to –2.7V, T_a = –30 to 85°C

Parameter	Symbol	Condition	Min	Typ	Max	Unit
FR delay time	t_{DFR}	C_L = 50 pF	—	120	240	ns
SYNC delay time	t_{DSNC}	C_L = 100 pF	—	120	240	ns
DYO LOW-level delay time	t_{DOL}		—	140	250	ns
DYO HIGH-level delay time	t_{DOH}		—	140	250	ns
CLO to DYO LOW-level delay time	t_{CDL}	SED156X operating in master mode only	—	100	200	ns
CLO to DYO HIGH-level delay time	t_{CDH}	SED156X operating in master mode only	—	100	200	ns

- **System Buses: Read/Write Characteristics I (80-Series MPU)**



V_{SS} = –5.0 ± 10%, T_a = –30 to 85°C

Parameter	Signal	Symbol	Condition	Min	Max	Unit
Address hold time	A0, $\overline{CS}$	t_{AH8}		10	—	ns
Address setup time		t_{AW8}		10	—	ns
System cycle time		t_{CYC8}		200	—	ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		22	—	ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		77	—	ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		172	—	ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		117	—	ns
Data setup time		t_{DS8}		20	—	ns
Data hold time		t_{DH8}		10	—	ns
$\overline{RD}$ access time	D0 ~ D7	t_{ACC8}	CL = 100pF	—	70	ns
Output disable time		t_{CH8}		10	50	ns
Input signal change time		t_r, t_f		—	15	ns

V_{SS} = –2.7 to –4.5V, T_a = –30 to 85°C

Parameter	Signal	Symbol	Condition	Min	Max	Unit
Address hold time	A0, $\overline{CS}$	t_{AH8}		25	—	ns
Address setup time		t_{AW8}		25	—	ns
System cycle time		t_{CYC8}		450	—	ns
Control L pulse width (WR)	$\overline{WR}$	t_{CCLW}		44	—	ns
Control L pulse width (RD)	$\overline{RD}$	t_{CCLR}		194	—	ns
Control H pulse width (WR)	$\overline{WR}$	t_{CCHW}		394	—	ns
Control H pulse width (RD)	$\overline{RD}$	t_{CCHR}		244	—	ns
Data setup time		t_{DS8}		40	—	ns
Data hold time		t_{DH8}		20	—	ns
$\overline{RD}$ access time	D0 ~ D7	t_{ACC8}	CL = 100pF	—	140	ns
Output disable time		t_{CH8}		10	100	ns
Input signal change time		t_r, t_f		—	15	ns

Notes: 1. When using the system cycle time in the high-speed mode, it is limited by $t_r + t_f \leq (t_{CYC8} - t_{CCLW} - t_{CCHW})$ or $t_r + t_f \leq (t_{CYC8} - t_{CCLR} - t_{CCHR})$

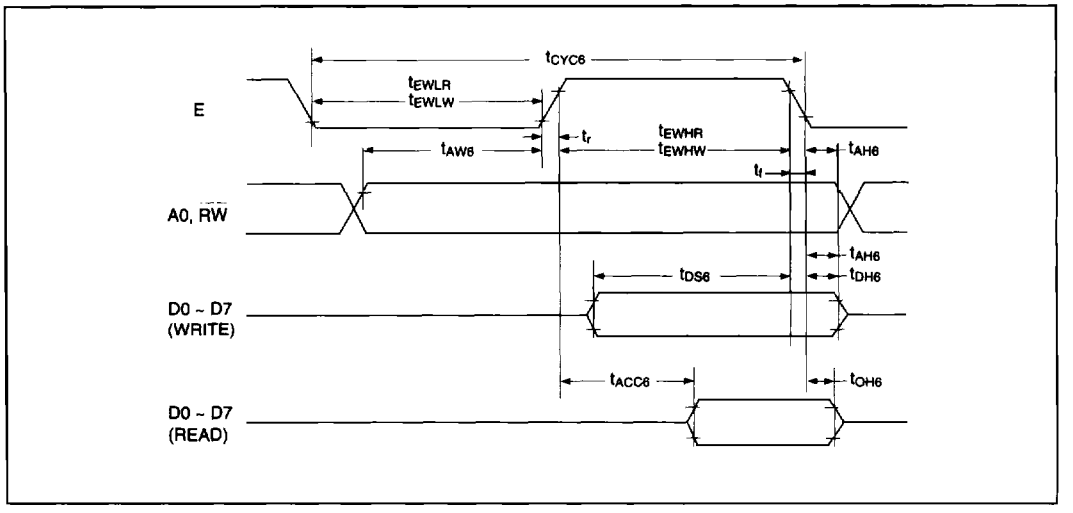
2. All signal timings are limited based on 20% and 80% of Vss voltage.

3. Read/write operation is performed while $\overline{CS}$ ($\overline{CS1}$ and CS2) is active and the $\overline{RD}$ or $\overline{WR}$ signal is in the low level.

   If read/write operation is performed by the $\overline{RD}$ or $\overline{WR}$ signal while $\overline{CS}$ is active, it is determined by the $\overline{RD}$ or $\overline{WR}$ signal timing.

   If read/write operation is performed by $\overline{CS}$ while the $\overline{RD}$ or $\overline{WR}$ signal is in the low level, it is determined by the $\overline{CS}$ active timing.

● **System Buses: Read/Write Characteristics II (68-Series MPU)**



Vss = –5.0V ± 10%, Ta = –30 to 85°C

Parameter		Signal	Symbol	Condition	Min	Max	Unit
System cycle time			tCYC6		200	—	ns
Address setup time		(A0)	tAW6		10	—	ns
Address hold time		R/$\overline{W}$	tAH6		10	—	ns
Data setup time		D0 ~ D7	tDS6		20	—	ns
Data hold time			tDH6		10	—	ns
Output disable time			tOH6	CL = 100pF	10	50	ns
Access time			tACC6		—	70	ns
Enable H pulse width	READ	E	tEWHR		77	—	ns
	WRITE		tEWHW		22	—	ns
Enable L pulse width	READ	E	tEWLR		117	—	ns
	WRITE		tEWLW		172	—	ns
Input signal change time			tr, tf		—	15	ns

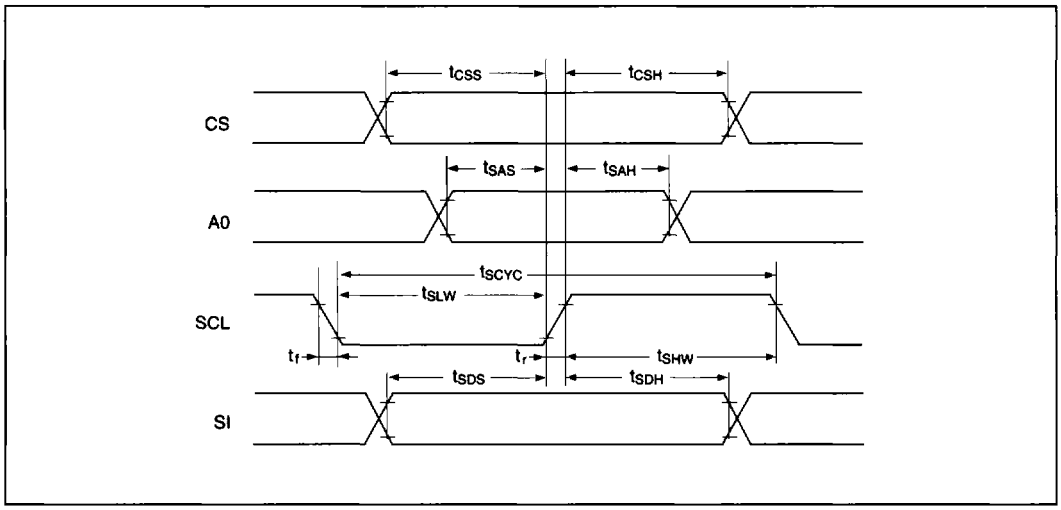
Vss = –5.0V ± 10%, Ta = –30 to 85°C

Parameter		Signal	Symbol	Condition	Min	Max	Unit
System cycle time		A0, $\overline{CS}$	tCYC6		450	—	ns
Address setup time		($\overline{CS1}$, CS2)	tAW6		25	—	ns
Address hold time		R/$\overline{W}$	tAH6		25	—	ns
Data setup time		D0 ~ D7	tDS6		40	—	ns
Data hold time			tDH6		20	—	ns
Output disable time			tOH6	CL = 100pF	20	100	ns
Access time			tACC5		—	140	ns
Enable H pulse width	READ	E	tEWHR		154	—	ns
	WRITE		tEWHW		44	—	ns
Enable L pulse width	READ	E	tEWLR		244	—	ns
	WRITE		tEWLW		394	—	ns
Input signal change time			tr, tf		—	15	ns

Notes: 1. When using the system cycle time in the high-speed mode, it is limited by $t_r + t_f \leq (t_{CYC6} - t_{EWLW} - t_{EWHW})$ or $t_r + t_f \leq (t_{CYC6} - t_{EWLR} - t_{EWHR})$

2. All signal timings are limited based on 20% and 80% of Vss voltage.
3. Read/write operation is performed while $\overline{CS}$ ($\overline{CS1}$ and CS2) is active and the E signal is in the high level.
   If read/write operation is performed by the E signal while $\overline{CS}$ is active, it is determined by the E signal timing.
   If read/write operation is performed by $\overline{CS}$ while the E signal is in the high level, it is determined by the $\overline{CS}$ active timing.

● Serial Interface



Vss = –5.0V ± 10%, Ta = –30 to 85°C

Parameter	Signal	Symbol	Condition	Min	Max	Unit
Serial clock cycle	SCL	tSCYC		500	—	ns
SCL high pulse width		tSHW		150	—	ns
SCL low pulse width		tSLW		150	—	ns
Address setup time	A0	tSAS		120	—	ns
Address hold time		tSAH		200	—	ns
Data setup time	SI	tSDS		120	—	ns
Data hold time		tSDH		50	—	ns
$\overline{CS}$-SCL time	$\overline{CS}$	tCSS		30	—	ns
		tCSH		400	—	ns
Input signal change time		tr, tf		—	50	ns

V_{SS} = –5.0V ± 10%, T_a = –30 to 85°C

Parameter	Signal	Symbol	Condition	Min	Max	Unit
Serial clock cycle	SCL	tSCYC		1000	—	ns
SCL high pulse width		tSHW		300	—	ns
SCL low pulse width		tSLW		300	—	ns
Address setup time	A0	tSAS		250	—	ns
Address hold time		tSAH		400	—	ns
Data setup time	SI	tSDS		250	—	ns
Data hold time		tSDH		100	—	ns
$\overline{CS}$-SCL time	$\overline{CS}$	tCSS		60	—	ns
		tCSH		800	—	ns
Input signal change time		tr, tf		—	50	ns

Note: *2. All signal timings are limited based on 20% and 80% of V_{SS} voltage.

■ RESET

When power is turned ON, the SED1560 is initialized on the rising edge of $\overline{RES}$. Initial settings are as follows:

1. Display ..... OFF
2. Display mode ..... Normal
3. *n*-line inversion ..... OFF
4. Duty cycle 1/64
5. ADC select ..... Normal
6. Read/write modify ..... OFF
7. On-chip power supply ..... OFF
8. Serial interface register ..... Cleared
9. Display initial line register ..... Line 1
10. Column address counter 0
11. Page address register ..... Page 0
12. Output selection circuit ..... Case 6
13. *n*-line inversion register 16
14. Set the electronic control register to zero (0)

$\overline{RES}$ should be connected to the microprocessor reset terminal so that both devices are reset at the same time. $\overline{RES}$ must be LOW for at least 1 µs to correctly reset the SED1560. Normal operation starts 1 µs after the rising edge on $\overline{RES}$.

If the SED1560 is not properly initialized when power is turned ON, it can lock itself into a state that cannot be cancelled.

When the Reset command is used, only initial settings 9 to 14 are active.

■ COMMANDS

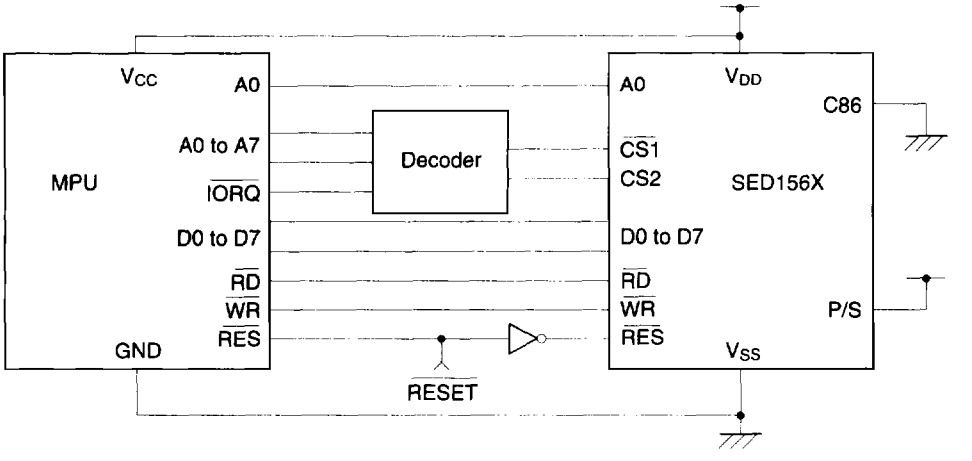
● The Command Set

A0, $\overline{RD}$ and $\overline{WR}$ identify the data bus commands. Interpretation and execution of commands are synchronized to the internal clock. Since a busy check is normally not needed, commands can be processed at high speed. When the serial interface is used, the order of data entry is D7 to D0.

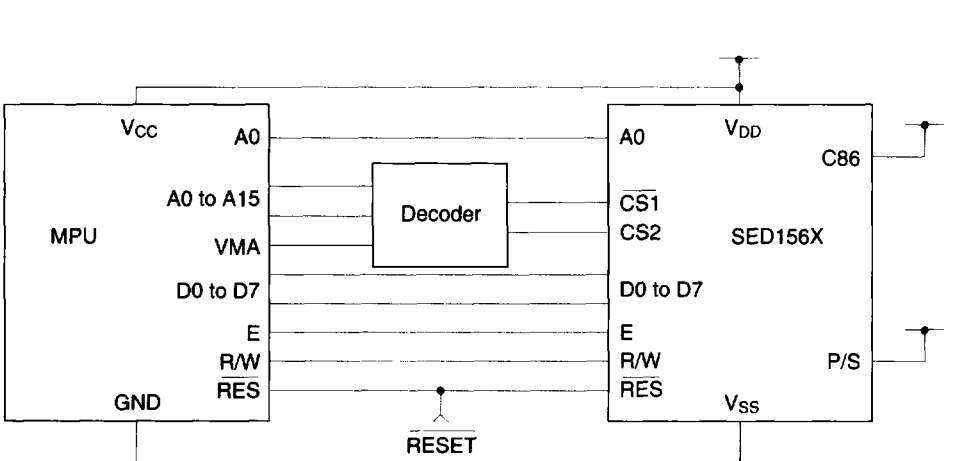
Command	Code											Description
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0 1	Turns the display ON and OFF. 0: OFF 1: ON
Display START Line set	0	1	0	0	1	Display line address						Determines the RAM display line for COM0.
Page address set	0	1	0	1	0	1	1	Page address				Sets the display RAM pages in the Page Address register.
Column address set high-order 4 bits	0	1	0	0	0	0	1	High-order column address				Sets the high-order 4 bits of the display RAM column address in the register.
Column address set low-order 4 bits	0	1	0	0	0	0	0	Low-order column address				Sets the low-order 4 bits of the display RAM column address in the register.
Status read	0	0	1	Status				0	0	0	0	Reads the status information.
Display data write	1	1	0	Write data								Writes data in the display RAM.
Display data read	1	0	1	Read data								Reads data from the display RAM.
ADC select	0	1	0	1	0	1	0	0	0	0	0 1	Outputs the display RAM address for SEG. 0: Normal 1: Reversed
Normal/reverse display	0	1	0	1	0	1	0	0	1	1	0 1	Display the LCD image in normal or reverse mode. 0: Normal 1: Reversed
All indicator ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	Lights all indicators. 0: Normal display 1: All ON
Duty select	0	1	0	1	0	1	0	1	0	0	0 1	Sets LCD drive duty (1). 0: 1/24, 48 1: 1/32, 64
Duty + 1	0	1	0	1	0	1	0	1	0	1	0 1	Sets LCD drive duty (2). 0: Normal 1: Duty + 1
n-line reverse register set	0	1	0	0	0	1	1	No. of reversed *n*-lines				Sets the line reverse driving and no. of reverse lines in the line reverse register.
n-line reverse register release	0	1	0	0	0	1	0	0	0	0	0	Releases the line reverse driving.
Read Modify Write	0	1	0	1	1	1	0	0	0	0	0	Increments by 1 during write of column address counter, and sets to 0 during read.
End	0	1	0	1	1	1	0	1	1	1	0	Releases the Read Modify write mode.
Reset	0	1	0	1	1	1	0	0	0	1	0	Internal reset.
Output status register set	0	1	0	1	1	0	0	Output status				Sets the COM and SEG status in registers.
Built-in power supply ON/OFF	0	1	0	0	0	1	0	0	1	0	0 1	0: Power OFF 1: Power ON
Power-on completion	0	1	0	1	1	1	0	1	1	0	1	Completes the turn-on sequence of built-in power supply.
Electronic control register set	0	1	0	1	0	0	Electronic control value					Sets the V5 output voltage in the electronic control register.
Power save												A complex command to turn off the display and light all indicators.

■ MICROPROCESSOR INTERFACE

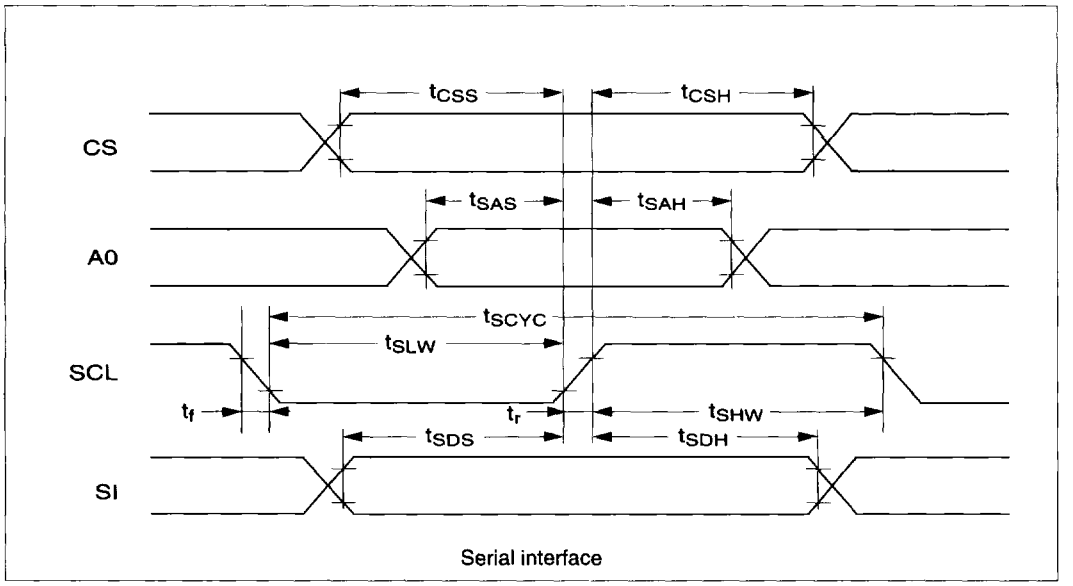
The SED1560 Series communicates with a high-speed microprocessor, such as the Intel 80XX family or the Motorola 68XX family, through 8-bit parallel data transfer. The number of connections to the microprocessor can be minimized by using a serial interface. When used in a multiple-chip configuration, the SED1560 Series is controlled by the chip select signals from the microprocessor.



8080-series microprocessors

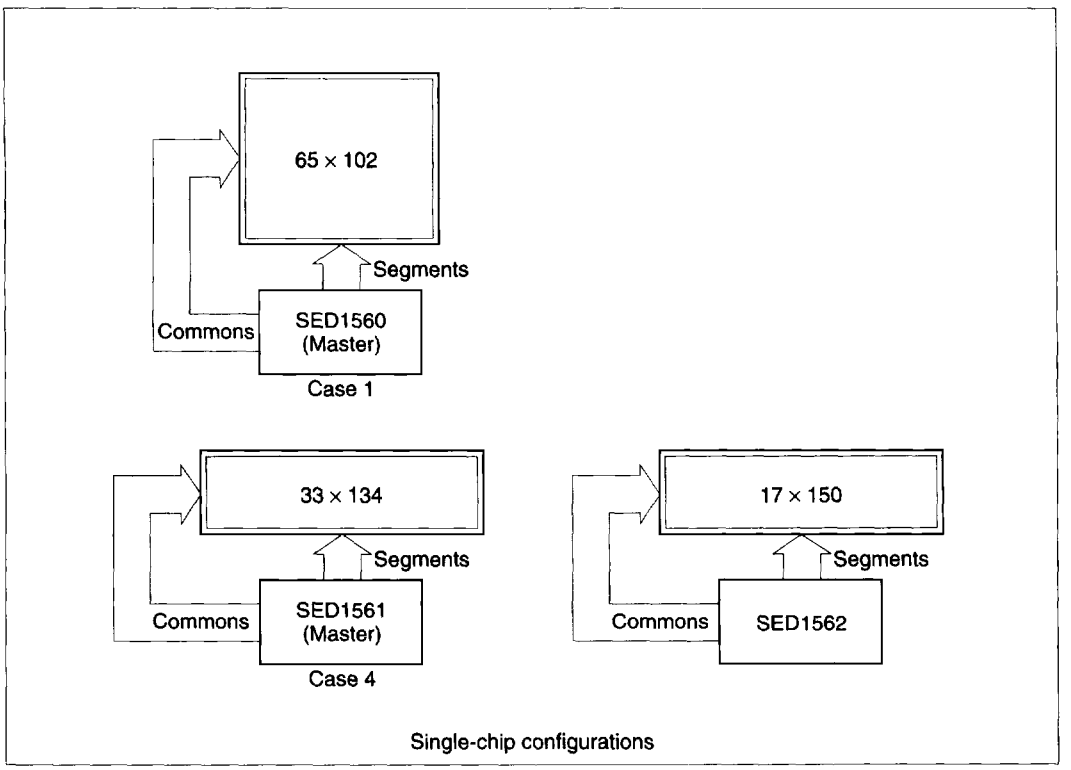


6800-series microprocessors



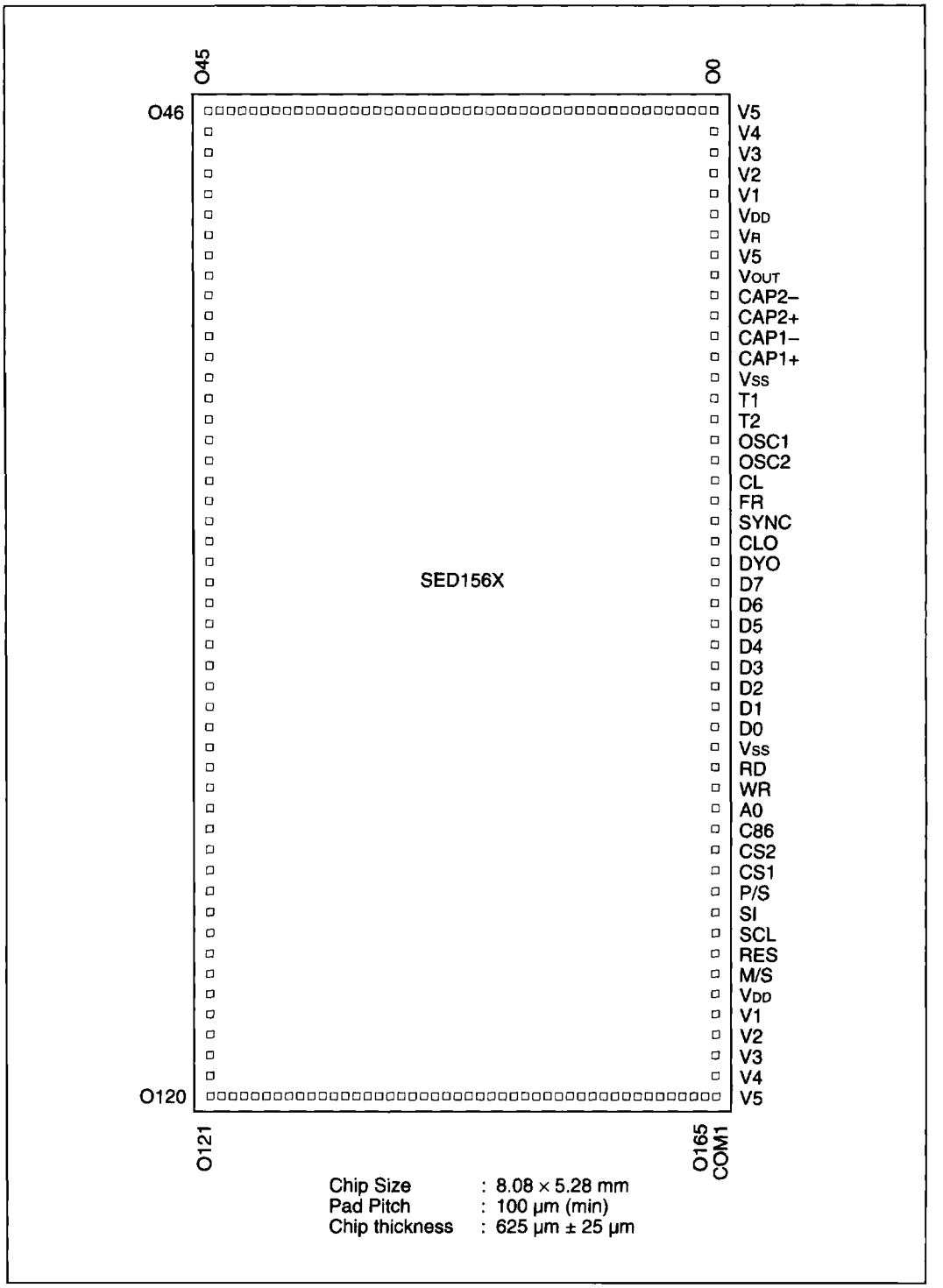
Serial interface

■ LCD PANEL INTERFACE EXAMPLES



Single-chip configurations

■ PAD LAYOUT



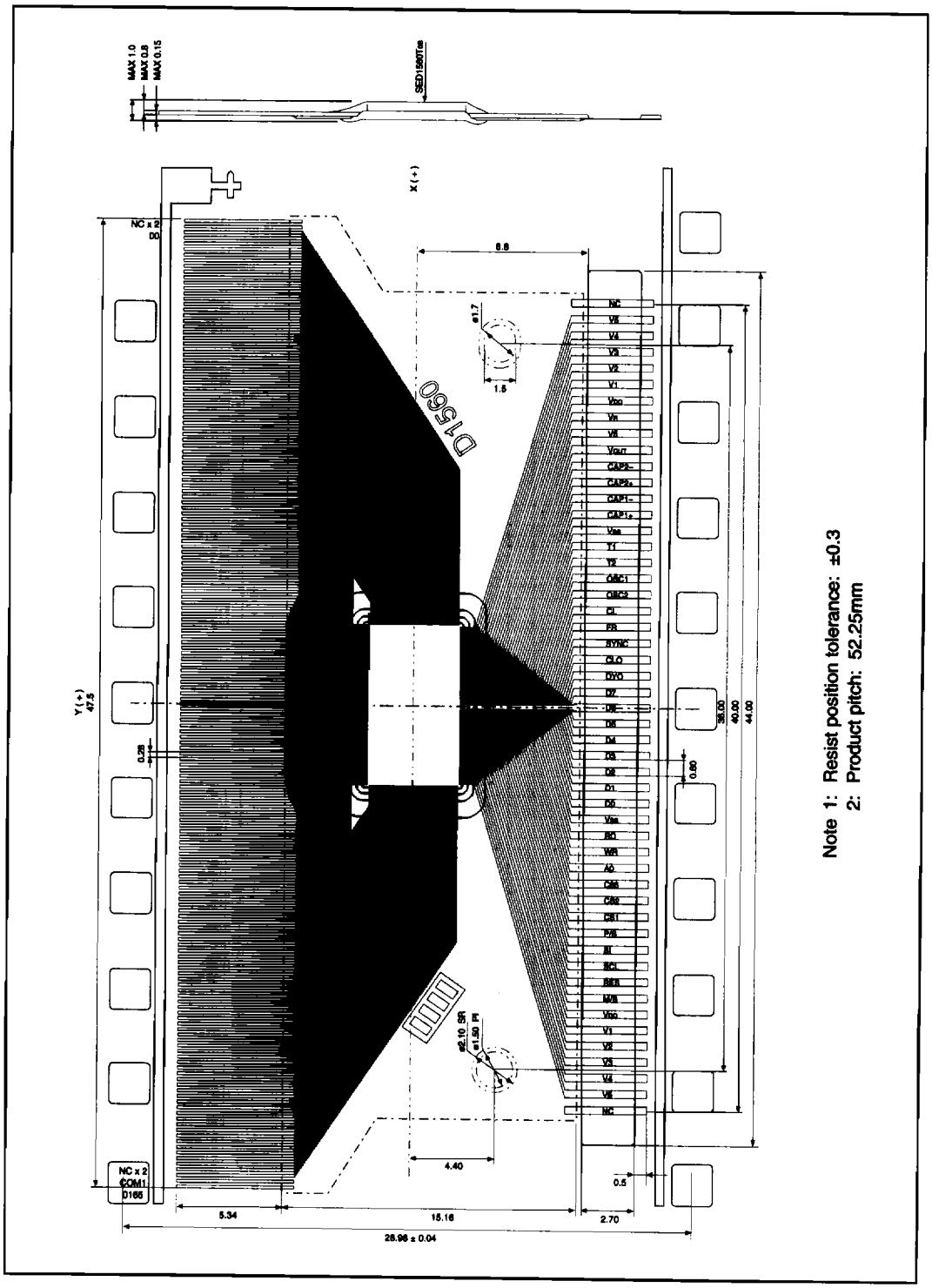
Chip Size : 8.08 × 5.28 mm
Pad Pitch : 100 µm (min)
Chip thickness : 625 µm ± 25 µm

● Pad Coordinates

Unit: µm

No.	Pin Name	X Coord.	Y Coord.
1	V5	3640	2487
2	V4	3489	2487
3	V3	3339	2487
4	V2	3188	2487
5	V1	3037	2487
6	V_{DD}	2889	2487
7	M/S	2755	2487
8	$\overline{RES}$	2604	2487
9	SCL	2453	2487
10	SI	2302	2487
11	P/S	2151	2487
12	$\overline{CS1}$	2001	2487
13	CS2	1850	2487
14	C86	1699	2487
15	A0	1548	2487
16	$\overline{WR}$	1397	2487
17	$\overline{RD}$	1247	2487
18	V_{SS}	1077	2487
19	D0	945	2487
20	D1	794	2487
21	D2	643	2487
22	D3	493	2487
23	D4	342	2487
24	D5	191	2487
25	D6	40	2487
26	D7	-111	2487
27	DYO	-261	2487
28	CLO	-412	2487
29	SYNC	-563	2487
30	FR	-714	2487
31	CL	-865	2487
32	OSC2	-1015	2487
33	OSC1	-1166	2487
34	T2	-1317	2487
35	T1	-1468	2487
36	VSS	-1638	2487
37	CAP1+	-1789	2487
38	CAP1-	-1939	2487
39	CAP2+	-2090	2487
40	CAP2-	-2241	2487
41	V_{OUT}	-2392	2487
42	V5	-2543	2487
43	VR	-2674	2487
44	V_{DD}	-2844	2487
45	V1	-2995	2487
46	V2	-3146	2487
47	V3	-3297	2487
48	V4	-3447	2487
49	V5	-3598	2487
50	O0	-3887	2294
51	O1	-3887	2194
52	O2	-3887	2094
53	O3	-3887	1994
54	O4	-3887	1894
55	O5	-3887	1794
56	O6	-3887	1694
57	O7	-3887	1594
58	O8	-3887	1494
59	O9	-3887	1394
60	O10	-3887	1294
61	O11	-3887	1194
62	O12	-3887	1094
63	O13	-3887	994
64	O14	-3887	894
65	O15	-3887	794
66	O16	-3887	694
67	O17	-3887	594
68	O18	-3887	494
69	O19	-3887	394
70	O20	-3887	294
71	O21	-3887	194
72	O22	-3887	94
73	O23	-3887	-6
74	O24	-3887	-106
75	O25	-3887	-206
76	O26	-3887	-306
77	O27	-3887	-406
78	O28	-3887	-506
79	O29	-3887	-606
80	O30	-3887	-706
81	O31	-3887	-806
82	O32	-3887	-906
83	O33	-3887	-1006
84	O34	-3887	-1106
85	O35	-3887	-1206
86	O36	-3887	-1306
87	O37	-3887	-1406
88	O38	-3887	-1506
89	O39	-3887	-1606
90	O40	-3887	-1706
91	O41	-3887	-1806
92	O42	-3887	-1906
93	O43	-3887	-2006
94	O44	-3887	-2106
95	O45	-3887	-2206
96	O46	-3711	-2487
97	O47	-3611	-2487
98	O48	-3511	-2487
99	O49	-3411	-2487
100	O50	-3311	-2487
101	O51	-3211	-2487
102	O52	-3111	-2487
103	O53	-3011	-2487
104	O54	-2911	-2487
105	O55	-2811	-2487
106	O56	-2711	-2487
107	O57	-2611	-2487
108	O58	-2511	-2487
109	O59	-2411	-2487
110	O60	-2311	-2487
111	O61	-2211	-2487
112	O62	-2111	-2487
113	O63	-2011	-2487
114	O64	-1911	-2487
115	O65	-1811	-2487
116	O66	-1711	-2487
117	O67	-1611	-2487
118	O68	-1511	-2487
119	O69	-1411	-2487
120	O70	-1311	-2487
121	O71	-1211	-2487
122	O72	-1111	-2487
123	O73	-1011	-2487
124	O74	-911	-2487
125	O75	-811	-2487
126	O76	-711	-2487
127	O77	-611	-2487
128	O78	-511	-2487
129	O79	-411	-2487
130	O80	-311	-2487
131	O81	-211	-2487
132	O82	-111	-2487
133	O83	-11	-2487
134	O84	89	-2487
135	O85	189	-2487
136	O86	289	-2487
137	O87	389	-2487
138	O88	489	-2487
139	O89	589	-2487
140	O90	689	-2487
141	O91	789	-2487
142	O92	889	-2487
143	O93	989	-2487
144	O94	1089	-2487
145	O95	1189	-2487
146	O96	1289	-2487
147	O97	1389	-2487
148	O98	1489	-2487
149	O99	1589	-2487
150	O100	1689	-2487
151	O101	1789	-2487
152	O102	1889	-2487
153	O103	1989	-2487
154	O104	2089	-2487
155	O105	2189	-2487
156	O106	2289	-2487
157	O107	2389	-2487
158	O108	2489	-2487
159	O109	2589	-2487
160	O110	2689	-2487
161	O111	2789	-2487
162	O112	2889	-2487
163	O113	2989	-2487
164	O114	3089	-2487
165	O115	3189	-2487
166	O116	3289	-2487
167	O117	3389	-2487
168	O118	3489	-2487
169	O119	3589	-2487
170	O120	3689	-2487
171	O121	3887	-2206
172	O122	3887	-2106
173	O123	3887	-2006
174	O124	3887	-1906
175	O125	3887	-1806
176	O126	3887	-1706
177	O127	3887	-1606
178	O128	3887	-1506
179	O129	3887	-1406
180	O130	3887	-1306
181	O131	3887	-1206
182	O132	3887	-1106
183	O133	3887	-1006
184	O134	3887	-906
185	O135	3887	-806
186	O136	3887	-706
187	O137	3887	-606
188	O138	3887	-506
189	O139	3887	-406
190	O140	3887	-306
191	O141	3887	-206
192	O142	3887	-106
193	O143	3887	-6
194	O144	3887	94
195	O145	3887	194
196	O146	3887	294
197	O147	3887	394
198	O148	3887	494
199	O149	3887	594
200	O150	3887	694
201	O151	3887	794
202	O152	3887	894
203	O153	3887	994
204	O154	3887	1094
205	O155	3887	1194
206	O156	3887	1294
207	O157	3887	1394
208	O158	3887	1494
209	O159	3887	1594
210	O160	3887	1694
211	O161	3887	1794
212	O162	3887	1894
213	O163	3887	1994
214	O164	3887	2094
215	O165	3887	2194
216	COMI	3887	2294

● **TCP Dimensions (2-sided)**



Note 1: Resist position tolerance: ±0.3
2: Product pitch: 52.25mm

● **TCP Dimensions (4-sided)**