PEX 8311 Key Features

- Generic Local Bus to PCI Express Bridge
- Root Complex and EndPoint Modes of Operation
- Local Bus Modes:
  - 32-bit address & 32-bit data (C-Mode)
  - Multiplexed 32-bit address/data (J-Mode)
- Local Clock rates up to 66MHz
- Zero wait state bursts to 264MB/s
- Integrated SERDES
- 2 DMA channels
- 21x21 mm^2, 337 pin PBGA
- Typical Power: under 1.0 Watt

Other Features

- Integrated PCIe Interface
- Compliant to PCIe r1.0a
- x1 Link, 2.5 Gbps / direction
- Auto Polarity Reversal
- Link CRC Support
- Link / Device Power Management
- Flow Control Buffering
- PCIe Transaction Queues for Eight outstanding TLPs
- Direct Master Data Transfers
- Direct Slave Data Transfers
- Configuration Through Host or Optional EEPROM
- On-the-fly Endian Conversion
- 8 Mailbox & 2 Doorbell Registers
- Four GPIO, 1 GPI, 1 GPO
- I2O Messaging Unit

Application:
Medical Imaging Systems

PLX Product:
PEX 8311 – Local Bus to PCIe Bridge

Key Benefit:
Full Connectivity to PCIe Components

New Medical Imaging Systems Migrating to PCI Express Designs

Medical imaging systems are limited in their ability to display images which can impact the ability of medical professionals to provide an accurate prognosis. The four important things that any medical imaging system should be able to perform are: image acquisition, image processing, image management and image display. These medical imaging systems should also enable real-time compression and provide 3D/4D pixel-perfect images for doctors to get a better understanding of the patient's status. A typical application would involve several scanners taking pixel-perfect images of the same part or multiple parts of the human body which are then processed, collated and displayed via a high-bandwidth interface so that doctors can collect images real-time, store them on the network and if necessary transmit them to remote locations. To implement such systems, an intelligent medical imaging system collects and feeds data to a central host through the network. Performance and multiple channels are a must. PCIe interconnect technology fits the need.

PEX 8311 Supports Full Protocol Translations

The PEX 8311 is a bridge from a low overhead parallel generic local bus (used by various processors, DSPs, memory, and FPGA designs) to a PCIe port. In this conversion, the bridge completely translates data from the local bus into PCIe packets with full packet header generation. Address spaces from the local bus and PCIe domain are fully translated. Out-of-band signals on the local bus are translated into message signaling interrupt (MSI) packets and vice versa. The bridge supports all transaction types. Full on-chip buffers provide flow control and the link layer CRC ensures data integrity.

High Bandwidth is the Key

Figure 1 shows the PEX 8311 used in a medical imaging system. Here multiple sources of video images from several scanners are passed to an FPGA for image processing and image management and then through the bridge. The bridge converts traffic to PCIe and passes it through an aggregation switch, such as PLX's PEX8532, and then passes it to the host controller for analysis and further action. FPGA devices routinely use a local bus type interface and connect with no glue logic to the PEX 8311 bridge. As there are multiple streams of data, several bridges are used in the design. A local CPU is used to manage this traffic flow. Memory or other components may also be present on this local bus.
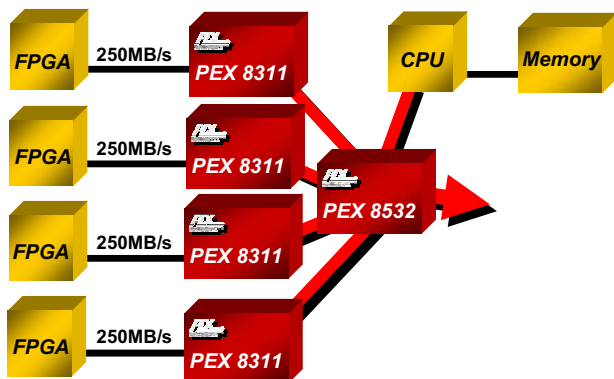

Figure 1

Shipping Now!

The PEX 8311 is in volume production with both the devices and RDK boards available in stock at PLX. The RDK boards allow quick evaluation of your design concept without having to lay out your own board.

Additional PEX 8311 Capabilities

Medical Imaging Systems may require large numbers of devices present on the local bus and have high bandwidth needs. Local bus devices need to communicate with each other and not just through the bridge. The PEX 8311 has the capability to

handle up to five simultaneous loads present on the local bus with up to 32-bit and 66 MHz operation.

In addition, the PEX 8311 includes Direct Master and Direct Slave operation simultaneously with DMA. As these modes have higher priority than DMA, they can be used to provide control data or other throughput that cannot be blocked by DMA transfers. To enhance throughput even more, the Read Ahead mode allows data to be obtained and stored in internal FIFOs before it is sent through the bridge.

Design Tools & Documentation:

On PLX Public ToolBox:
http://www.plxtech.com/products/pci_express/PEX8311/default.asp

♦ Data Book, BSDL, IBIS and HSPICE Models, RDK, OrCAD Symbols and Gerber files.

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