

# FET Input Power Operational Amplifier

## FEATURES

- **LOW BIAS CURRENT** — FET Input
- **PROTECTED OUTPUT STAGE** — Thermal Shutoff
- **EXCELLENT LINEARITY** — Class A/B Output
- **WIDE SUPPLY RANGE** — ±12V TO ±50V
- **HIGH OUTPUT CURRENT** — ±5A Peak



8-PIN TO-3  
PACKAGE STYLE CE

## APPLICATIONS

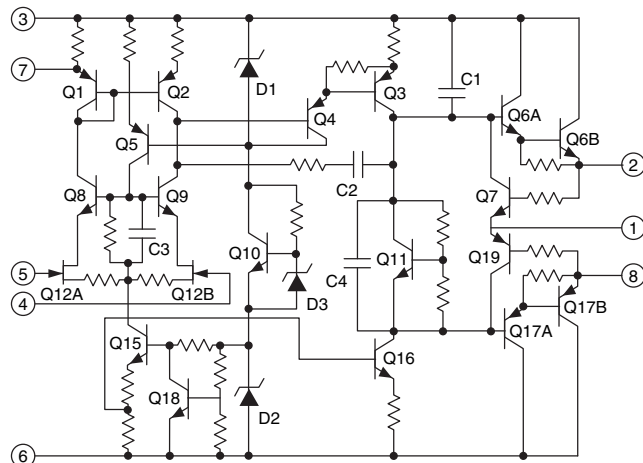
- **MOTOR, VALVE AND ACTUATOR CONTROL**
- **MAGNETIC DEFLECTION CIRCUITS UP TO 4A**
- **POWER TRANSDUCERS UP TO 100kHz**
- **TEMPERATURE CONTROL UP TO 180W**
- **PROGRAMMABLE POWER SUPPLIES UP TO 90V**
- **AUDIO AMPLIFIERS UP TO 60W RMS**

## DESCRIPTION

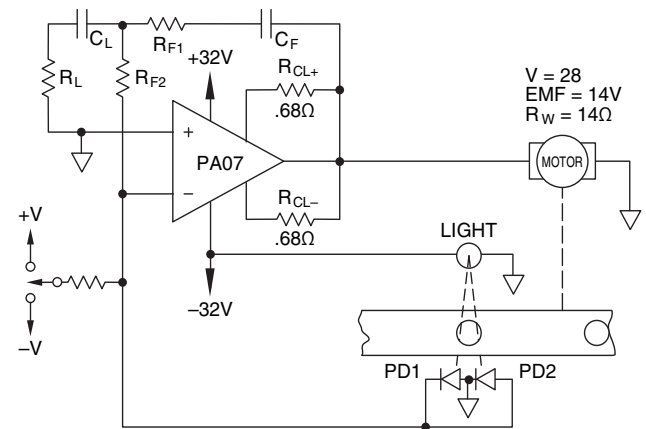
The PA07 is a high voltage, high output current operational amplifier designed to drive resistive, inductive and capacitive loads. For optimum linearity, especially at low levels, the output stage is biased for class A/B operation using a thermistor compensated base-emitter voltage multiplier circuit. A thermal shutoff circuit protects against overheating and minimizes heatsink requirements for abnormal operating conditions. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

This hybrid circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible washers and/or improper mounting torque will void the product warranty. Please see "General Operating Considerations".

## EQUIVALENT SCHEMATIC



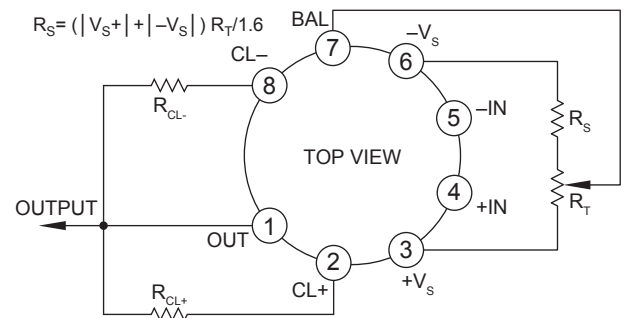
## TYPICAL APPLICATION



**Negates optoelectronic instabilities**  
**Lead network minimizes overshoot**  
**SEQUENTIAL POSITION CONTROL**

Position is sensed by the differentially connected photo diodes, a method that negates the time and temperature variations of the optical components. Off center positions produce an error current which is integrated by the op amp circuit, driving the system back to center position. A momentary switch contact forces the system out of lock and then the integrating capacitor holds drive level while both diodes are in a dark state. When the next index point arrives, the lead network of C1 and R1 optimize system response by reducing overshoot. The very low bias current of the PA07 augments performance of the integrator circuit.

## EXTERNAL CONNECTIONS



NOTE: Input offset voltage trim optional.  $R_T = 10K\Omega$  MAX

**ABSOLUTE MAXIMUM RATINGS**

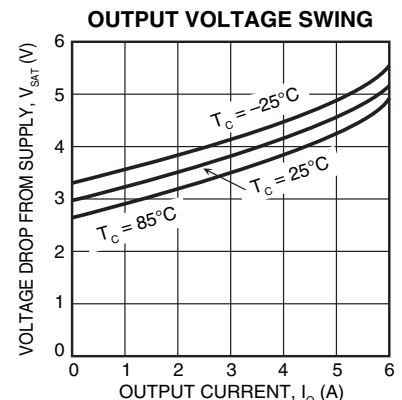
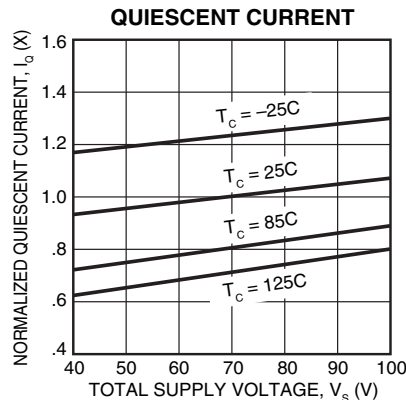
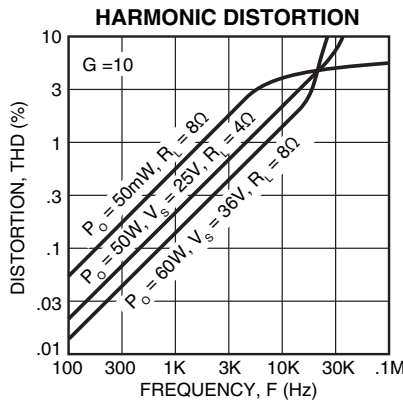
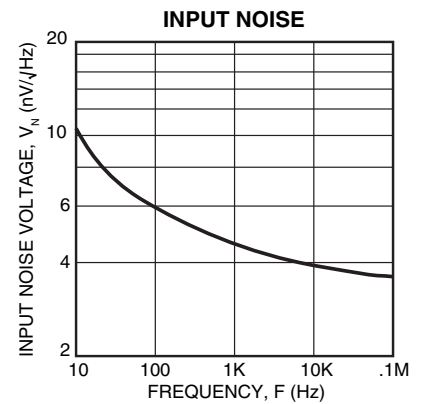
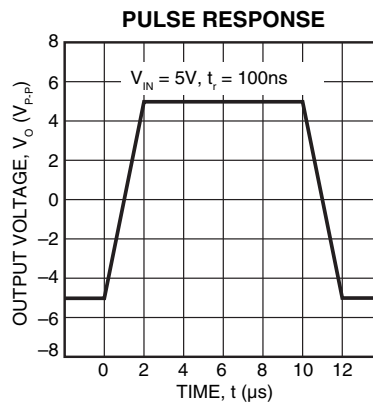
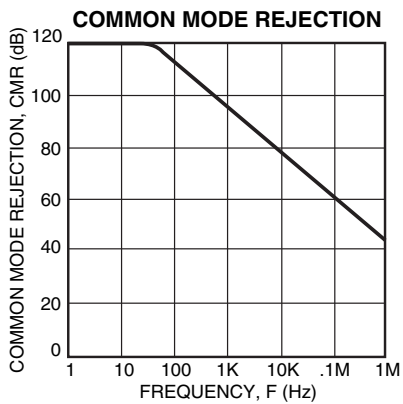
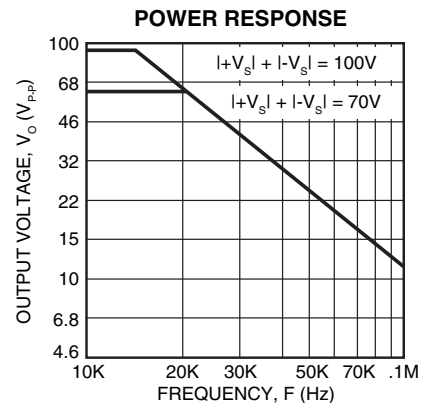
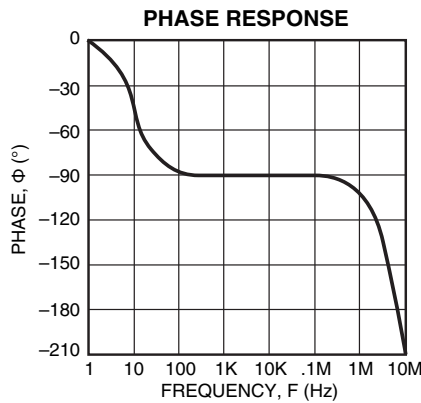
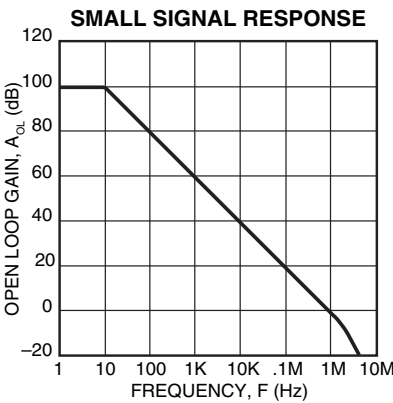
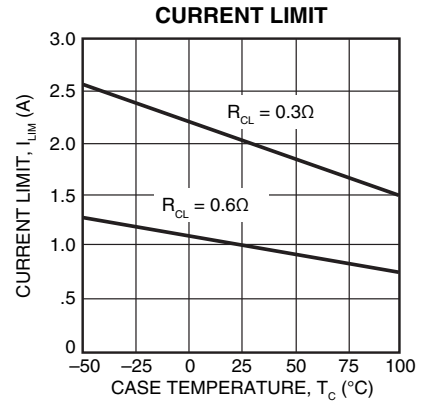
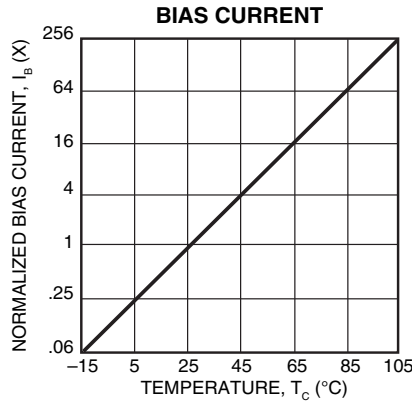
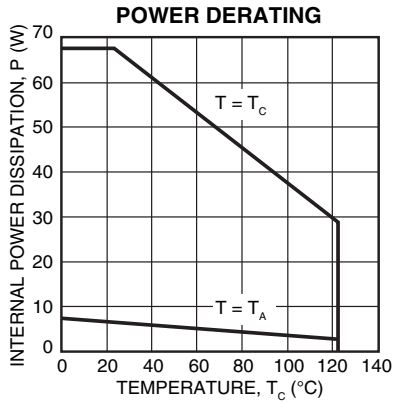
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|--|-----------------|
| SUPPLY VOLTAGE, +V <sub>S</sub> to -V <sub>S</sub> | 100V            |
| OUTPUT CURRENT, within SOA                         | 5A              |
| POWER DISSIPATION, internal <sup>1</sup>           | 67W             |
| INPUT VOLTAGE, differential                        | ±50V            |
| INPUT VOLTAGE, common mode                         | ±V <sub>S</sub> |
| TEMPERATURE, pin solder - 10s                      | 350°C           |
| TEMPERATURE, junction <sup>1</sup>                 | 200°C           |
| TEMPERATURE RANGE, storage                         | -65 to +150°C   |
| OPERATING TEMPERATURE RANGE, case                  | -55 to +125°C   |

**SPECIFICATIONS**

| PARAMETER                                     | TEST CONDITIONS <sup>2</sup>                   | PA07                |                  |     | PA07A |      |     | UNITS |
|---|--|---------------------|------------------|-----|-------|------|-----|-------|
|   |  | MIN                 | TYP              | MAX | MIN   | TYP  | MAX |       |
| <b>INPUT</b>                                  |  |                     |                  |     |       |      |     |       |
| OFFSET VOLTAGE, initial                       | T <sub>C</sub> = 25°C                          |                     | .5               | ±2  |       | ±.25 | ±.5 | mV    |
| OFFSET VOLTAGE, vs. temperature               | Full temperature range                         |                     | 10               | 30  |       | 5    | 10  | μV/°C |
| OFFSET VOLTAGE, vs. supply                    | T <sub>C</sub> = 25°C                          |                     | 8                |     |       | *    |     | μV/V  |
| OFFSET VOLTAGE, vs. power                     | Full temperature range                         |                     | 20               |     |       | 10   |     | μV/W  |
| BIAS CURRENT, initial <sup>3</sup>            | T <sub>C</sub> = 25°C                          |                     | 5                | 50  |       | 3    | 10  | pA    |
| BIAS CURRENT, vs. supply                      | T <sub>C</sub> = 25°C                          |                     | .01              |     |       | *    |     | pA/V  |
| OFFSET CURRENT, initial <sup>3</sup>          | T <sub>C</sub> = 25°C                          |                     | 2.5              | 50  |       | 1.5  | 10  | pA    |
| INPUT IMPEDANCE, DC                           | T <sub>C</sub> = 25°C                          |                     | 10 <sup>11</sup> |     |       | *    |     | Ω     |
| INPUT CAPACITANCE                             | T <sub>C</sub> = 25°C                          |                     | 4                |     |       | *    |     | pF    |
| COMMON MODE VOLTAGE RANGE <sup>4</sup>        | Full temperature range                         | ±V <sub>S</sub> -10 |                  |     | *     |      |     | V     |
| COMMON MODE REJECTION, DC                     | Full temperature range, V <sub>CM</sub> = ±20V |                     | 120              |     |       | *    |     | dB    |
| <b>GAIN</b>                                   |  |                     |                  |     |       |      |     |       |
| OPEN LOOP GAIN at 15Hz                        | T <sub>C</sub> = 25°C, R <sub>L</sub> = 15Ω    | 89                  | 95               |     | *     | *    |     | dB    |
| GAIN BANDWIDTH PRODUCT @ 1MHz                 | T <sub>C</sub> = 25°C, R <sub>L</sub> = 15Ω    |                     | 1.3              |     |       | *    |     | MHz   |
| POWER BANDWIDTH                               | T <sub>C</sub> = 25°C, R <sub>L</sub> = 15Ω    |                     | 18               |     |       | *    |     | kHz   |
| PHASE MARGIN                                  | Full temperature range, R <sub>L</sub> = 15Ω   |                     | 70               |     |       | *    |     | °     |
| <b>OUTPUT</b>                                 |  |                     |                  |     |       |      |     |       |
| VOLTAGE SWING <sup>4</sup>                    | Full temp. range, I <sub>O</sub> = 5A          | ±V <sub>S</sub> -5  |                  |     | *     |      |     | V     |
| VOLTAGE SWING <sup>4</sup>                    | Full temp. range, I <sub>O</sub> = 2A          | ±V <sub>S</sub> -5  |                  |     | *     |      |     | V     |
| VOLTAGE SWING <sup>4</sup>                    | Full temp. range, I <sub>O</sub> = 90mA        | ±V <sub>S</sub> -5  |                  |     | *     |      |     | V     |
| CURRENT, peak                                 | T <sub>C</sub> = 25°C                          | 5                   |                  |     | *     |      |     | A     |
| SETTLING TIME to .1%                          | T <sub>C</sub> = 25°C, 2V step                 |                     | 1.5              |     |       | *    |     | μs    |
| SLEW RATE                                     | T <sub>C</sub> = 25°C                          |                     | 5                |     |       | *    |     | V/μs  |
| CAPACITIVE LOAD, unity gain                   | Full temperature range                         |                     |                  | 1   |       |      | *   | nF    |
| CAPACITIVE LOAD, gain>4                       | Full temperature range                         |                     |                  | SOA |       |      | *   |       |
| <b>POWER SUPPLY</b>                           |  |                     |                  |     |       |      |     |       |
| VOLTAGE                                       | Full temperature range                         | ±12                 | ±35              | ±50 | *     | *    | *   | V     |
| CURRENT, quiescent                            | T <sub>C</sub> = 25°C                          |                     | 18               | 30  |       | *    | *   | mA    |
| <b>THERMAL</b>                                |  |                     |                  |     |       |      |     |       |
| RESISTANCE, AC, junction to case <sup>5</sup> | F>60Hz   |                     | 1.9              | 2.1 |       | *    | *   | °C/W  |
| RESISTANCE, DC, junction to case              | F<60Hz   |                     | 2.4              | 2.6 |       | *    | *   | °C/W  |
| RESISTANCE, junction to air                   |  |                     | 30               |     |       | *    | *   | °C/W  |
| TEMPERATURE RANGE, case                       | Meets full range specifications                | -25                 | 25               | +85 | *     | *    | *   | °C    |

- NOTES: \* The specification of PA07A is identical to the specification for PA07 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
  2. The power supply voltage for all specifications is the TYP rating unless otherwise noted as a test condition.
  3. Doubles for every 10°C of temperature increase.
  4. +V<sub>S</sub> and -V<sub>S</sub> denote the positive and negative supply rail respectively. Total V<sub>S</sub> is measured from +V<sub>S</sub> to -V<sub>S</sub>.
  5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

**CAUTION** The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.



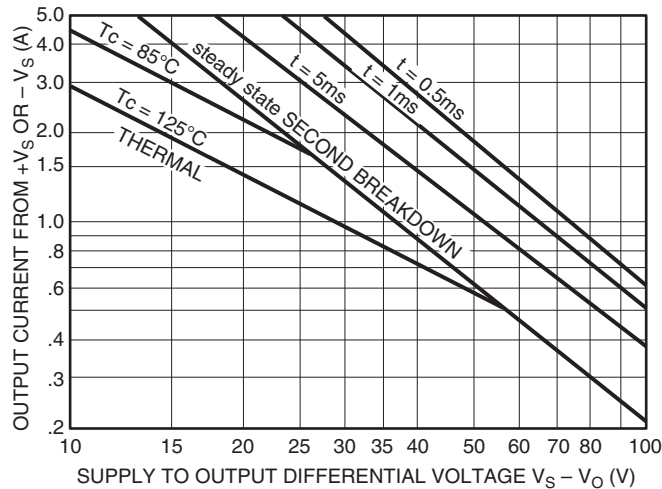
**GENERAL**

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit [www.Cirrus.com](http://www.Cirrus.com) for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex Precision Power's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

**SAFE OPERATING AREA (SOA)**

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceed specified limits.
3. The junction temperature of the output transistors.



**SAFE OPERATING AREA CURVES**

The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts.

1. For DC outputs, especially those resulting from fault conditions, check worst case stress levels against the SOA graph. Make sure the load line does not cross the 0.5ms limit and that excursions beyond any other second breakdown line do not exceed the time label, and have a duty cycle of no more than 10%.

A Spice type analysis can be very useful in that a hardware setup often calls for instruments or amplifiers with wide common mode rejection ranges. Please refer to Application Notes, AN01 and AN22 for detailed information regarding SOA considerations.

2. The amplifier can handle any reactive or EMF generating load and short circuits to the supply rail or common if the current limits are set as follows at  $T_c = 85^\circ\text{C}$ :

| $\pm V_s$ | SHORT TO $\pm V_s$<br>C, L, OR EMF LOAD | SHORT TO<br>COMMON |
|-----------|---|--------------------|
| 50V       | .21A                                    | .61A               |
| 40V       | .3A                                     | .87A               |
| 30V       | .46A                                    | 1.4A               |
| 20V       | .87A                                    | 2.5A               |
| 15V       | 1.4A                                    | 4.0A               |

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

**THERMAL SHUTDOWN PROTECTION**

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds approximately  $150^\circ\text{C}$ . This allows heatsink selection to be based on normal operating conditions while protecting the amplifier against excessive junction temperature during temporary fault conditions.

Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the  $T_c = 25^\circ\text{C}$  boundary). It is designed to protect against short-term fault conditions that result in high power dissipation within the amplifier. If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, will destroy signal integrity and reduce the reliability of the device.

**CURRENT LIMIT**

Proper operation requires the use of two current limit resistors, connected as shown in the external connections diagram. The minimum value for  $R_{CL}$  is  $.12\Omega$ , however, for optimum reliability it should be set as high as possible. Refer to the "General Operating Considerations" section of the handbook for current limit adjust details.

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## CONTACTING CIRRUS LOGIC SUPPORT

For all Apex Precision Power product questions and inquiries, call toll free 800-546-2739 in North America.

For inquiries via email, please contact [apex.support@cirrus.com](mailto:apex.support@cirrus.com).

International customers can also request support by contacting their local Cirrus Logic Sales Representative.

To find the one nearest to you, go to [www.cirrus.com](http://www.cirrus.com)

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