1.8-V MICROPOWER CMOS OPERATIONAL AMPLIFIER ZERO-DRIFT SERIES

Check for Samples: OPA2333-HT

FEATURES

- **Low Offset Voltage: 26 μV (Max)**
- **0.01-Hz to 10-Hz Noise: 1.5 μV_{PP}**
- **Quiescent Current: 50 μA**
- **Single-Supply Operation**
- **Supply Voltage: 1.8 V to 5.5 V**
- **Rail-to-Rail Input/Output**

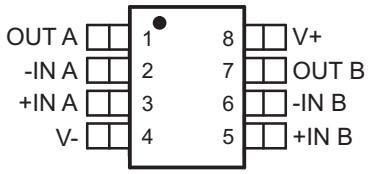
APPLICATIONS

- **Down-Hole Drilling**
- **High Temperature Environments**

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Extreme (–55°C/210°C) Temperature Range**(1)
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**
- **Texas Instruments' high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.**

D OR JD OR HKJ PACKAGE
(TOP VIEW)



(1) Custom temperature ranges available

DESCRIPTION/ORDERING INFORMATION(2)

The OPA2333 series of CMOS operational amplifiers uses a proprietary auto-calibration technique to simultaneously provide very low offset voltage and near-zero drift over time and temperature. These miniature, high-precision, low-quiescent-current amplifiers offer high-impedance inputs that have a common-mode range 100 mV beyond the rails, and rail-to-rail output that swings within 150 mV of the rails. Single or dual supplies as low as 1.8 V (±0.9 V) and up to 5.5 V (±2.75 V) may be used. They are optimized for low-voltage single-supply operation.

The OPA2333 family offers excellent common-mode rejection ratio (CMRR) without the crossover associated with traditional complementary input stages. This design results in superior performance for driving analog-to-digital converters (ADCs) without degradation of differential linearity.

(2) Refer to Electrical Characteristics for performance degradation over temperature.

Table 1. ORDERING INFORMATION(1)

TA	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 210°C	KGD	OPA2333SKGD1	NA
	JD	OPA2333SJD	OPA2333SJD
	HKJ	OPA2333SHKJ	OPA2333SHKJ
–55°C to 175°C	D	OPA2333HD	O2333H

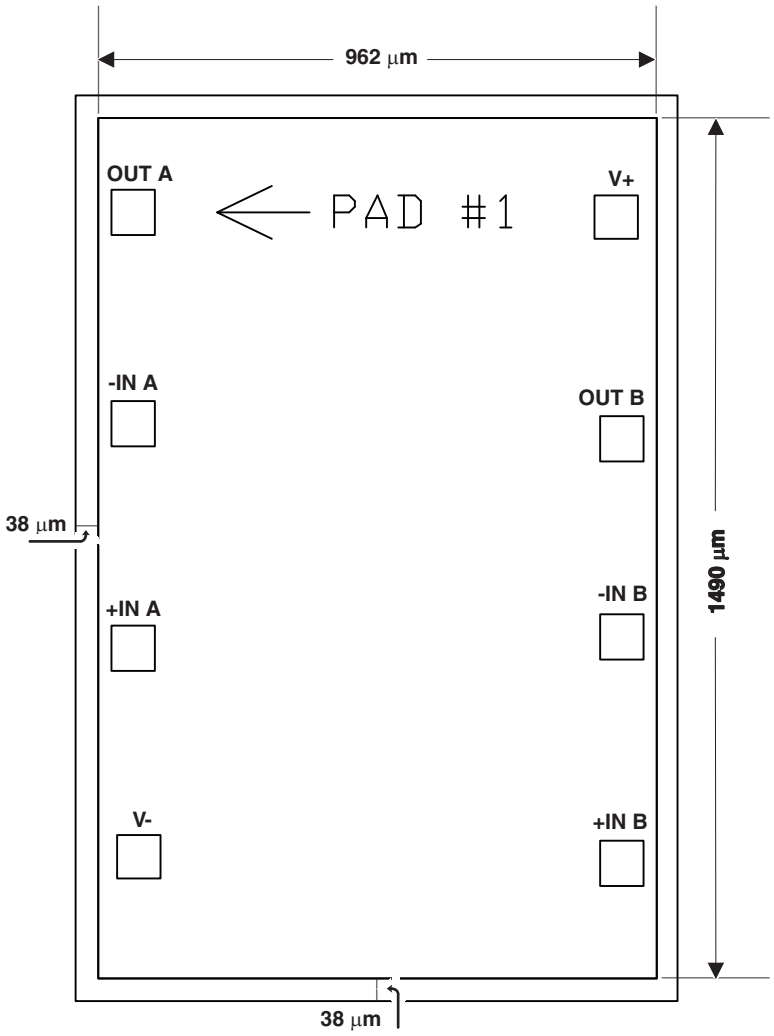
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION
15 mils.	Silicon with backgrind	V-	Al-Si-Cu (0.5%)

Table 2. BOND PAD COORDINATES

DESCRIPTION	PAD NUMBER	a	b	c	d
OUT A	1	21.20	1288.50	97.20	1364.50
–IN A	2	21.20	923.65	97.20	999.65
+IN A	3	21.20	533.05	97.20	609.05
V–	4	31.30	172.20	107.30	248.20
+IN B	5	864.80	162.25	940.80	238.25
–IN B	6	864.80	552.65	940.80	628.65
OUT B	7	864.80	897.10	940.80	973.10
V+	8	854.70	1280.45	930.70	1356.45


962 µm
OUT A
PAD #1
V+
-IN A
OUT B
38 µm
1490 µm
+IN A
-IN B
V-
+IN B
38 µm

THERMAL CHARACTERISTICS FOR JD PACKAGE

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-ambient thermal resistance(1)	High-K board(2), no airflow		64.9		°C/W
		No airflow		83.4		
θ_{JB}	Junction-to-board thermal resistance	High-K board without underfill		27.9		°C/W
θ_{JC}	Junction-to-case thermal resistance			6.49		°C/W

(1) The intent of θ_{JA} specification is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.
(2) JED51-7, high effective thermal conductivity test board for leaded surface mount packages

THERMAL CHARACTERISTICS FOR HKJ PACKAGE

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
θ_{JC}	Junction-to-case thermal resistance (to bottom of case)			5.7	°C/W
	Junction-to-case thermal resistance (to top of case lid - as if formed dead bug)			13.7	

THERMAL CHARACTERISTICS FOR D PACKAGE

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
θ_{JC}	Junction-to-case thermal resistance (to bottom of case)			39.4	°C/W

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage			7	V
Signal input terminals, voltage(2)		–0.3	(V+) + 0.3	V
Output short circuit(3)			Continuous	
Operating temperature range	JD, HKJ packages	–55	210	°C
	D package	–55	175	
Junction temperature	JD, HKJ packages		210	°C
	D package		175	
ESD rating	Human-Body Model (HBM)		4000	V
	Charged-Device Model (CDM)		1000	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short circuit to ground, one amplifier per package.

Electrical Characteristics: V_S = 1.8 V to 5.5 V

Boldface limits apply over the specified temperature range, **T_A = –55°C to 210°C.** At T_A = 25°C, R_L = 10 kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 175°C (1)			T_A = 210°C (2)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE												
Input offset voltage	V_{OS}	V_S = 5 V		2	10							µV
over temperature					**22**			**26**			**26**	**µV**
vs temperature	**dV_{OS}/d_T**			0.02			0.05			0.05		**µV/°C**
vs power supply	**PSRR**	**V_S = 1.8 V to 5.5 V**		**1**	**6**		**1.2**	**8**		**1.7**	**11**	**µV/V**
Long-term stability (3)				See (3)								
Channel separation, dc				0.1								µV/V
INPUT BIAS CURRENT												
Input bias current	I_B			±70	±200							pA
over Temperature				**±150**			**±1250**			**±5300**		**pA**
Input offset current	I_{OS}			±140	±400		±700			±10600		pA
NOISE												
Input voltage noise, f = 0.01 Hz to 1 Hz				0.3			1.0			1.0		$µV_{PP}$
Input voltage noise, f = 0.1 Hz to 10 Hz				1.1			1.5			1.5		$µV_{PP}$
Input current noise, f = 10 Hz	i_n			100								$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE												
Common mode voltage range	V_{CM}		(V–) – 0.1		(V+) + 0.1	(V–) – 0.25		(V–) + 0.25	(V–) – 0.25		(V–) + 0.25	V
Common-Mode Rejection Ratio	CMRR	**(V–) – 0.1 V < V_{CM} < (V+) + 0.1 V**	**102**	**130**		**101**			**91**			**dB**
INPUT CAPACITANCE												
Differential				2			4.25			4.25		pF
Common mode				4			12.25			12.25		pF
OPEN-LOOP GAIN												
Open-loop voltage gain	**A_{OL}**	**(V–) + 100 mV < V_O < (V+) – 100 mV, R_L = 10 kΩ**	**104**	**130**		**93**	**110**		**85**	**93**		**dB**
FREQUENCY RESPONSE												
Gain-bandwidth product	GBW	C_L = 100 pF		350			350			350		kHz
Slew rate	SR	G = 1		0.16			0.25			0.25		V/µs

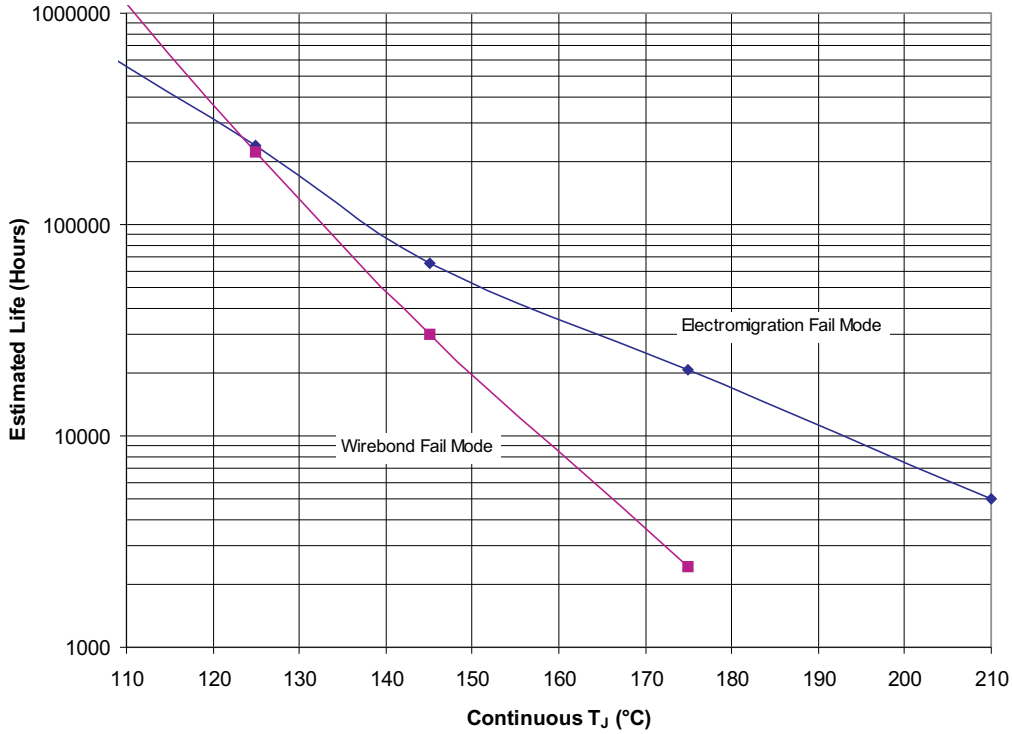
(1) Minimum and maximum parameters are characterized for operation at T_A = 175°C, but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
(2) Minimum and maximum parameters are characterized for operation at T_A = 210°C, but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
(3) 300-hour life test at 150°C demonstrated randomly distributed variation of approximately 1 µV.

Electrical Characteristics: V_S = 1.8 V to 5.5 V (continued)

Boldface limits apply over the specified temperature range, **T_A = –55°C to 210°C.** At T_A = 25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2 (unless otherwise noted).

PARAMETER		TEST CONDITIONS	T_A = –55°C to 125°C			T_A = 175°C (1)			T_A = 210°C (2)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT												
Voltage output swing from rail		R_L = 10 kΩ		30	50							mV
over temperature		**R_L = 10 kΩ**			**85**			**110**			**150**	**mV**
Short-circuit current	ISC			±5								mA
Capacitive load drive	CL											
(4)Open-loop output impedance		f = 350 kHz, I_O = 0		2								kΩ
POWER SUPPLY												
Specified voltage range	V_S		1.8		5.5	1.8		5.5	1.8		5.5	V
Quiescent current per amplifier	I_Q	I_O = 0		17	25							µA
over temperature					**30**		**35**	**40**		**50**	**80**	**µA**
Turn-on time		V_S = 5 V		100								µs
TEMPERATURE RANGE												
Specified range			-55 to 210			-55 to 175			-55 to 210			°C
Operating range			-55 to 210			-55 to 175			-55 to 210			°C

(4) See Typical Characteristics.



(1) See datasheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

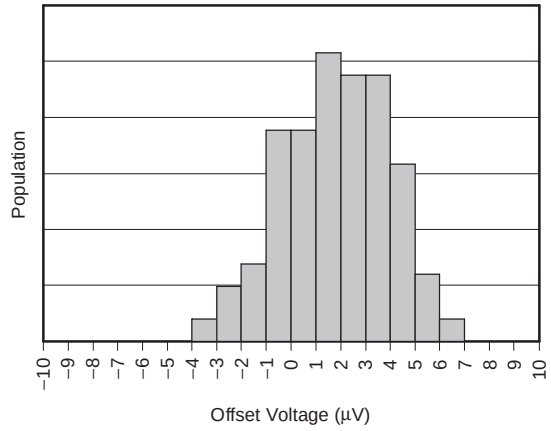
(4) Wirebond fail mode applicable for D package only.

Figure 1. OPA2333SKGD1/OPA2333HD Operating Life Derating Chart

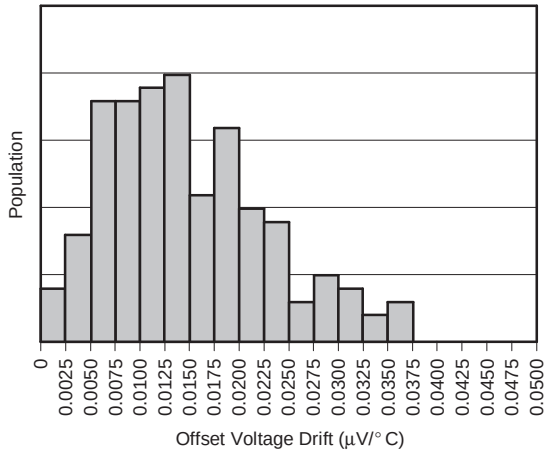
TYPICAL CHARACTERISTICS

At T_A = 25°C, V_S = 5 V, and C_L = 0 pF (unless otherwise noted).

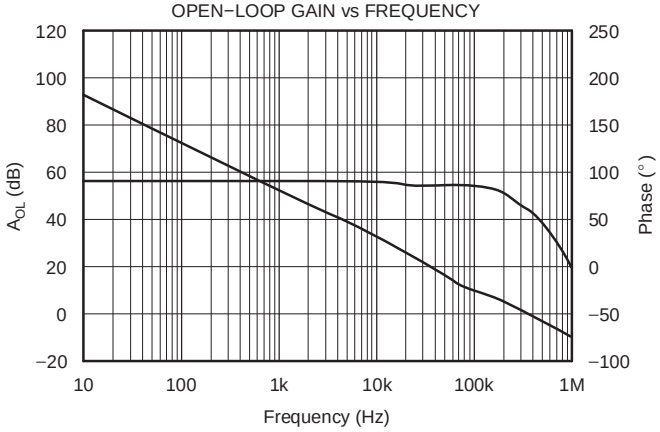
OFFSET VOLTAGE PRODUCTION DISTRIBUTION



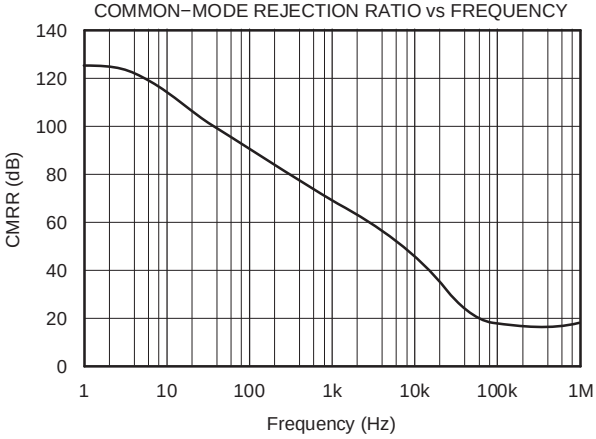
OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION



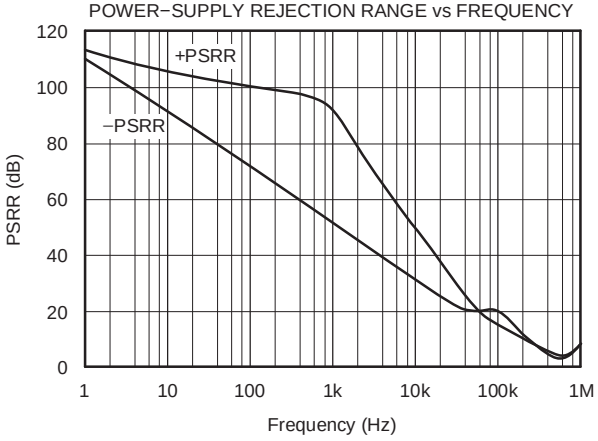
OPEN−LOOP GAIN vs FREQUENCY



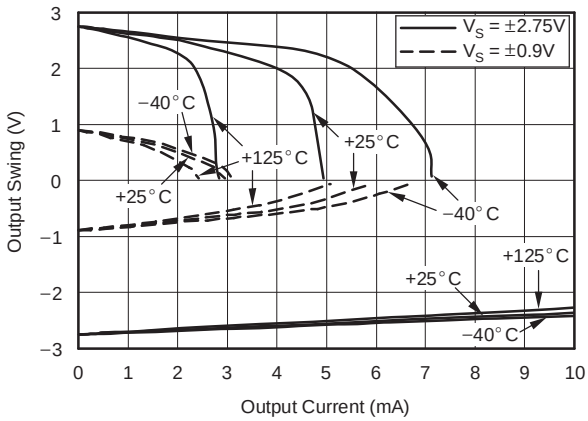
COMMON−MODE REJECTION RATIO vs FREQUENCY



POWER−SUPPLY REJECTION RANGE vs FREQUENCY

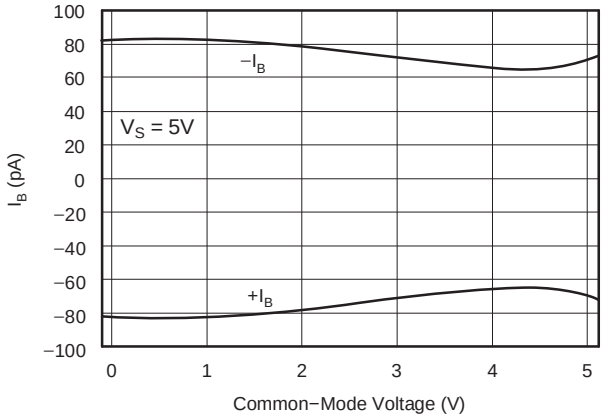


OUTPUT VOLTAGE SWING vs OUTPUT CURRENT

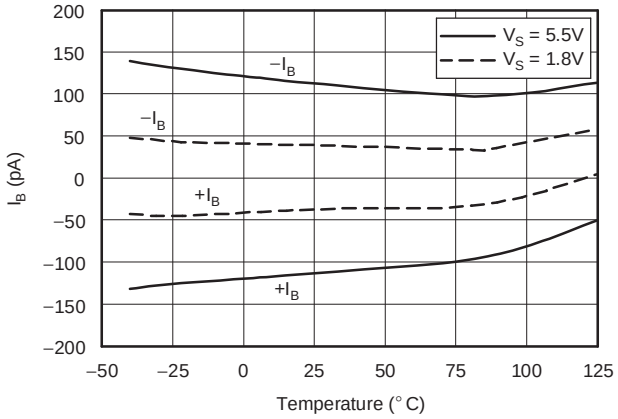


TYPICAL CHARACTERISTICS (continued)

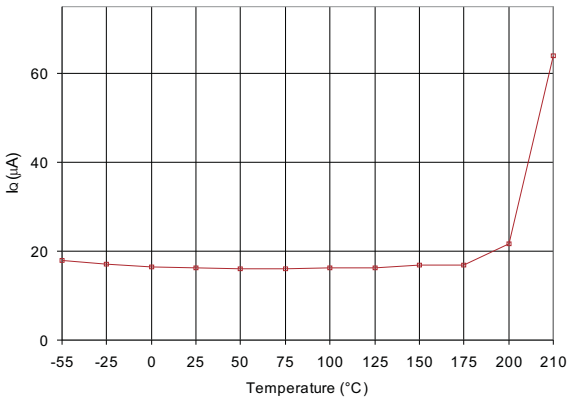
INPUT BIAS CURRENT vs COMMON−MODE VOLTAGE



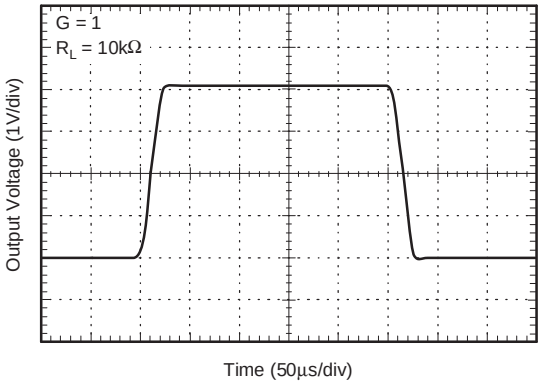
INPUT BIAS CURRENT vs TEMPERATURE



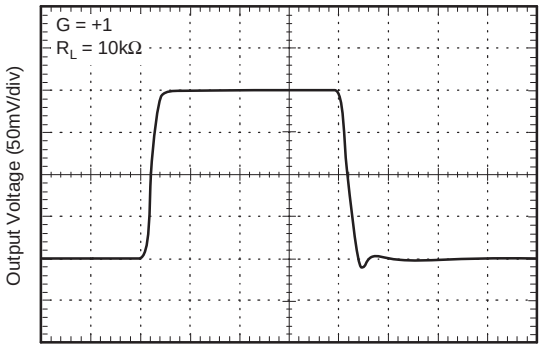
QUIESCENT CURRENT vs TEMPERATURE



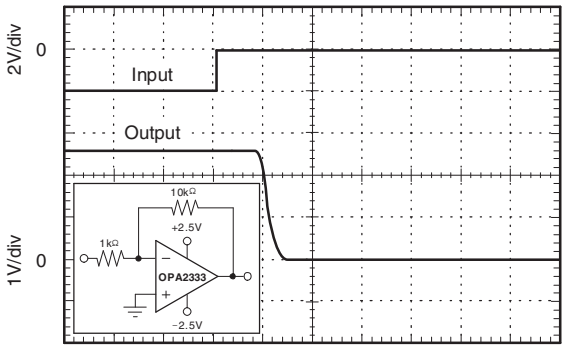
LARGE−SIGNAL STEP RESPONSE



SMALL−SIGNAL STEP RESPONSE

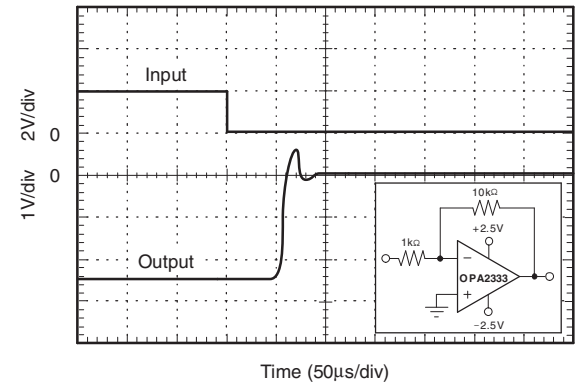


POSITIVE OVER- VOLTAGE RECOVERY

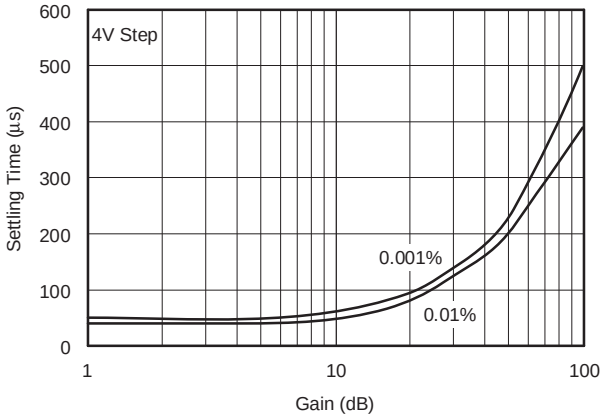


TYPICAL CHARACTERISTICS (continued)

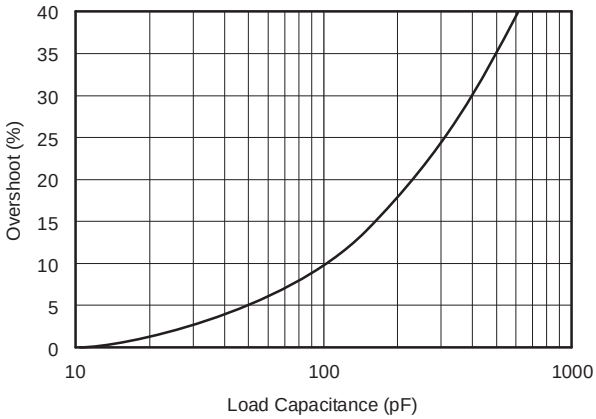
NEGATIVE OVER- VOLTAGE RECOVERY



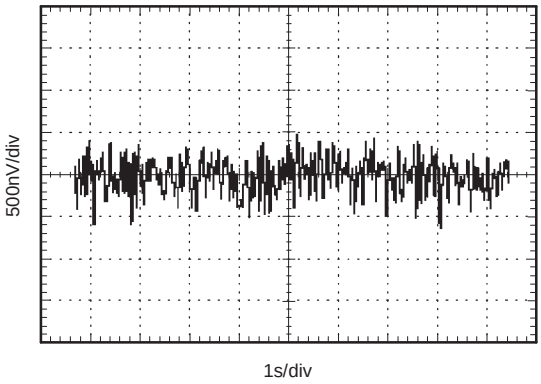
SETTLING TIME vs CLOSED−LOOP GAIN



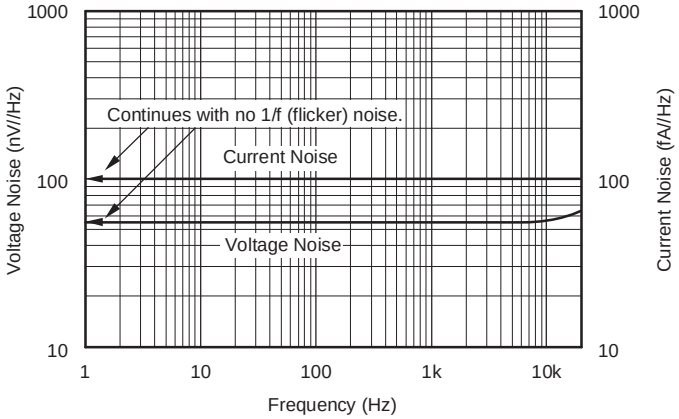
SMALL−SIGNAL OVERSHOOT vs LOAD CAPACITANCE



0.1Hz TO 10Hz NOISE



CURRENT AND VOLTAGE NOISE SPECTRAL DENSITY vs FREQUENCY



APPLICATION INFORMATION(1)

The OPA2333 is unity-gain stable and free from unexpected output phase reversal. It uses a proprietary auto-calibration technique to provide low offset voltage and very low drift over time and temperature. For lowest offset voltage and precision performance, circuit layout and mechanical conditions should be optimized. Avoid temperature gradients that create thermoelectric (Seebeck) effects in the thermocouple junctions formed from connecting dissimilar conductors. These thermally-generated potentials can be made to cancel by ensuring they are equal on both input terminals. Other layout and design considerations include:

- Use low thermoelectric-coefficient conditions (avoid dissimilar metals)
- Thermally isolate components from power supplies or other heat sources
- Shield op amp and input circuitry from air currents, such as cooling fans

Following these guidelines will reduce the likelihood of junctions being at different temperatures, which can cause thermoelectric voltages of 0.1 μV/°C or higher, depending on materials used.

Operating Voltage

The OPA2333 op amp operates over a power-supply range of 1.8 V to 5.5 V (±0.9 V to ±2.75 V). Supply voltages higher than 7 V (absolute maximum) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

Input Voltage

The OPA2333 input common-mode voltage range extends 0.1 V beyond the supply rails. The OPA2333 is designed to cover the full range without the troublesome transition region found in some other rail-to-rail amplifiers.

Normally, input bias current is about 70 pA; however, input voltages exceeding the power supplies can cause excessive current to flow into or out of the input pins. Momentary voltages greater than the power supply can be tolerated if the input current is limited to 10 mA. This limitation is easily accomplished with an input resistor(see Figure 2).

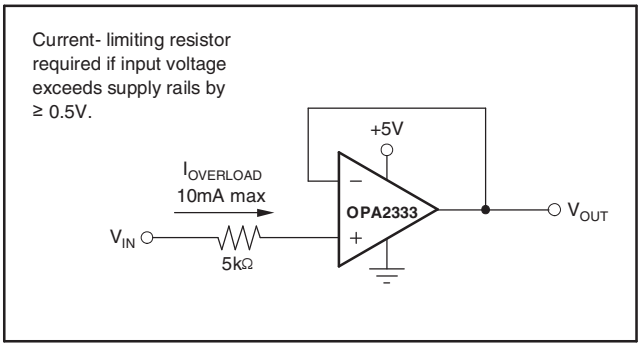


Figure 2. Input Current Protection

Internal Offset Correction

The OPA2333 op amp uses an auto-calibration technique with a time-continuous 350-kHz op amp in the signal path. This amplifier is zero corrected every 8 μs using a proprietary technique. Upon power up, the amplifier requires approximately 100 μs to achieve specified V_{OS} accuracy. This design has no aliasing or flicker noise.

(1) At T_A = 25°C (unless otherwise noted).

Achieving Output Swing to the Op Amp Negative Rail

Some applications require output voltage swings from 0 V to a positive full-scale voltage (such as 2.5 V) with excellent accuracy. With most single-supply op amps, problems arise when the output signal approaches 0 V, near the lower output swing limit of a single-supply op amp. A good single-supply op amp may swing close to single-supply ground, but will not reach ground. The output of the OPA2333 can be made to swing to ground, or slightly below, on a single-supply power source. To do so requires the use of another resistor and an additional, more negative, power supply than the op amp negative supply. A pulldown resistor may be connected between the output and the additional negative supply to pull the output down below the value that the output would otherwise achieve (see Figure 3).

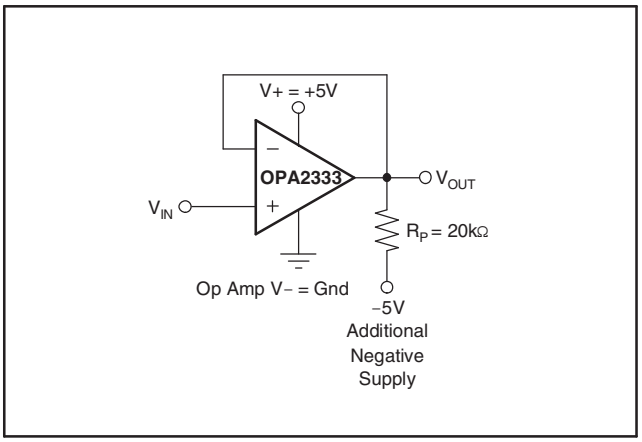


Figure 3. V_{OUT} Range to Ground

The OPA2333 has an output stage that allows the output voltage to be pulled to its negative supply rail, or slightly below, using the technique previously described. This technique only works with some types of output stages. The OPA2333 has been characterized to perform with this technique; however, the recommended resistor value is approximately 20 kΩ. Note that this configuration will increase the current consumption by several hundreds of microamps. Accuracy is excellent down to 0 V and as low as –2 mV. Limiting and nonlinearity occurs below –2 mV, but excellent accuracy returns as the output is again driven above –2 mV. Lowering the resistance of the pulldown resistor allows the op amp to swing even further below the negative rail. Resistances as low as 10 kΩ can be used to achieve excellent accuracy down to –10 mV.

General Layout Guidelines

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-μF capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

Operational amplifiers vary in their susceptibility to radio frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. The OPA2333 has been specifically designed to minimize susceptibility to RFI and demonstrates remarkably low sensitivity compared to previous-generation devices. Strong RF fields may still cause varying offset levels.

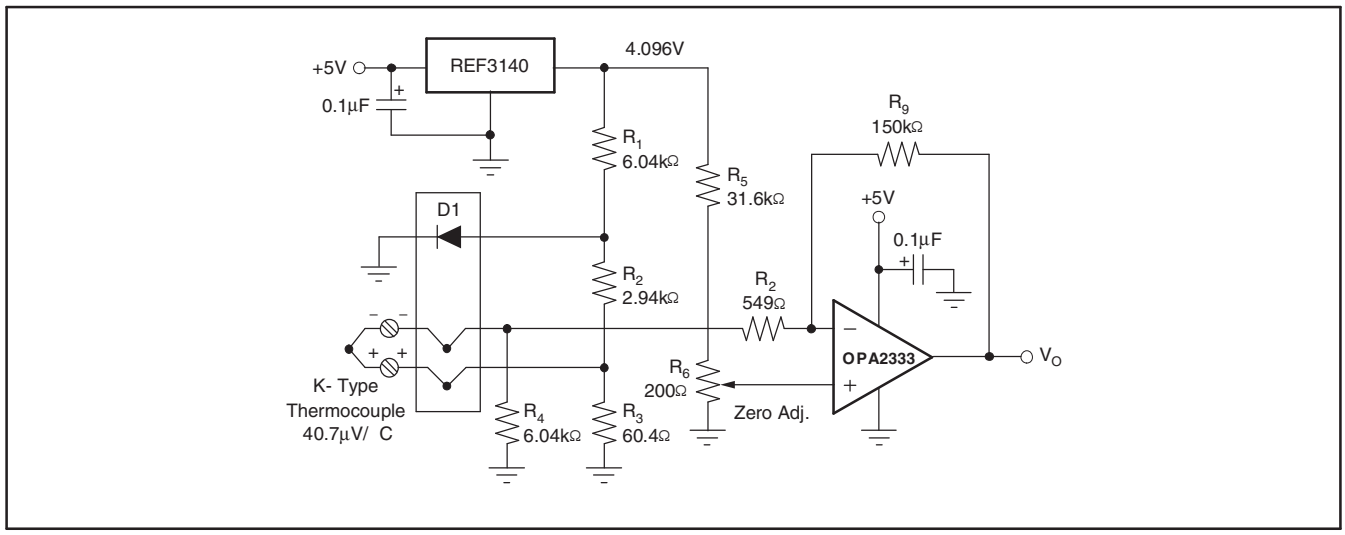


Figure 4. Temperature Measurement

Figure 5 shows the basic configuration for a bridge amplifier.

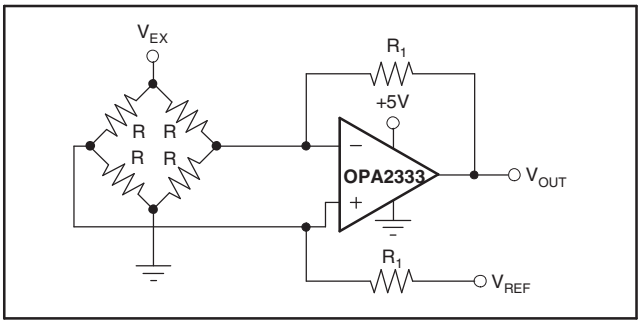


Figure 5. Single Op-Amp Bridge Amplifier

A low-side current shunt monitor is shown in Figure 6. R_N are operational resistors used to isolate the ADS1100 from the noise of the digital I^2C bus. Since the ADS1100 is a 16-bit converter, a precise reference is essential for maximum accuracy. If absolute accuracy is not required, and the 5-V power supply is sufficiently stable, the REF3130 may be omitted.

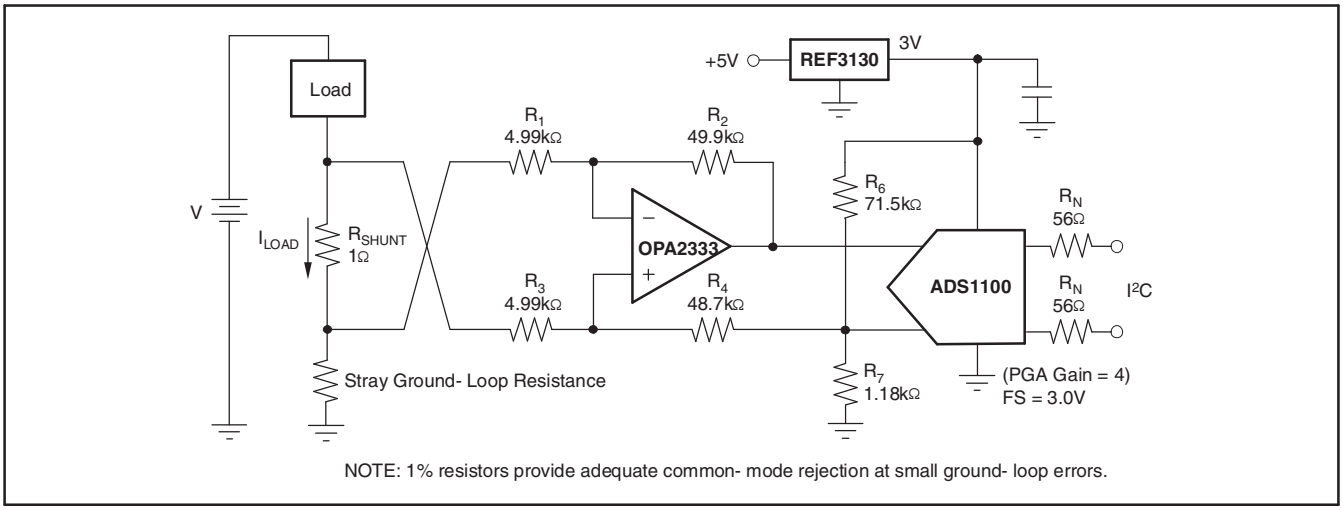


Figure 6. Low-Side Current Monitor

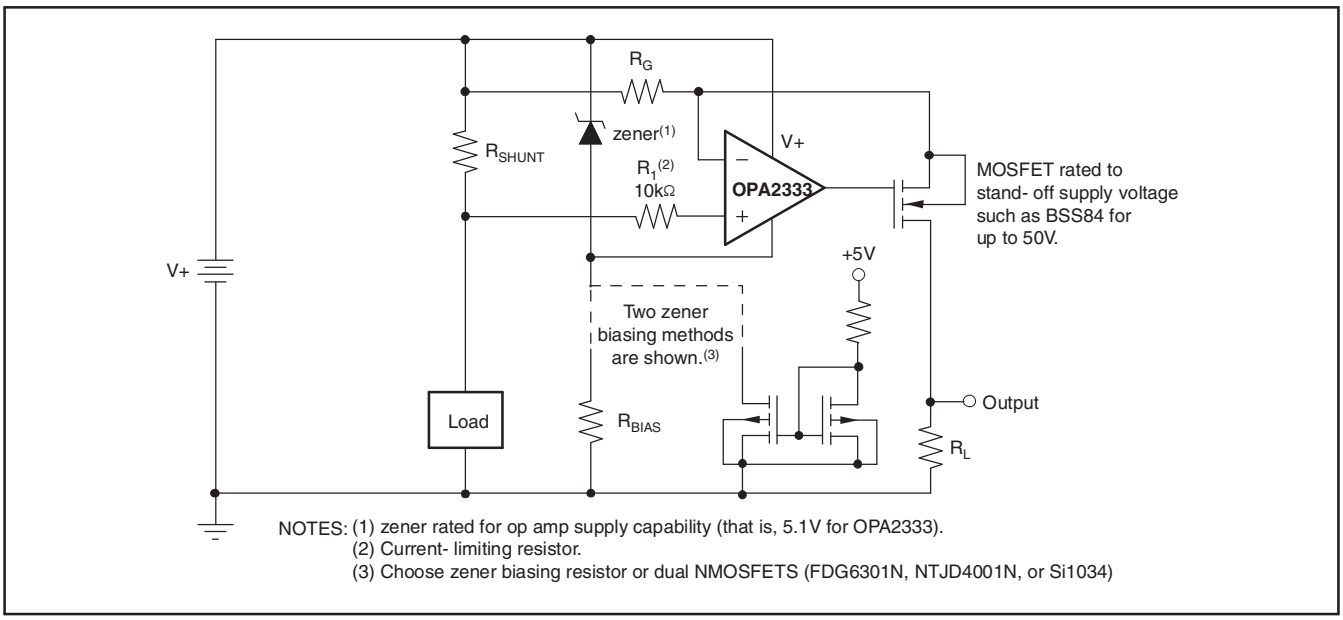


Figure 7. High-Side Current Monitor

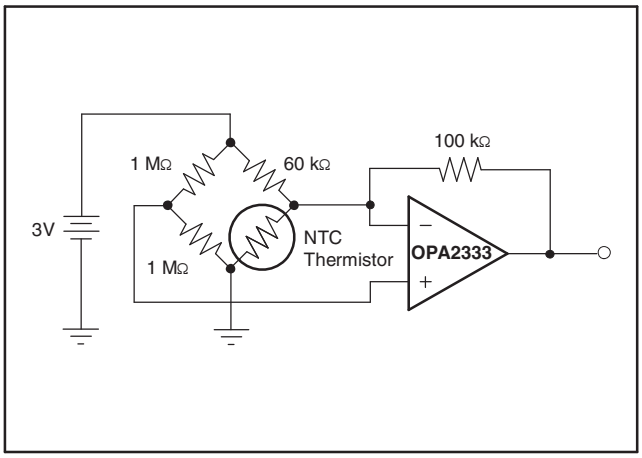


Figure 8. Thermistor Measurement

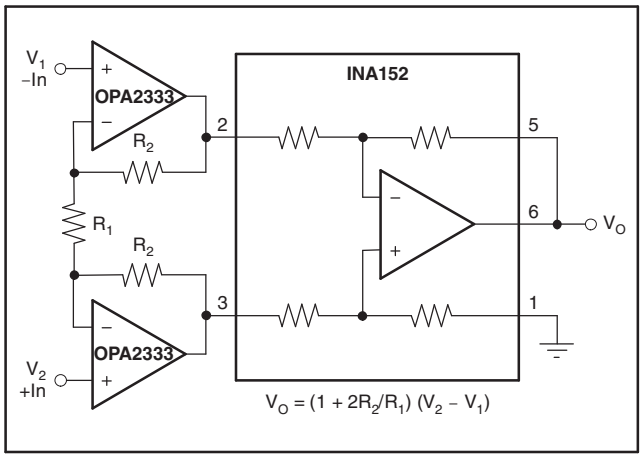


Figure 9. Precision Instrumentation Amplifier

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
OPA2333HD	PREVIEW	SOIC	D	8		TBD	Call TI	Call TI	Samples Not Available
OPA2333SHKJ	ACTIVE	CFP	HKJ	8	1	TBD	Call TI	N / A for Pkg Type	Call Local Sales Office
OPA2333SJD	ACTIVE	CDIP SB	JD	8	1	TBD	POST-PLATE	N / A for Pkg Type	Call Local Sales Office
OPA2333SKGD1	ACTIVE	XCEPT	KGD	0	100	TBD	Call TI	Call TI	Call Local Sales Office

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

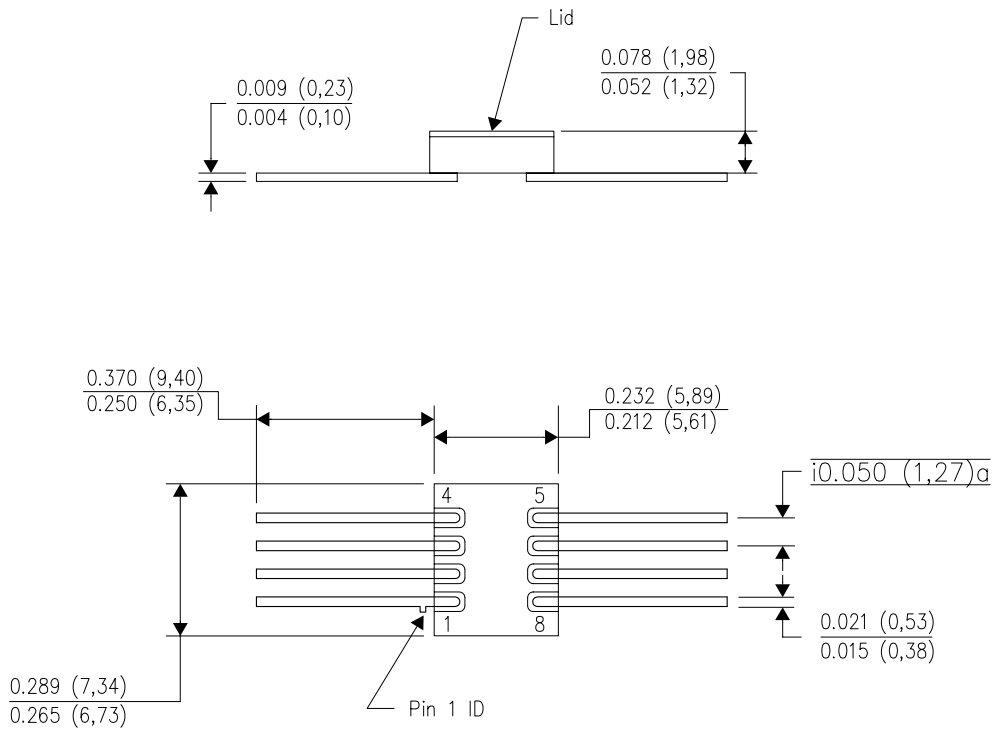
OTHER QUALIFIED VERSIONS OF OPA2333-HT :

- Catalog: OPA2333
- Automotive: OPA2333-Q1

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

HKJ (R–CDFP–F8) CERAMIC DUAL FLATPACK

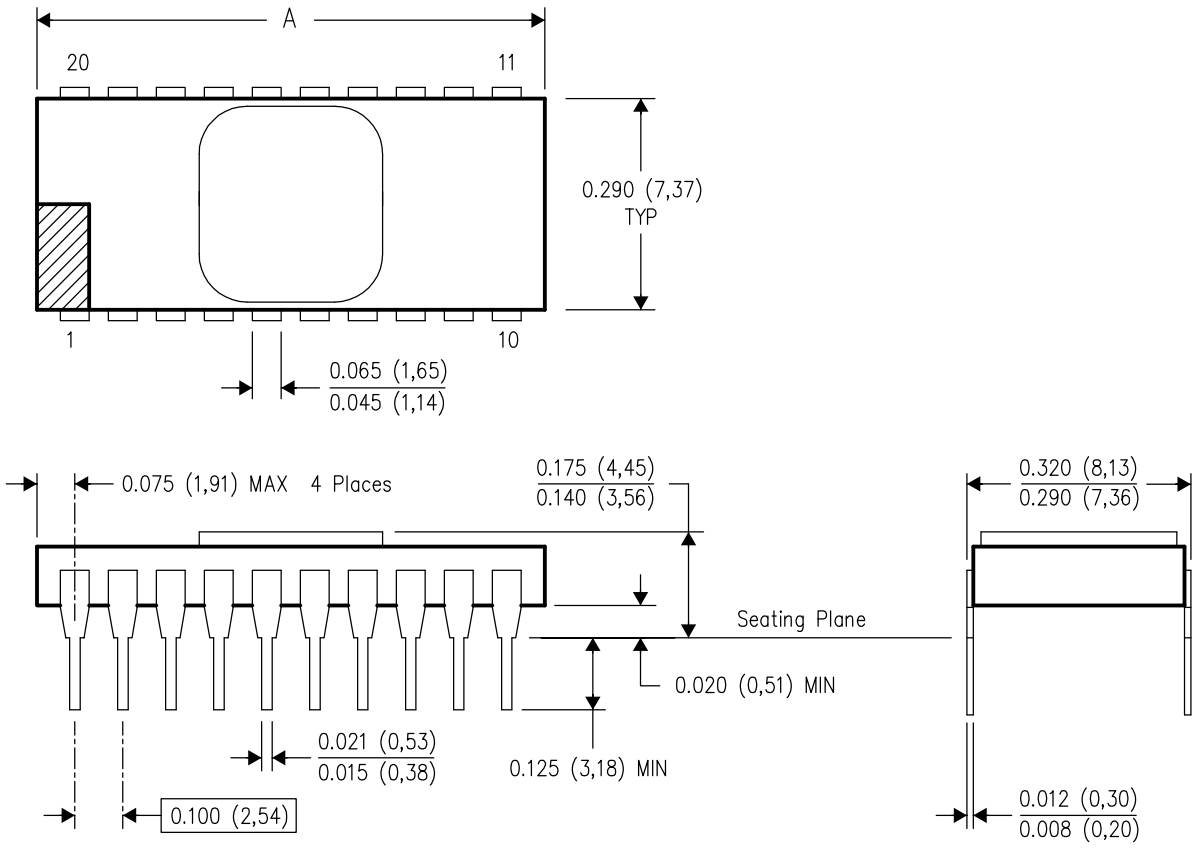


4209892/A 10/08

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.

JD (R–CDIP–T**) CERAMIC SIDE–BRAZE DUAL–IN–LINE PACKAGE

20 PINS SHOWN

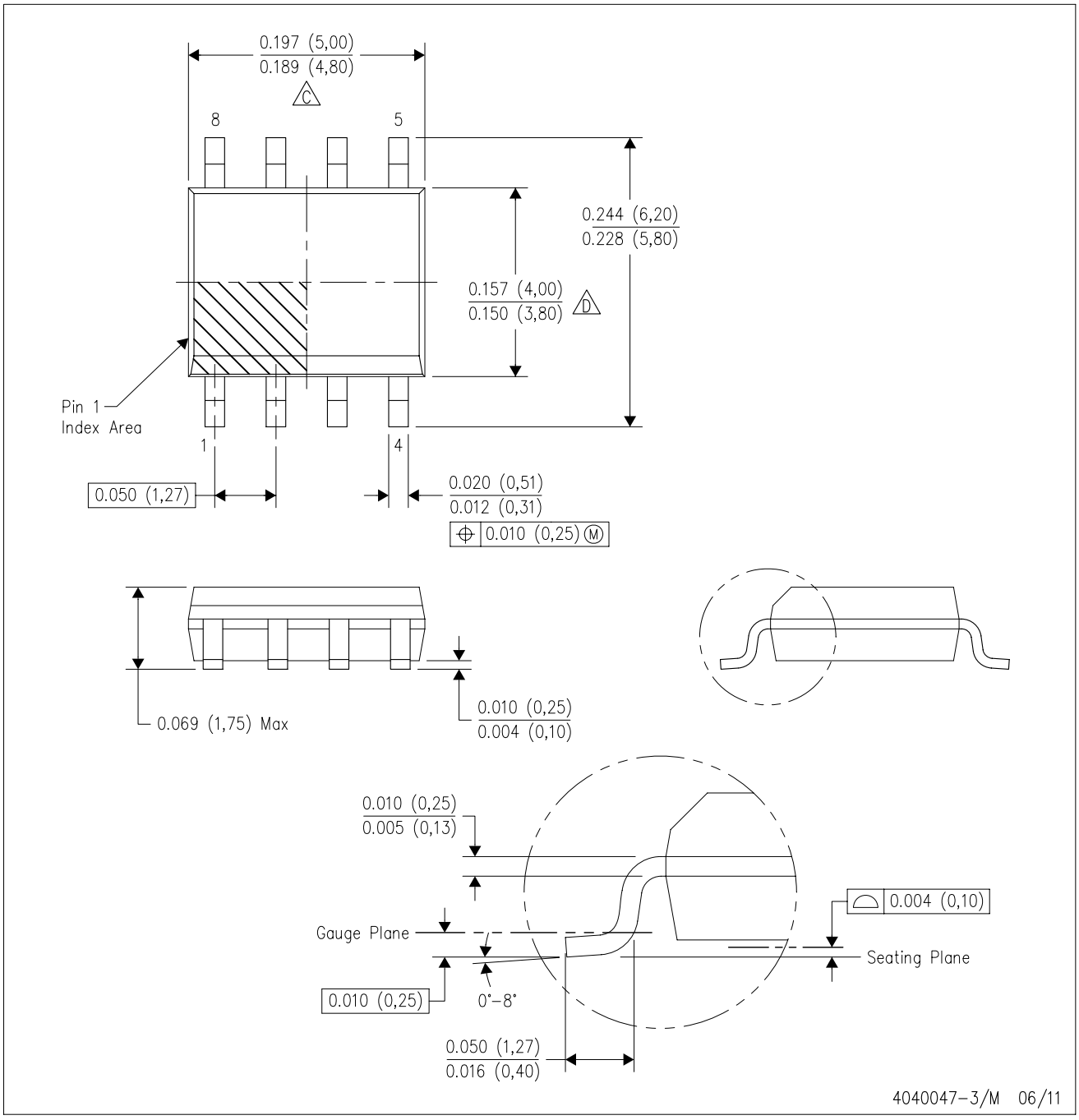


DIM \ PINS **	8	14	16	18	20	24
A MAX	0.405 (10,29)	0.757 (19,23)	0.810 (20,57)	0.910 (23,11)	1.010 (25,65)	1.100 (27,94)

4040086–2/F 07/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within MIL STD 1835 CDIP2 – T8, T14, T16, T18, T20 and T24 respectively.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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