ANALOG DEVICES

Precision Low-Input-Current Operational Amplifier

OP-12

FEATURES

- **Low Offset Voltage ..... 150μV Max**
- **Low Offset Voltage Drift ..... 2.5μV/°C Max**
- **Load Current Capability ..... 5mA Min**
- **Internal Frequency Compensation**
- **125°C Temperature Tested Die**
- **Low Offset Current ..... 200pA Max**
- **Low Bias Current ..... 2.0nA Max**
- **Low Power Consumption ..... 18mW Max @ ±15V**
- **High Common-Mode Input Range ..... ±13V Min**
- **MIL-STD-883 Class B Processing Available**
- **Silicon-Nitride Passivation**
- **Available in Die Form**

ORDERING INFORMATION †

T_A = +25°C V_{OS} MAX (mV)	PACKAGE TO-99 8-PIN	PACKAGE CERDIP 8-PIN	OPERATING TEMPERATURE RANGE
0.15	–	OP12AZ*	MIL
0.15	OP12EJ	OP12EZ	COM
0.30	OP12BJ	OP12BZ/883	MIL
0.30	OP12FJ	OP12FZ	COM
1.0	OP12GJ	–	COM

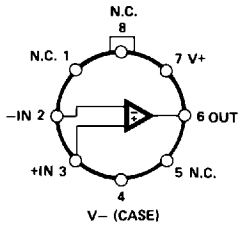
* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

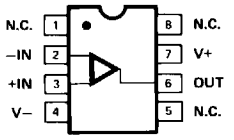
GENERAL DESCRIPTION

The PMI OP-12 is an improved version of the popular LM108A low-power op amp. The OP-12 is internally compensated and its chip dimensions are only 42 X 58 mils. Offset voltage is lower; the total worst-case input offset voltage over −55°C to +125°C for the OP-12A is only 350μV. In addition, the OP-12 drives a 2kΩ load which is five times the output current capability of the 108A. This excellent performance is achieved by applying PMI's ion-implanted super-beta process and on-chip zener-zap trimming capabilities. The internal compensation makes this op amp ideal for hybrid assembly applications.

PIN CONNECTIONS

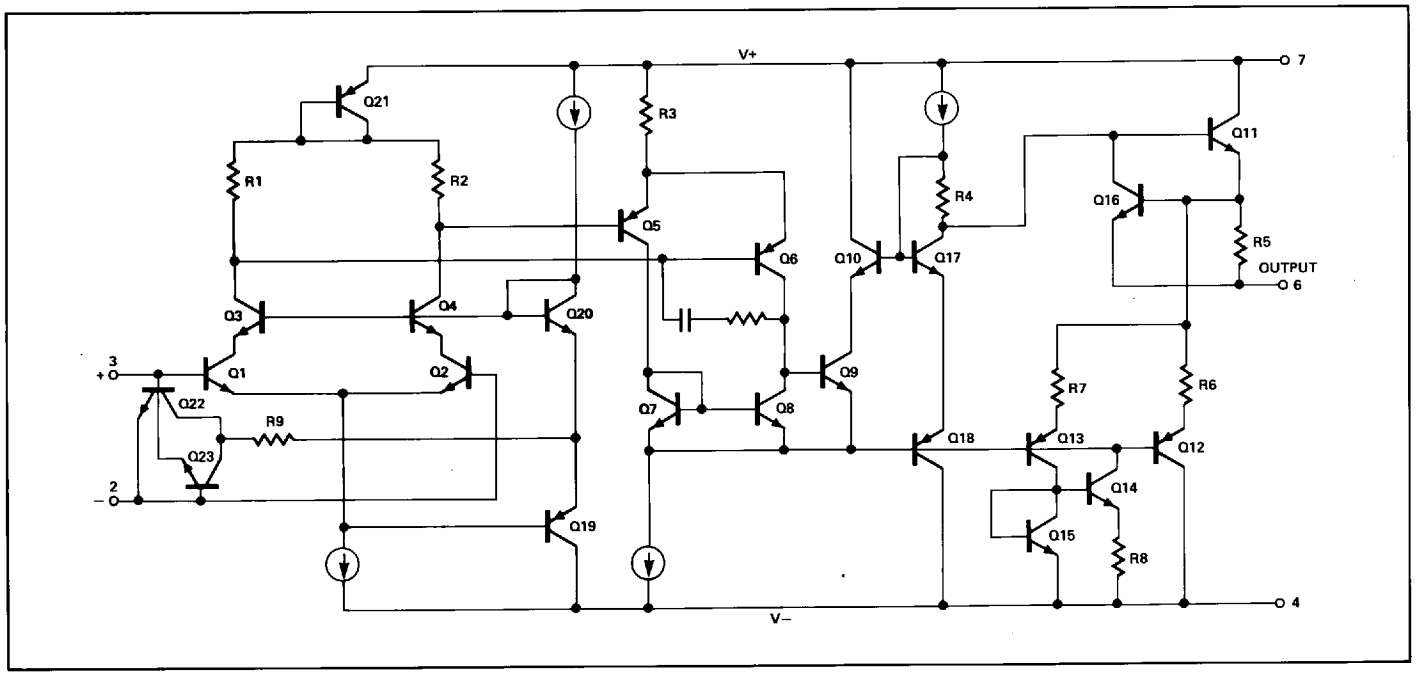


TO-99 (J-Suffix)



8-PIN HERMETIC MINI-DIP (Z-Suffix)

SIMPLIFIED SCHEMATIC



ABSOLUTE MAXIMUM RATINGS (Note 4)

Supply Voltage
OP-12A, OP-12B,
OP-12E, OP-12F, All DICE except GR ..... ±20V
OP-12G, GR DICE Only ..... ±18V
Operating Temperature Range
OP-12A, OP-12B ..... –55°C to +125°C
OP-12E, OP-12F, OP-12G ..... 0°C to +70°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Differential Input Current (Note 1) ..... ±10mA
Input Voltage (Note 2) ..... ±15V
Output Short-Circuit Duration ..... Indefinite
Junction Temperature (T_J) ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (NOTE 3)	Θ_{JC}	UNITS
TO-99 (J)	170	24	°C/W
8-Pin Hermetic DIP (Z)	162	26	°C/W

NOTES:
1. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is provided.
2. For supply voltages less than –15V, the absolute maximum input voltage is equal to the supply voltage.
3. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for TO and CerDIP packages.
4. Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 20V$ and $T_A = 25°C$ for A, B, E and F grades, $V_S = \pm 15V$, and $T_A = 25°C$ for C and G grades, unless otherwise noted.

			OP-12A/E			OP-12B/F			OP-12G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.07	0.15	—	0.18	0.30	—	0.25	1.0	mV
Input Offset Current	I_{OS}		—	0.05	0.20	—	0.05	0.20	—	0.08	0.50	nA
Input Bias Current	I_B		—	0.8	2.0	—	0.8	2.0	—	1.0	5.0	nA
Input Resistance — Differential-Mode	R_{IN}	(Note 1)	26	70	—	26	70	—	10	50	—	MΩ
Input Voltage Range	IVR	$V_S = \pm 15V$	±13	±14	—	±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	104	120	—	104	120	—	84	116	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	—	1	7	—	1	7	—	4	63	μV/V
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$, $V_S = \pm 15V$ $R_L \geq 2k\Omega$, $V_S = \pm 15V$	±13 ±10	±14 ±12	— —	±13 ±10	±14 ±12	— —	±13 ±10	±14 ±12	— —	V
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$ $V_O = \pm 10V$ $R_L \geq 2k\Omega$ $V_O = \pm 10V$	80 50	300 150	— —	80 50	300 150	— —	40 —	250 100	— —	V/mV
Power Consumption	P_d	$V_S = \pm 15V$, No Load $V_S = \pm 5V$, No Load	— —	9 3	18 6	— —	9 3	18 6	— —	12 4	24 8	mW
Input Noise Voltage	e_{np-p}	0.1Hz to 10Hz	—	0.9	—	—	0.9	—	—	0.9	—	μV_{p-p}
Input Noise Voltage Density	e_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	— — —	22 21 20	— — —	— — —	22 21 20	— — —	— — —	22 21 20	— — —	$nV/\sqrt{Hz}$
Input Noise Current	i_{np-p}	0.1Hz to 10Hz	—	3	—	—	3	—	—	3	—	pA_{p-p}
Input Noise Current Density	i_n	$f_O = 10Hz$ $f_O = 100Hz$ $f_O = 1000Hz$	— — —	0.15 0.14 0.13	— — —	— — —	0.15 0.14 0.13	— — —	— — —	0.15 0.14 0.13	— — —	$pA/\sqrt{Hz}$
Slew Rate	SR	$R_L \geq 2k\Omega$	—	0.12	—	—	0.12	—	—	0.12	—	V/μs
Closed-Loop Bandwidth	BW	$A_{VCL} = +1$	—	0.80	—	—	0.80	—	—	0.80	—	MHz
Open-Loop Output Resistance	R_O	$V_O = 0$, $I_O = 0$	—	200	—	—	200	—	—	200	—	Ω

NOTE:
1. Guaranteed by input bias current.

ELECTRICAL CHARACTERISTICS at V_S = ±20V for A and B grades, –55°C ≤ T_A ≤ +125°C, unless otherwise noted.

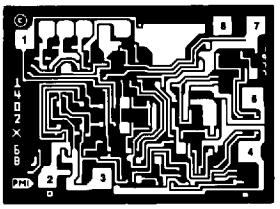
			OP-12A			OP-12B			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		–	0.12	0.35	–	0.28	0.60	mV
Average Input Offset Voltage Drift	TCV_{OS}		–	0.50	2.5	–	1.0	3.5	µV/°C
Input Offset Current	I_{OS}		–	0.12	0.40	–	0.12	0.40	nA
Average Input Offset Current Drift	TCI_{OS}		–	0.50	2.5	–	0.50	2.5	pA/°C
Input Bias Current	I_B		–	1.2	3.0	–	1.2	3.0	nA
Input Voltage Range	IVR	V_S = ±15V	±13	± 14	–	±13	±14	–	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	100	116	–	100	116	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±15V	–	4	10	–	4	10	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 5kΩ V_O = ±10V	40	120	–	40	120	–	V/mV
Output Voltage Swing	V_O	R_L ≥ 10kΩ, V_S = ±15V R_L ≥ 5kΩ, V_S = ±15V	±13 ±10	±14 ±13	– –	±13 ±10	±14 ±13	– –	V
Power Consumption	P_d	V_S = ±15V, No Load	–	9	18	–	9	18	mW

ELECTRICAL CHARACTERISTICS at V_S = ±15V for G grade, V_S = ±20V for E and F grades, 0°C ≤ T_A ≤ 70°C, unless otherwise noted.

			OP-12E			OP-12F			OP-12G			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}		—	0.10	0.26	—	0.23	0.45	—	0.32	1.4	mV
Average Input Offset Voltage Drift	TCV_{OS}		—	0.50	2.5	—	1.0	3.5	—	1.5	10	µV/°C
Input Offset Current	I_{OS}		—	0.08	0.30	—	0.11	0.60	—	0.12	0.70	nA
Average Input Offset Current Drift	TCI_{OS}		—	0.50	2.5	—	1.0	5.0	—	1.0	5.0	pA/°C
Input Bias Current	I_B		—	1.0	2.6	—	1.2	5.2	—	1.4	6.5	nA
Input Voltage Range	IVR	V_S = ±15V	±13	±14	—	±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	100	116	—	100	116	—	80	112	—	dB
Power Supply Rejection Ratio	PSRR	V_S = ±5 to ±15V	—	4	10	—	4	10	—	6	100	µV/V
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 10kΩ V_O = ±10V R_L ≥ 2kΩ V_O = ±10V	60 25	200 100	— —	60 25	200 100	— —	25 —	150 80	— —	V/mV
Output Voltage Swing	V_O	R_L ≥ 10kΩ V_S = ±15V R_L ≥ 5kΩ V_S = ±15V	±13 ±10	±14 ±12	— —	±13 ±10	±14 ±12	— —	±13 ±10	±14 ±12	— —	V
Power Consumption	P_d	V_S = ±15V, No Load	—	9	18	—	9	18	—	15	24	mW

For typical performance characteristics, see OP-08 data sheet. Assume C_C = 30pF.

DICE CHARACTERISTICS (125°C TESTED DICE AVAILABLE)



DIE SIZE 0.059 × 0.043 inch, 2537 sq. mils
(1.50 × 1.09 mm, 1.64 sq. mm)

1. NO CONNECTION
2. INVERTING INPUT
3. NONINVERTING INPUT
4. V–
6. OUTPUT
7. V +
8. NO CONNECTION

WAFER TEST LIMITS at $V_S = \pm 15V$, $T_A = 25°C$ for OP-12N, OP-12G and OP-12GR devices; $T_A = 125°C$ for OP-12NT and OP-12GT devices, unless otherwise noted. (Note 2)

PARAMETER	SYMBOL	CONDITIONS	OP-12NT LIMIT	OP-12N LIMIT	OP-12GT LIMIT	OP-12G LIMIT	OP-12GR LIMIT	UNITS
Input Offset Voltage	V_{OS}		0.35	0.15	0.6	0.3	1	mV MAX
Input Offset Current	I_{OS}		0.4	0.2	0.4	0.2	0.5	nA MAX
Input Bias Current	I_B		3	2	3	2	5	nA MAX
Input Voltage Range	IVR		±13	±13	±13	±13	±13	V MIN
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	100	104	100	104	84	dB MIN
Power Supply Rejection Ratio	PSRR	$V_S = \pm 5V$ to $\pm 15V$	10	7	10	7	63	µV/V MAX
Output Voltage Swing	V_O	$R_L \geq 10k\Omega$	±13	±13	±13	±13	±13	V MIN
		$R_L \geq 2k\Omega$	—	±10	—	±10	±10	
		$R_L \geq 5k\Omega$	±10	—	±10	—	—	
Large-Signal Voltage Gain	A_{VO}	$R_L \geq 10k\Omega$, $V_O = \pm 10V$	80	80	80	80	40	V/mV MIN
		$R_L \geq 2k\Omega$, $V_O = \pm 10V$	—	50	—	50	—	
		$R_L \geq 5k\Omega$, $V_O = \pm 10V$	40	—	40	—	—	
Input Resistance	R_{IN}	(Note 1)	26	26	26	26	10	MΩ MIN
Supply Current	I_{SY}	$I_{OUT} = 0$ $V_{OUT} = 0$	0.6	0.6	0.6	0.6	0.8	mA MAX

NOTES:
1. Guaranteed by design.
2. For 25°C specifications of OP-12NT and OP-12GT, see OP-12N and OP-12G, respectively.

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-12NT TYPICAL	OP-12N TYPICAL	OP-12GT TYPICAL	OP-12G TYPICAL	OP-12GR TYPICAL	UNITS
Average Input Offset Voltage Drift	TCV_{OS}		0.5	0.5	1.0	1.0	1.5	µV/°C
Average Input Offset Current Drift	TCI_{OS}		0.5	0.5	1.0	1.0	1.0	pA/°C