MICRON TECHNOLOGY, INC.

512K x 16, 1 MEG x 8 BOOT BLOCK FLASH MEMORY

FLASH MEMORY

MT28F800B1

SMARTVOLTAGE

FEATURES

- Eleven erase blocks:
  - 16KB / 8K-word boot block (protected)
  - Two 8KB / 4K-word parameter blocks
  - Eight main memory blocks
- SmartVoltage Technology (SVT):
  - 3.3V ±0.3V or 5V ±10% V_{CC}
  - 5V ±10% or 12V ±5% V_{PP}
- Address access times:
  - 80ns at 5V V_{CC}
  - 110ns at 3.3V V_{CC}
- Selectable organizations:
  - 524,288 x 16 or
  - 1,048,576 x 8
- Industry-standard pinouts
- Inputs and outputs are fully TTL-compatible
- Automated write and erase algorithm
- Two-cycle WRITE / ERASE sequence
- Byte- or word-wide READ and WRITE
- TSOP and SOP packaging options

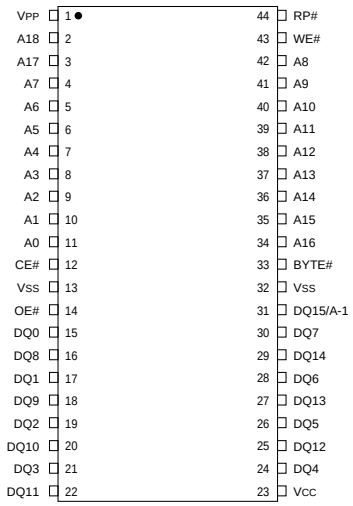
OPTIONS / MARKING

- Timing (5V V_{CC} / 3.3V V_{CC})
  - 80ns / 110ns access: -8
- Boot Block Starting Address
  - Top (7FFFFH): T
  - Bottom (00000H): B
- Packages
  - Plastic SOP (600 mil): SG
  - Plastic 48-pin TSOP Type 1 (12mm x 20mm): WG
- Part Number Example: MT28F800B1SG-8 T

PIN ASSIGNMENT (Top View)

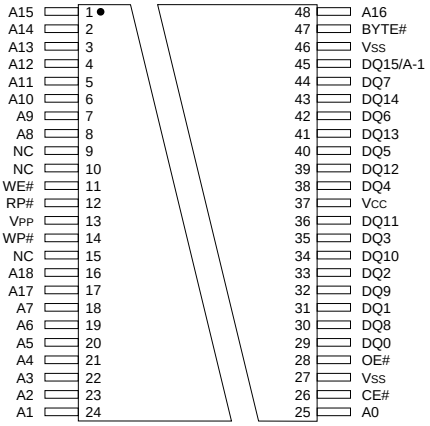
44-Pin SOP

(B-1)



48-Pin TSOP Type I

(C-3)



GENERAL DESCRIPTION

The MT28F800B1 is a nonvolatile, electrically block-erasable (flash), programmable read-only memory containing 8,388,608 bits organized as 524,288 words by 16 bits or 1,048,576 words by 8 bits. SmartVoltage Technology (SVT) provides industry-standard, multi- or single-voltage, dual-supply operation. Writing or erasing the device is done with either a 5V or 12V V_{PP} voltage, while all operations are performed with a 3.3V or 5V V_{CC}. It is fabricated with Micron's advanced CMOS floating-gate process.

The MT28F800B1 is organized into eleven separately erasable blocks. To ensure that critical firmware is protected from accidental erasure or overwrite, the MT28F800B1 features a hardware-protected boot block. Writing or erasing the boot block requires either applying a super-voltage to the RP# pin or driving WP# HIGH in addition to executing the normal WRITE or ERASE sequences. This block may be used to store code implemented in low-level system

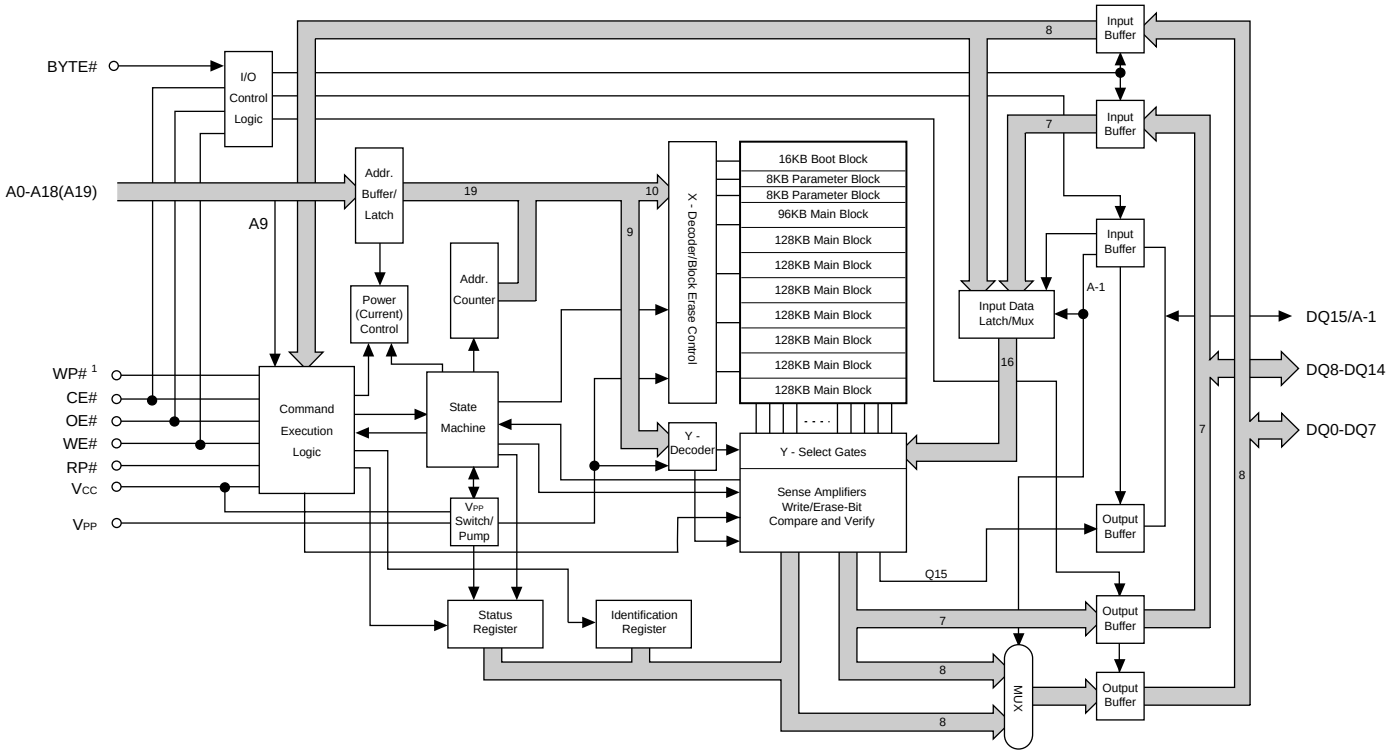
GENERAL DESCRIPTION (continued)

recovery. The remaining blocks vary in density and are written and erased with no additional security measures.

The byte or word address is issued to read the memory array with CE# and OE# LOW and WE# HIGH. Valid data is output until the next address is issued. The BYTE# pin is used to switch the data path between 8 bits wide and 16 bits wide. When BYTE# is LOW, the dual-use pin DQ15/A-1 becomes the lowest order address bit (A-1). When BYTE# is HIGH, the DQ15/A-1 pin becomes the most significant data bit (DQ15).

Please refer to Micron's Web site (www.micron.com/flash/htmls/datasheets.html) for the latest full-length data sheet.

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. On MT28F800B1 WG only.

PIN DESCRIPTIONS

SOP PIN NUMBERS	TSOP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
43	11	WE#	Input	Write Enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is either a WRITE to the command execution logic (CEL) or to the memory array.
–	14	WP#	Input	Write Protect: Unlocks the boot block when HIGH if $V_{PP} = V_{PPH1}$ (5V) or V_{PPH2} (12V) and RP# = V_{IH} during a WRITE or ERASE. Does not affect WRITE or ERASE operation on other blocks.
12	26	CE#	Input	Chip Enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby power mode.
44	12	RP#	Input	Reset/Power-Down: When LOW, RP# clears the status register, sets the internal state machine (ISM) to the array read mode and places the device in deep power-down mode. All inputs, including CE#, are “Don’t Care,” and all outputs are High-Z. RP# unlocks the boot block and overrides the condition of WP# when at V_{HH} (12V), and must be held at V_{IH} during all other modes of operation.
14	28	OE#	Input	Output Enable: Enables data output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
33	47	BYTE#	Input	Byte Enable: If BYTE# = HIGH, the upper byte is active through DQ8-DQ15. If BYTE# = LOW, DQ8-DQ14 are High-Z, and all data is accessed through DQ0-DQ7. DQ15/A-1 becomes the least significant address input.
11, 10, 9, 8, 7, 6, 5, 4, 42, 41, 40, 39, 38, 37, 36, 35, 34, 3, 2	25, 24, 23, 22, 21, 20, 19, 18, 8, 7, 6, 5, 4, 3, 2, 1, 48, 17, 16	A0-A18	Input	Address Inputs: Select a unique 16-bit word out of the 524,288 available. The DQ15/A-1 input becomes the lowest order address when BYTE# = LOW to allow for a selection of an 8-bit byte from the 1,048,576 available.
31	45	DQ15/ A-1	Input/ Output	Data I/O: MSB of data when BYTE# = HIGH. Address Input: LSB of address input when BYTE# = LOW during READ or WRITE operation.
15, 17, 19, 21, 24, 26, 28, 30	29, 31, 33, 35, 38, 40, 42, 44	DQ0-DQ7	Input/ Output	Data I/Os: Data output pins during any READ operation or data input pins during a WRITE. These pins are used to input commands to the CEL.
16, 18, 20, 22, 25, 27, 29	30, 32, 34, 36, 39, 41, 43	DQ8-DQ14	Input/ Output	Data I/Os: Data output pins during any READ operation or data input pins during a WRITE when BYTE# = HIGH. These pins are High-Z when BYTE# is LOW.
–	9, 10, 15	NC	–	No Connect: These pins may be driven or left unconnected.
1	13	V_{PP}	Supply	Write/Erase Supply Voltage: From a WRITE or ERASE CONFIRM until completion of the WRITE or ERASE, V_{PP} must be at V_{PPH1} (5V) or V_{PPH2} (12V). V_{PP} = “Don’t Care” during all other operations.
23	37	V_{CC}	Supply	Power Supply: +5V ±10% or +3.3V ±0.3V.
13, 32	27, 46	V_{SS}	Supply	Ground.

TRUTH TABLE[1]

FUNCTION	RP#	CE#	OE#	WE#	WP#	BYTE#	A0	A9	V_{PP}	DQ0-DQ7	DQ8-DQ14	DQ15/A-1
Standby	H	H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
RESET	L	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
READ												
READ (word mode)	H	L	L	H	X	H	X	X	X	Data-Out	Data-Out	Data-Out
READ (byte mode)	H	L	L	H	X	L	X	X	X	Data-Out	High-Z	A-1
Output Disable	H	L	H	H	X	X	X	X	X	High-Z	High-Z	High-Z
WRITE/ERASE (EXCEPT BOOT BLOCK)[2]												
ERASE SETUP	H	L	H	L	X	X	X	X	X	20H	X	X
ERASE CONFIRM[3]	H	L	H	L	X	X	X	X	V_{PPH}	D0H	X	X
WRITE SETUP	H	L	H	L	X	X	X	X	X	10H/40H	X	X
WRITE (word mode)[4]	H	L	H	L	X	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
WRITE (byte mode)[4]	H	L	H	L	X	L	X	X	V_{PPH}	Data-In	X	A-1
READ ARRAY[5]	H	L	H	L	X	X	X	X	X	FFH	X	X
WRITE/ERASE (BOOT BLOCK)[2, 7]												
ERASE SETUP	H	L	H	L	X	X	X	X	X	20H	X	X
ERASE CONFIRM[3]	V_{HH}	L	H	L	X	X	X	X	V_{PPH}	D0H	X	X
ERASE CONFIRM[3, 6]	H	L	H	L	H	X	X	X	V_{PPH}	D0H	X	X
WRITE SETUP	H	L	H	L	X	X	X	X	X	10H/40H	X	X
WRITE (word mode)[4]	V_{HH}	L	H	L	X	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
WRITE (word mode)[4, 6]	H	L	H	L	H	H	X	X	V_{PPH}	Data-In	Data-In	Data-In
WRITE (byte mode)[4]	V_{HH}	L	H	L	X	L	X	X	V_{PPH}	Data-In	X	A-1
WRITE (byte mode)[4, 6]	H	L	H	L	H	L	X	X	V_{PPH}	Data-In	X	A-1
READ ARRAY[5]	H	L	H	L	X	X	X	X	X	FFH	X	X
DEVICE IDENTIFICATION[8, 9]												
Manufacturer Compatibility (word mode)[10]	H	L	L	H	X	H	L	V_{ID}	X	89H	00H	–
Manufacturer Compatibility (byte mode)	H	L	L	H	X	L	L	V_{ID}	X	89H	High-Z	X
Device (word mode, top boot)[10]	H	L	L	H	X	H	H	V_{ID}	X	9CH	88H	–
Device (byte mode, top boot)	H	L	L	H	X	L	H	V_{ID}	X	9CH	High-Z	X
Device (word mode, bottom boot)[10]	H	L	L	H	X	H	H	V_{ID}	X	9DH	88H	–
Device (byte mode, bottom boot)	H	L	L	H	X	L	H	V_{ID}	X	9DH	High-Z	X

NOTE:

1. L = V_{IL} (LOW), H = V_{IH} (HIGH), X = V_{IL} or V_{IH} ("Don't Care").
2. $V_{PPH} = V_{PPH1}$ = 5V or V_{PPH2} = 12V.
3. Operation must be preceded by ERASE SETUP command.
4. Operation must be preceded by WRITE SETUP command.
5. The READ ARRAY command must be issued before reading the array after writing or erasing.
6. When WP# = V_{IH}, RP# may be at V_{IH} or V_{HH}.
7. V_{HH} = 12V.
8. V_{ID} = 12V; may also be read by issuing the IDENTIFY DEVICE command.
9. A1-A8, A10-A18 = V_{IL}.
10. Value reflects DQ8-DQ15.

FUNCTIONAL DESCRIPTION

The MT28F800B1 flash memory incorporates a number of features to make it ideally suited for system firmware. The memory array is segmented into individual erase blocks. Each block may be erased without affecting data stored in other blocks. These memory blocks are read, written and erased with commands to the command execution logic (CEL). The CEL controls the operation of the internal state machine (ISM), which completely controls all WRITE, BLOCK ERASE and VERIFY operations. The ISM protects each memory location from over-erasure and optimizes each memory location for maximum data retention. In addition, the ISM greatly simplifies the control necessary for writing the device in-system or in an external programmer.

The Functional Description provides detailed information on the operation of the MT28F800B1 and is organized into these sections:

- Overview
- Memory Architecture
- Output (READ) Operations
- Input Operations
- Command Set
- ISM Status Register
- Command Execution
- Error Handling
- WRITE/ERASE Cycle Endurance
- Power Usage
- Power-Up

OVERVIEW

SMARTVOLTAGE TECHNOLOGY (SVT)

SmartVoltage Technology allows maximum flexibility for in-system READ, WRITE and ERASE operations. For 5V-only systems, WRITE and ERASE operations may be executed with a V_{PP} voltage of 5V. If 12V is available in a system, the highest ERASE and WRITE performance can be achieved with a V_{PP} voltage of 12V. For any operation, V_{CC} may be at 3.3V or 5V.

ELEVEN INDEPENDENTLY ERASABLE MEMORY BLOCKS

The MT28F800B1 is organized into eleven independently erasable memory blocks that allow portions of the memory to be erased without affecting the rest of the memory data. A special boot block is hardware-protected against inadvertent erasure or writing by requiring either a super-voltage on the RP# pin or driving the WP# pin HIGH. (The WP# pin does not apply to the SOP package.) One of these two conditions must exist along with the V_{PP} voltage (5V or 12V) on the V_{PP} pin before a WRITE or ERASE will be performed on the boot block. The remaining blocks require only the V_{PP} voltage be present on the V_{PP} pin before writing or erasing.

HARDWARE-PROTECTED BOOT BLOCK

This block of the memory array can be erased or written only when the RP# pin is taken to V_{HH} or when the WP# pin is brought HIGH. (The WP# pin does not apply to the SOP package.) This provides additional security for the core firmware during in-system firmware updates should an unintentional power fluctuation or system reset occur. The MT28F800B1 is available in two versions: the MT28F800B1T addresses the boot block starting from 7FFFFH, and the MT28F800B1B addresses the boot block starting from 00000H.

SELECTABLE BUS SIZE

The MT28F800B1 allows selection of an 8-bit (1 Meg x 8) or 16-bit (512K x 16) data bus for reading and writing the memory. The BYTE# pin is used to select the bus width. In the x16 configuration, control data is read or written only on the lower 8 bits (DQ0-DQ7).

Data written to the memory array utilizes all active data pins for the selected configuration. When the x8 configuration is selected, data is written in byte form; when the x16 configuration is selected, data is written in word form.

INTERNAL STATE MACHINE (ISM)

BLOCK ERASE and BYTE/WORD WRITE timing are simplified with an ISM that controls all erase and write algorithms in the memory array. The ISM ensures protection against over-erasure and optimizes write margin to each cell.

During WRITE operations, the ISM automatically increments and monitors WRITE attempts, verifies write margin on each memory cell and updates the ISM status register. When BLOCK ERASE is performed, the ISM automatically overwrites the entire addressed block (eliminates over-erasure), increments and monitors ERASE attempts, and sets bits in the ISM status register.

ISM STATUS REGISTER

The ISM status register allows an external processor to monitor the status of the ISM during WRITE and ERASE operations. Two bits of the 8-bit status register are set and cleared entirely by the ISM. These bits indicate whether the ISM is busy with an ERASE or WRITE task and when an ERASE has been suspended. Additional error information is set in three other bits: V_{PP} status, write status and erase status.

COMMAND EXECUTION LOGIC (CEL)

The CEL receives and interprets commands to the device. These commands control the operation of the ISM and the READ path (i.e., memory array, ID register or status register). Commands may be issued to the CEL while the ISM is active. However, there are restrictions on what commands are allowed in this condition. See the Command Execution section for more detail.

DEEP POWER-DOWN MODE

To allow for maximum power conservation, the MT28F800B1 features a very low current, deep power-down mode. To enter this mode, the RP# pin is taken to V_{SS} ±0.2V. In this mode, the current draw is a maximum of 20µA at 5V V_{CC} and 8µA at 3.3V V_{CC}. Entering deep power-down also clears the status register and sets the ISM to the read array mode.

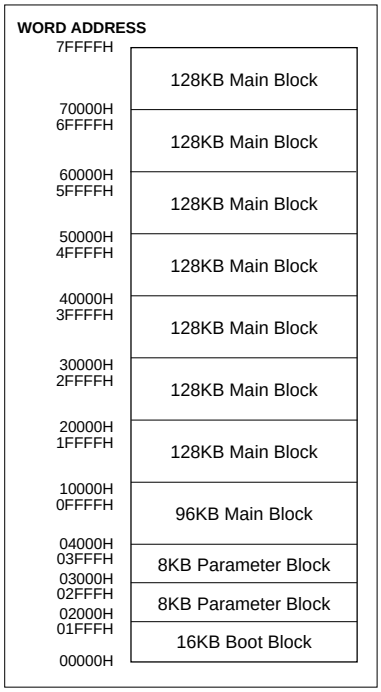
MEMORY ARCHITECTURE

The MT28F800B1 memory array architecture is designed to allow sections to be erased without disturbing the rest of the array. The array is divided into eleven addressable blocks that vary in size and are independently erasable. When blocks rather than the entire array are erased, total device endurance is enhanced, as is system flexibility. Only the ERASE function is block-oriented. All READ and WRITE operations are done on a random-access basis.

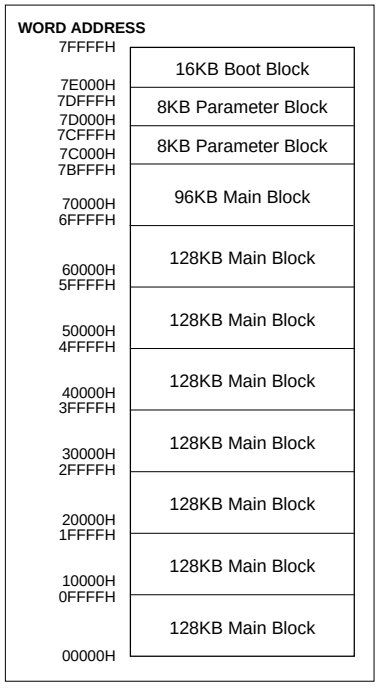
The boot block is protected from unintentional ERASE or WRITE with a hardware protection circuit that requires a super-voltage be applied to RP# or that the WP# pin be driven HIGH before erasure is commenced. The boot block is intended for the core firmware required for basic system functionality. The remaining ten blocks do not require either of these two conditions be met before WRITE or ERASE operations.

BOOT BLOCK

The hardware-protected boot block provides extra security for the most sensitive portions of the firmware. This 16KB block may only be erased or written when the RP# pin is at the specified boot block unlock voltage (V_{HH}) of 12V or when the WP# pin is HIGH. During a WRITE or ERASE of the boot block, the RP# pin must be held at V_{HH} or the WP# pin held HIGH until the WRITE or ERASE is completed. (The WP# pin does not apply to the SOP package.) The V_{PP} pin must be at V_{PPH} (5V or 12V) when the boot block is written to or erased.



Bottom Boot - MT28F800B1xx-xxB



Top Boot - MT28F800B1xx-xxT

Figure 1
MEMORY ADDRESS MAPS

The MT28F800B1 is available in two configurations, top or bottom boot block. The MT28F800B1T top boot block version supports processors of the x86 variety. The MT28F800B1B bottom boot block version is intended for 680X0 and RISC applications. Figure 1 illustrates the memory address maps associated with these two versions.

PARAMETER BLOCKS

The two 8KB parameter blocks store less sensitive and more frequently changing system parameters and also may store configuration or diagnostic coding. These blocks are enabled for erasure when the V_{PP} pin is at V_{PPH}. No super-voltage unlock or WP# control is required.

MAIN MEMORY BLOCKS

The eight remaining blocks are general-purpose memory blocks and do not require a super-voltage on RP# or WP# control to be erased or written. These blocks are intended for code storage, ROM-resident applications or operating systems that require in-system update capability.

OUTPUT (READ) OPERATIONS

The MT28F800B1 features three different types of READs. Depending on the current mode of the device, a READ operation will produce data from the memory array, status register or device identification register. In each of these three cases, the WE#, CE# and OE# inputs are controlled in a similar manner. Moving between modes to perform a specific READ will be covered in the Command Execution section.

MEMORY ARRAY

To read the memory array, WE# must be HIGH, and OE# and CE# must be LOW. Valid data will be output on the DQ pins once these conditions have been met and a valid address is given. Valid data will remain on the DQ pins until the address changes, or OE# or CE# goes HIGH, whichever occurs first. The DQ pins will continue to output new data after each address transition as long as OE# and CE# remain LOW.

The MT28F800B1 features selectable bus widths. When the memory array is accessed as a 512K x 16, BYTE# is HIGH, and data will be output on DQ0-DQ15. To access the memory array as a 1 Meg x 8, BYTE# must be LOW, DQ8-DQ14 are High-Z, and all data is output on DQ0-DQ7. The DQ15/A-1 pin now becomes the lowest order address input so that 1,048,576 locations can be read.

After power-up or RESET, the device will automatically be in the array read mode. All commands and their operations are covered in the Command Set and Command Execution sections.

STATUS REGISTER

Performing a READ of the status register requires the same input sequencing as a READ of the array except that the address inputs are "Don't Care." The status register contents are always output on DQ0-DQ7, regardless of the condition of BYTE#. DQ8-DQ15 are LOW when BYTE# is HIGH, and DQ8-DQ14 are High-Z when BYTE# is LOW. Data from the status register is latched on the falling edge of OE# or CE#, whichever occurs last. If the contents of the status register change during a READ of the status register, either OE# or CE# may be toggled while the other is held LOW to update the output.

Following a WRITE or ERASE, the device automatically enters the status register read mode. In addition, a READ during a WRITE or ERASE will produce the status register contents on DQ0-DQ7. When the device is in the erase suspend mode, a READ operation will produce the status register contents until another command is issued, while in certain other modes, READ STATUS REGISTER may be given to return to the status register read mode. All commands and their operations are covered in the Command Set and Command Execution sections.

IDENTIFICATION REGISTER

A READ of the two 8-bit device identification registers requires the same input sequencing as a READ of the array. WE# must be HIGH, and OE# and CE# must be LOW. However, ID register data is output only on DQ0-DQ7, regardless of the condition of BYTE#. A0 is used to decode between the two bytes of the device ID register; all other address inputs are "Don't Care." When A0 is LOW, the manufacturer compatibility ID is output, and when A0 is HIGH, the device ID is output. DQ8-DQ15 are High-Z when BYTE# is LOW. When BYTE# is HIGH, DQ8-DQ15 are 00H when the manufacturer compatibility ID is read and 88H when the device ID is read.

To get to the identification register read mode, READ IDENTIFICATION may be issued while the device is in certain other modes. In addition, the identification register read mode can be reached by applying a super-voltage (V_{ID}) to the A9 pin. Using this method, the ID register can be read while the device is in any mode. Once A9 is returned to V_{IL} or V_{IH}, the device will return to the previous mode.

INPUT OPERATIONS

The DQ pins are used either to input data to the array or to input a command to the CEL. A command input issues an 8-bit command to the CEL to control the mode of operation of the device. A WRITE is used to input data to the memory array. The following section describes both types of inputs. More information describing how to use the two types of

inputs to write or erase the device is provided in the Command Execution section.

COMMANDS

To perform a command input, OE# must be HIGH, and CE# and WE# must be LOW. Addresses are "Don't Care" but must be held stable, except during an ERASE CONFIRM (described in a later section). The 8-bit command is input on DQ0-DQ7, while DQ8-DQ15 are "Don't Care." The command is latched on the rising edge of CE# (CE#-controlled) or WE# (WE#-controlled), whichever occurs first. The condition of BYTE# has no effect on a command input.

MEMORY ARRAY

A WRITE to the memory array sets the desired bits to logic 0s but cannot change a given bit to a logic 1 from a logic 0. Setting any bits to a logic 1 requires that the entire block be erased. To perform a WRITE, OE# must be HIGH, CE# and WE# must be LOW, and V_{PP} must be set to V_{PPH1} or V_{PPH2}. Writing to the boot block also requires that the RP# pin be at V_{HH} or WP# be HIGH. A0-A18 provide the address to be written, while the data to be written to the array is input on the DQ pins. The data and addresses are latched on the rising edge of CE# (CE#-controlled) or WE# (WE#-controlled), whichever occurs first. A WRITE must be preceded by a WRITE SETUP command. Details on how to input data to the array will be covered in the Write Sequence section.

Selectable bus sizing applies to WRITEs as it does to READs. When BYTE# is LOW (byte mode), data is input on DQ0-DQ7, DQ8-DQ14 are High-Z, and DQ15 becomes the lowest order address input. When BYTE# is HIGH (word mode), data is input on DQ0-DQ15.

Table 1
COMMAND SET

COMMAND	HEX CODE	DESCRIPTION
RESERVED	00H	This command and all unlisted commands are invalid and should not be called. These commands are reserved to allow for future feature enhancements.
READ ARRAY	FFH	Must be issued after any other command cycle before the array can be read. It is not necessary to issue this command after power-up or RESET.
IDENTIFY DEVICE	90H	Allows the device and manufacturer compatibility ID to be read. A0 is used to decode between the manufacturer compatibility ID (A0 = LOW) and device ID (A0 = HIGH).
READ STATUS REGISTER	70H	Allows the status register to be read. Please refer to Table 2 for more information on the status register bits.
CLEAR STATUS REGISTER	50H	Clears status register bits 3 through 5, which cannot be cleared by the ISM.
ERASE SETUP	20H	The first command given in the two-cycle ERASE sequence. The ERASE will not be completed unless followed by ERASE CONFIRM.
ERASE CONFIRM/RESUME	D0H	The second command given in the two-cycle ERASE sequence. Must follow an ERASE SETUP command to be valid. Also used during an ERASE SUSPEND to resume the ERASE.
WRITE SETUP	40H or 10H	The first command given in the two-cycle WRITE sequence. The write data and address are given in the following cycle to complete the WRITE.
ERASE SUSPEND	B0H	Requests a halt of the ERASE and puts the device into the erase suspend mode. When the device is in this mode, only READ STATUS REGISTER, READ ARRAY and ERASE RESUME commands may be executed.

COMMAND SET

To simplify writing of the memory blocks, the MT28F800B1 incorporates an ISM that controls all internal algorithms for the WRITE and ERASE cycles. An 8-bit command set is used to control the device. Details on how to sequence commands are provided in the Command Execution section. Table 1 lists the valid commands.

ISM STATUS REGISTER

The 8-bit ISM status register (see Table 2) is polled to check for WRITE or ERASE completion or any related errors. During or following a WRITE, ERASE or ERASE SUSPEND, a READ operation will output the status register contents on DQ0-DQ7 without prior command. While the status register contents are read, the outputs will not be updated if there is a change in the ISM status unless OE# or CE# is toggled. If the device is not in the write, erase, erase suspend or status register read mode, READ STATUS REGISTER (70H) can be issued to view the status register contents.

All of the defined bits are set by the ISM, but only the ISM and erase suspend status bits are reset by the ISM. The erase, write and V_{PP} status bits must be cleared using CLEAR STATUS REGISTER. If the V_{PP} status bit (SR3) is set, the CEL will not allow further WRITE or ERASE operations until the status register is cleared. This allows the user to choose when to poll and clear the status register. For example, the host system may perform multiple BYTE WRITE operations before checking the status register instead of checking after each individual WRITE. Asserting the RP# signal or powering down the device will also clear the status register.

Table 2
STATUS REGISTER

STATUS BIT #	STATUS REGISTER BIT	DESCRIPTION
SR7	ISM STATUS 1 = Ready 0 = Busy	The ISMS bit displays the active status of the state machine during WRITE or BLOCK ERASE operations. The controlling logic polls this bit to determine when the erase and write status bits are valid.
SR6	ERASE SUSPEND STATUS 1 = ERASE suspended 0 = ERASE in progress/completed	Issuing an ERASE SUSPEND places the ISM in the suspend mode and sets this and the ISMS bit to “1.” The ESS bit will remain “1” until an ERASE RESUME is issued.
SR5	ERASE STATUS 1 = BLOCK ERASE error 0 = Successful BLOCK ERASE	ES is set to “1” after the maximum number of ERASE cycles is executed by the ISM without a successful verify. ES is only cleared by a CLEAR STATUS REGISTER command or after a RESET.
SR4	WRITE STATUS 1 = WORD/BYTE WRITE error 0 = Successful WORD/BYTE WRITE	WS is set to “1” after the maximum number of WRITE cycles is executed by the ISM without a successful verify. WS is only cleared by a CLEAR STATUS REGISTER command or after a RESET.
SR3	V_{PP} STATUS 1 = No V_{PP} voltage detected 0 = V_{PP} present	V_{PP}S detects the presence of a V_{PP} voltage. It does not monitor V_{PP} continuously, nor does it indicate a valid V_{PP} voltage. The V_{PP} pin is sampled for 5V or 12V after WRITE or ERASE CONFIRM is given. V_{PP}S must be cleared by CLEAR STATUS REGISTER or by a RESET.
SR0-2	RESERVED	Reserved for future use.

COMMAND EXECUTION

Commands are issued to bring the device into different operational modes. Each mode allows specific operations to be performed. Several modes require a sequence of commands to be written before they are reached. The following section describes the properties of each mode, and Table 3 lists all command sequences required to perform the desired operation.

READ ARRAY

The array read mode is the initial state of the device upon power-up and after a RESET. If the device is in any other mode, READ ARRAY (FFH) must be given to return to the array read mode. Unlike the WRITE SETUP command (40H), READ ARRAY does not need to be given before each individual READ access.

IDENTIFY DEVICE

IDENTIFY DEVICE (90H) may be written to the CEL to enter the identify device mode. While the device is in this mode, any READ will produce the device identification when A0 is HIGH and manufacturer compatibility identification when A0 is LOW. The device will remain in this mode until another command is given.

WRITE SEQUENCE

Two consecutive cycles are needed to input data to the array. WRITE SETUP (40H or 10H) is given in the first cycle. The next cycle is the WRITE, during which the write address and data are issued and V_{PP} is brought to V_{PPH}. Writing to the boot block also requires that the RP# pin be brought to V_{HH} or the WP# pin be brought HIGH at the same time V_{PP} is brought to V_{PPH}. The ISM will now begin to write the word or byte. V_{PP} must be held at V_{PPH} until the WRITE is completed (SR7 = 1).

While the ISM executes the WRITE, the ISM status bit (SR7) will be at 0, and the device will not respond to any commands. Any READ operation will produce the status register contents on DQ0-DQ7. When the ISM status bit (SR7) is set to a logic 1, the WRITE has been completed, and the device will go into the status register read mode until another command is given.

After the ISM has initiated the WRITE, it cannot be aborted except by a RESET or by powering down the part. Doing either during a WRITE will corrupt the data being written. If only the WRITE SETUP command has been given, the WRITE may be nullified by performing a null WRITE. To execute a null WRITE, FFH must be written

Table 3
COMMAND SEQUENCES

COMMANDS	BUS CYCLES REQ'D	1ST CYCLE			2ND CYCLE			NOTES
		OPERATION	ADDRESS	DATA	OPERATION	ADDRESS	DATA	
READ ARRAY	1	WRITE	X	FFH				1
IDENTIFY DEVICE	3	WRITE	X	90H	READ	IA	ID	2, 3
READ STATUS REGISTER	2	WRITE	X	70H	READ	X	SRD	4
CLEAR STATUS REGISTER	1	WRITE	X	50H				
ERASE SETUP/CONFIRM	2	WRITE	X	20H	WRITE	BA	D0H	5, 6
ERASE SUSPEND/RESUME	2	WRITE	X	B0H	WRITE	X	D0H	
WRITE SETUP/WRITE	2	WRITE	X	40H	WRITE	WA	WD	6, 7
ALTERNATE WORD/BYTE WRITE	2	WRITE	X	10H	WRITE	WA	WD	6, 7

NOTE:
1. Must follow WRITE or ERASE CONFIRM commands to the CEL in order to enable flash array READ cycles.
2. IA = Identify Address: 00H for manufacturer compatibility ID; 01H for device ID.
3. ID = Identify Data.
4. SRD = Status Register Data.
5. BA = Block Address (A12-A18).
6. Addresses are "Don't Care" in first cycle but must be held stable.
7. WA = Address to be written; WD = Data to be written to WA.

when BYTE# is LOW, or FFFFH must be written when BYTE# is HIGH. Once the ISM status bit (SR7) has been set, the device will be in the status register read mode until another command is issued.

ERASE SEQUENCE

Executing an ERASE sequence will set all bits within a block to logic 1. The command sequence necessary to execute an ERASE is similar to that of a WRITE. To provide added security against accidental block erasure, two consecutive command cycles are required to initiate an ERASE of a block. In the first cycle, addresses are "Don't Care," and ERASE SETUP (20H) is given. In the second cycle, V_{PP} must be brought to V_{PPH}, an address within the block to be erased must be issued, and ERASE CONFIRM (D0H) must be given. If a command other than ERASE CONFIRM is given, the write and erase status bits (SR4 and SR5) will be set, and the device will be in the status register read mode.

After the ERASE CONFIRM (D0H) is issued, the ISM will start the ERASE of the addressed block. Any READ operation will output the status register contents on DQ0-DQ7. V_{PP} must be held at V_{PPH} until the ERASE is completed (SR7 = 1). Once the ERASE is completed, the device will be in the status register read mode until another command is issued. Erasing the boot block also requires that either the RP# pin be set to V_{HH} or the WP# pin be held HIGH at the same time V_{PP} is set to V_{PPH}.

ERASE SUSPENSION

The only command that may be issued while an ERASE is in progress is ERASE SUSPEND. This command allows other commands to be executed while pausing the ERASE in progress. Once the device has reached the erase suspend mode, the erase suspend status bit (SR6) and ISM status bit (SR7) will be set. The device may now be given a READ ARRAY, ERASE RESUME or READ STATUS REGISTER command. After READ ARRAY has been issued, any location not within the block being erased may be read. If ERASE RESUME is issued before SR6 has been set, the device will immediately proceed with the ERASE in progress.

ERROR HANDLING

After the ISM status bit (SR7) has been set, the V_{PP} (SR3), write (SR4) and erase (SR5) status bits may be checked. If one or a combination of these three bits has been set, an error has occurred. The ISM cannot reset these three bits. To clear these bits, CLEAR STATUS REGISTER (50H) must be given. If the V_{PP} status bit (SR3) is set, further WRITE or ERASE operations cannot resume until the status register is cleared. Table 4 lists the combination of errors.

Table 4
STATUS REGISTER ERROR DECODE[1]

STATUS BITS			
SR5	SR4	SR3	ERROR DESCRIPTION
0	0	0	No errors
0	0	1	V_{PP} voltage error
0	1	0	WRITE error
0	1	1	WRITE error, V_{PP} voltage not valid at time of WRITE
1	0	0	ERASE error
1	0	1	ERASE error, V_{PP} voltage not valid at time of ERASE CONFIRM
1	1	0	Command sequencing error or WRITE/ERASE error
1	1	1	Command sequencing error, V_{PP} voltage error, with WRITE and ERASE errors

NOTE: 1. SR3-SR5 must be cleared using CLEAR STATUS REGISTER.

WRITE/ERASE CYCLE ENDURANCE

The MT28F800B1 is designed and fabricated to meet advanced firmware storage requirements. To ensure this level of reliability, V_{PP} must be at 12V ±5% or 5V ±10% during WRITE or ERASE cycles. Operation outside these limits may reduce the number of WRITE and ERASE cycles that can be performed on the device.

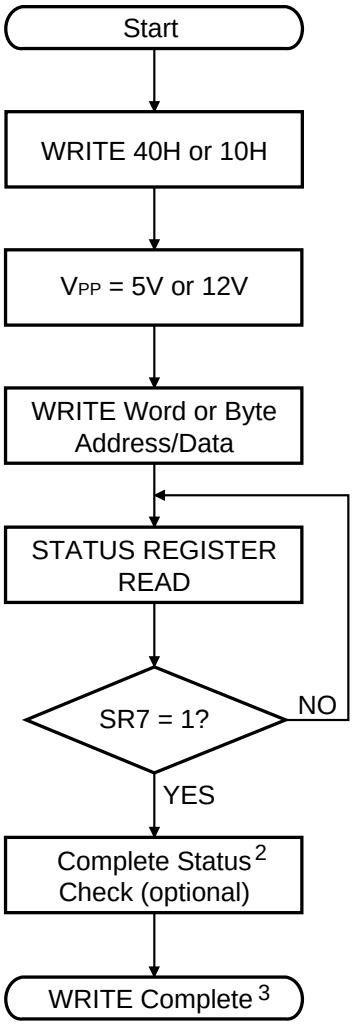
POWER USAGE

The MT28F800B1 offers several power-saving features that may be utilized in the array read mode to conserve power. Deep power-down mode is enabled by bringing RP# LOW. Current draw (I_{CC}) in this mode is a maximum of 20µA at 5V V_{CC} and 8µA at 3.3V V_{CC}. With CE# LOW, the device will enter idle current mode when it is not being accessed. In this mode, the maximum I_{CC} current is 3mA at 5V V_{CC} and 2mA at 3.3V V_{CC}. When CE# is HIGH, the device will enter standby mode. In this mode, maximum I_{CC} current is 130µA at 5V and 110µA at 3.3V. If CE# is brought HIGH during a WRITE or ERASE, the ISM will continue to operate, and the device will consume the respective active power until the WRITE or ERASE is completed.

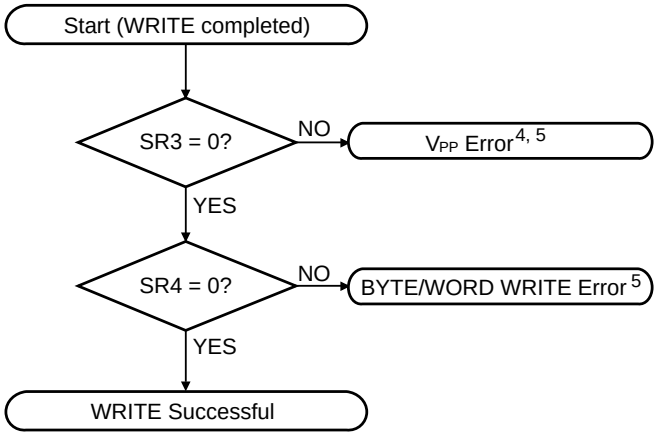
POWER-UP

During a power-up, it is not necessary to sequence V_{CC} and V_{PP}. The likelihood of unwanted WRITE or ERASE operations is minimized since two consecutive cycles are required to execute either operation. However, CE# or WE# may be held HIGH or RP# may be held LOW during power-up for additional protection while V_{CC} is ramping above V_{LKO} and V_{PP} is active. After a power-up or RESET, the status register is reset, and the device will enter the array read mode.

SELF-TIMED WRITE SEQUENCE (WORD or BYTE WRITE)[1]

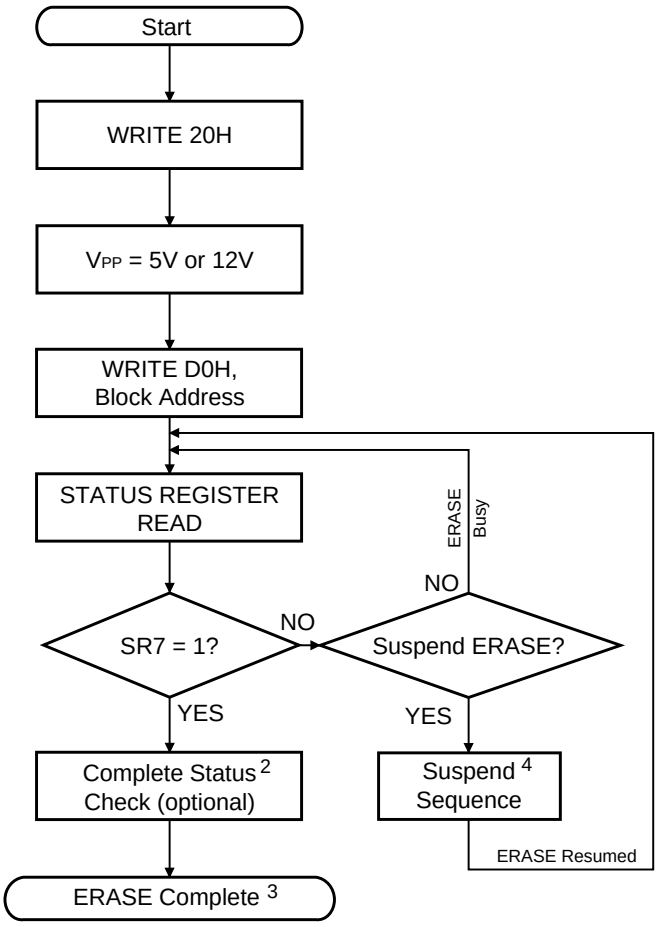


COMPLETE WRITE STATUS-CHECK SEQUENCE

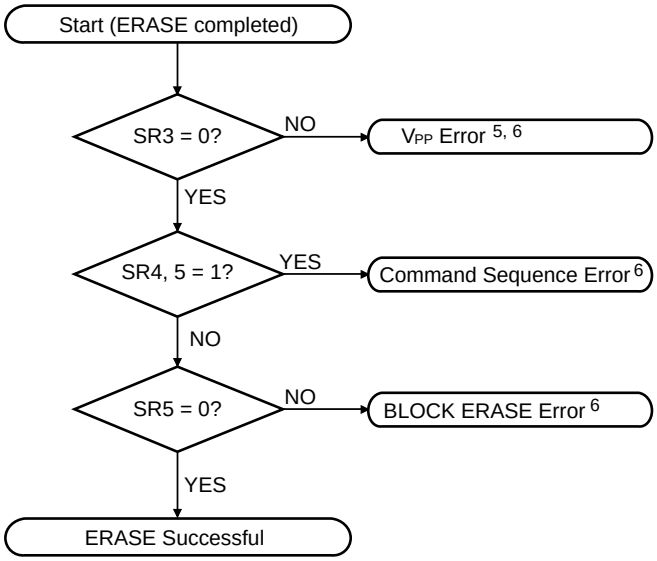


NOTE:
1. Sequence may be repeated for additional BYTE or WORD WRITEs.
2. Complete status check is not required. However, if SR3 = 1, further WRITEs are inhibited until the status register is cleared.
3. Device will be in status register read mode. To return to the array read mode, the FFH command must be issued.
4. If SR3 is set during a WRITE or BLOCK ERASE attempt, CLEAR STATUS REGISTER must be issued before further WRITE or ERASE operations are allowed by the CEL.
5. Status register bits 3-5 must be cleared using CLEAR STATUS REGISTER.

SELF-TIMED BLOCK ERASE SEQUENCE[1]

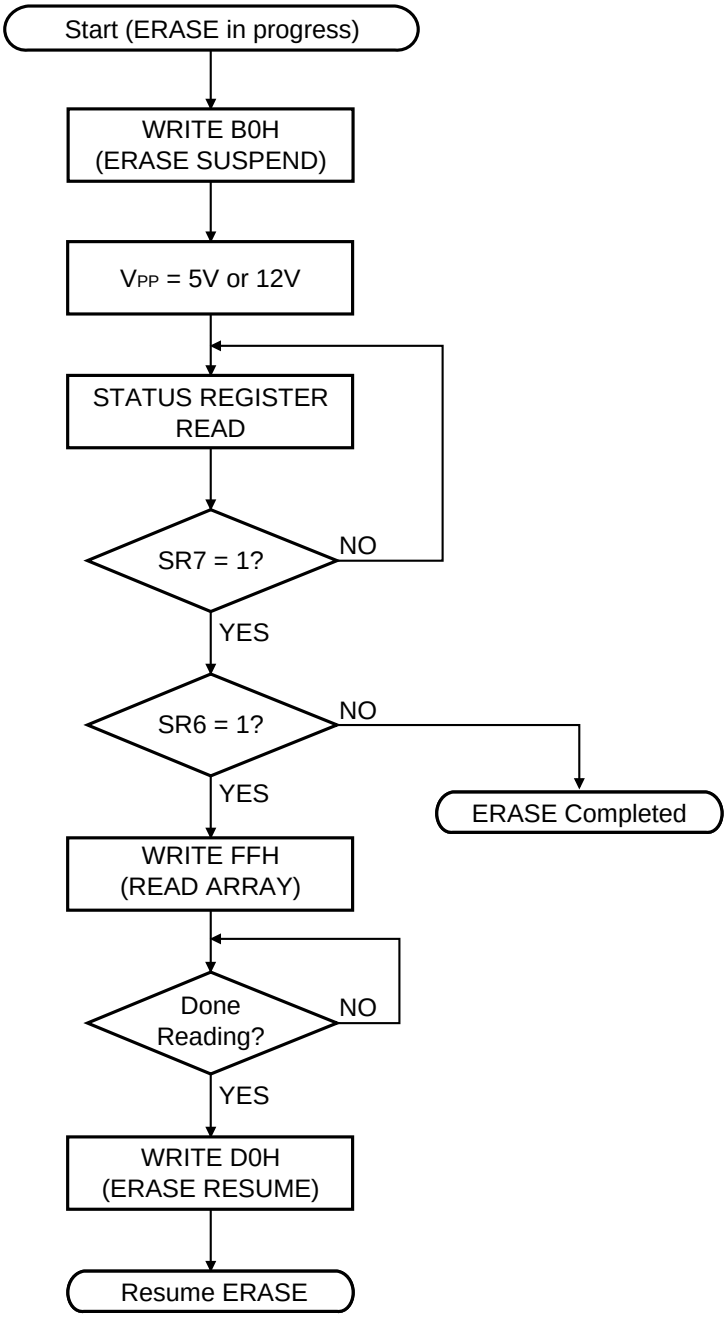


COMPLETE BLOCK ERASE STATUS-CHECK SEQUENCE



NOTE:
1. Sequence may be repeated to erase additional blocks.
2. Complete status check is not required. However, if SR3 = 1, further ERASEs are inhibited until the status register is cleared.
3. To return to the array read mode, the FFH command must be issued.
4. Refer to the ERASE SUSPEND flowchart for more information.
5. If SR3 is set during a WRITE or BLOCK ERASE attempt, CLEAR STATUS REGISTER must be issued before further WRITE or ERASE operations are allowed by the CEL.
6. Status register bits 3-5 must be cleared using CLEAR STATUS REGISTER.

ERASE SUSPEND/RESUME SEQUENCE



ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +6V**
Input Voltage Relative to V_{SS} ..... -0.5V to +6V**
V_{PP} Voltage Relative to V_{SS} ..... -0.5V to +12.6V†
RP# or A9 Pin Voltage Relative to V_{SS} .... -0.5V to +12.6V†
Temperature under Bias ..... -10°C to +80°C
Storage Temperature (plastic)..... -55°C to +125°C
Power Dissipation 1W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**V_{CC}, input and I/O pins may transition to -2V for <20ns and V_{CC} + 2V for <20ns.

†Voltage may pulse to -2V for <20ns and 14V for <20ns.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC READ OPERATING CONDITIONS

(0°C ≤ T_A ≤ +70°C)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
5V Supply Voltage	V_{CC}	4.5	5.5	V	1
3.3V Supply Voltage	V_{CC}	3	3.6	V	1
Input High (Logic 1) Voltage, all inputs	V_{IH}	2	V_{CC} + 0.5	V	1
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-0.5	0.8	V	1
Device Identification Voltage, A9	V_{ID}	11.4	12.6	V	1
V_{PP} Supply Voltage	V_{PP}	-0.5	12.6	V	1

DC OPERATING CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C)

		V_{CC} = 3.3V		V_{CC} = 5V			
PARAMETER/CONDITION	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
OUTPUT VOLTAGE LEVELS (TTL) Output High Voltage (I_{OH} = -2mA [3.3V], -2.5mA [5V]) Output Low Voltage (I_{OL} = 2mA [3.3V], 5.8mA [5V])	V_{OH1} V_{OL}	2.4 –	– 0.45	2.4 –	– 0.45	V V	1
OUTPUT VOLTAGE LEVELS (CMOS) Output High Voltage (I_{OH} = -100µA)	V_{OH2}	V_{CC} - 0.4	–	V_{CC} - 0.4	–	V	1
INPUT LEAKAGE CURRENT Any input (0V ≤ V_{IN} ≤ V_{CC}); All other pins not under test = 0V	I_L	-1	1	-1	1	µA	
INPUT LEAKAGE CURRENT: A9 INPUT (11.4V ≤ A9 ≤ 12.6 = V_{ID})	I_{ID}	–	500	–	500	µA	
INPUT LEAKAGE CURRENT: RP# INPUT (11.4V ≤ RP# ≤ 12.6 = V_{HH})	I_{HH}	–	500	–	500	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled; 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	-10	10	µA	

NOTE: 1. All voltages referenced to V_{SS}.

CAPACITANCE

(T_A = 25°C; f = 1 MHz)

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	C_I	8	pF	
Output Capacitance	C_O	12	pF	

READ AND STANDBY CURRENT DRAIN

(0°C ≤ T_A ≤ +70°C)

PARAMETER/CONDITION	SYMBOL	3.3V V_{CC} MAX	5V V_{CC} MAX	UNITS	NOTES
READ CURRENT: WORD-WIDE, TTL INPUT LEVELS ($\overline{CE}$ = V_{IL}; $\overline{OE}$ = V_{IH}; f = 10 MHz; Other inputs = V_{IL} or V_{IH}; $\overline{RP}$ = V_{IH})	I_{CC1}	30	65	mA	1, 2
READ CURRENT: WORD-WIDE, CMOS INPUT LEVELS ($\overline{CE}$ ≤ 0.2V; $\overline{OE}$ ≥ V_{CC} - 0.2V; f = 10 MHz; Other inputs ≤ 0.2V or ≥ V_{CC} - 0.2V; $\overline{RP}$ ≥ V_{CC} - 0.2V)	I_{CC2}	30	60	mA	1, 2
READ CURRENT: BYTE-WIDE, TTL INPUT LEVELS ($\overline{CE}$ = V_{IL}; $\overline{OE}$ = V_{IH}; f = 10 MHz; Other inputs = V_{IL} or V_{IH}; $\overline{RP}$ = V_{IH})	I_{CC3}	30	65	mA	1, 2
READ CURRENT: BYTE-WIDE, CMOS INPUT LEVELS ($\overline{CE}$ ≤ 0.2V; $\overline{OE}$ ≥ V_{CC} - 0.2V; f = 10 MHz; Other inputs ≤ 0.2V or ≥ V_{CC} - 0.2V; $\overline{RP}$ = V_{CC} - 0.2V)	I_{CC4}	30	60	mA	1, 2
STANDBY CURRENT: TTL INPUT LEVELS V_{CC} power supply standby current ($\overline{CE}$ = $\overline{RP}$ = V_{IH}; Other inputs = V_{IL} or V_{IH})	I_{CC5}	1.5	2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS V_{CC} power supply standby current ($\overline{CE}$ = $\overline{RP}$ = V_{CC} - 0.2V)	I_{CC6}	110	130	µA	
IDLE CURRENT: CMOS INPUT LEVELS ($\overline{CE}$ ≤ 0.2V; f = 0Hz; Other inputs ≤ 0.2V or ≥ V_{CC} - 0.2V; $\overline{RP}$ = V_{CC} - 0.2V; Array read mode)	I_{CC7}	2	3	mA	
DEEP POWER-DOWN CURRENT: V_{CC} SUPPLY ($\overline{RP}$ = V_{SS} ±0.2V)	I_{CC8}	8	20	µA	
STANDBY OR READ CURRENT: V_{PP} SUPPLY (V_{PP} > 5.5V)	I_{PP1}	50	50	µA	
STANDBY OR READ CURRENT: V_{PP} SUPPLY (V_{PP} ≤ 5.5V)	I_{PP2}	±15	±10	µA	
DEEP POWER-DOWN CURRENT: V_{PP} SUPPLY ($\overline{RP}$ = V_{SS} ±0.2V)	I_{PP3}	5	5	µA	

NOTE: 1. I_{CC} is dependent on cycle rates.
2. I_{CC} is dependent on output loading. Specified values are obtained with the outputs open.

READ TIMING PARAMETERS
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
TEST CONDITION 1 (5V)

(0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-8			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ cycle time	^tRC	80		ns	1
Access time from CE#	^tACE		80	ns	1, 2
Access time from OE#	^tAOE		40	ns	1, 2
Access time from address	^tAA		80	ns	1
RP# HIGH to output valid delay	^tRWH		500	ns	1
OE# or CE# HIGH to output in High-Z	^tOD		20	ns	1
Output hold time from OE#, CE# or address change	^tOH	0		ns	1
RP# LOW pulse width	^tRP	60		ns	1

TEST CONDITION 2 (3.3V)

(0°C ≤ T_A ≤ +70°C; V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-8			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
READ cycle time	^tRC	110		ns	3
Access time from CE#	^tACE		110	ns	2, 3
Access time from OE#	^tAOE		55	ns	2, 3
Access time from address	^tAA		110	ns	3
RP# HIGH to output valid delay	^tRWH		1,000	ns	3
OE# or CE# HIGH to output in High-Z	^tOD		30	ns	3
Output hold time from OE#, CE# or address change	^tOH	0		ns	3
RP# LOW pulse width	^tRP	150		ns	3

NOTE:
1. Measurements tested under AC Test Condition 1.
2. OE# may be delayed by ^tACE minus ^tAOE after CE# falls before ^tACE is affected.
3. Measurements tested under AC Test Condition 2.

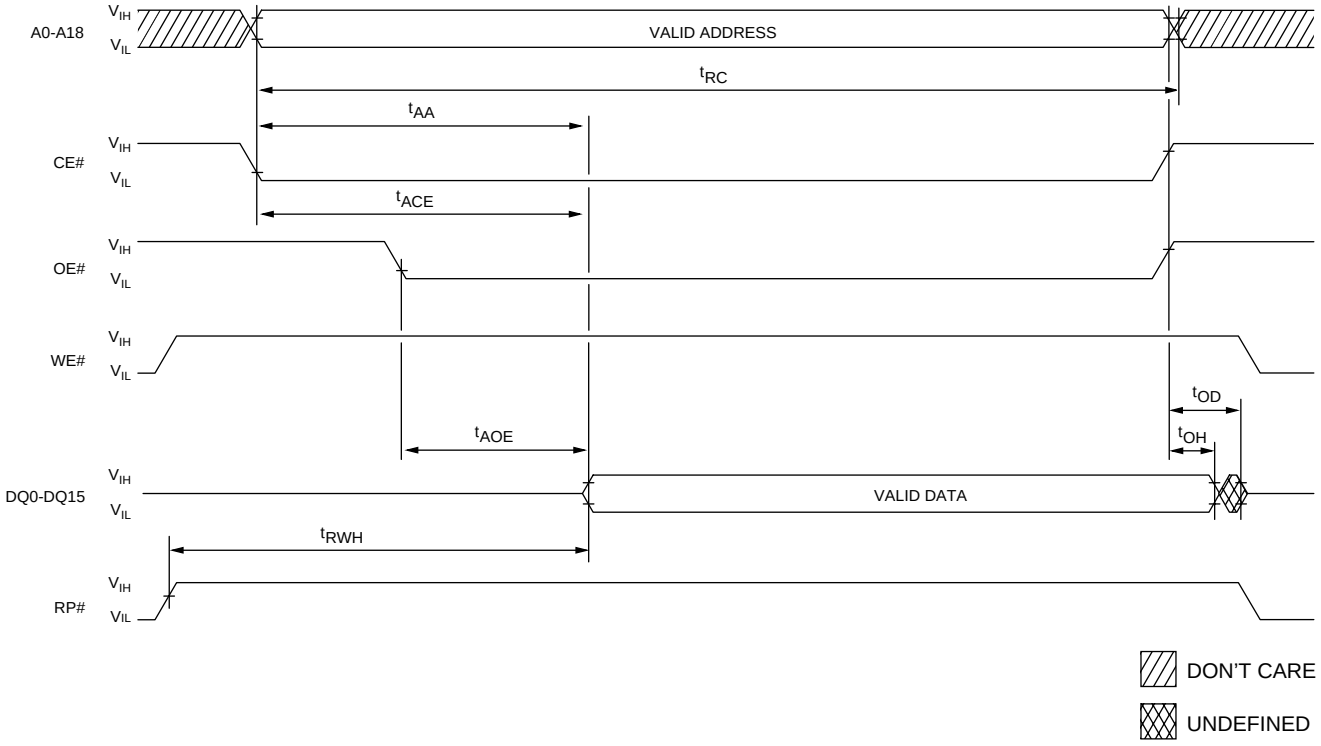
AC TEST CONDITION 1

Input pulse levels	0.4V to 2.4V
Input rise and fall times	<10ns
Input timing reference level	0.8V and 2V
Output timing reference level	0.8V and 2V
Output load	1 TTL gate and C_L = 100pF

AC TEST CONDITION 2

Input pulse levels	0V to 3V
Input rise and fall times	<10ns
Input timing reference level	1.5V
Output timing reference level	1.5V
Output load	1 TTL gate and C_L = 50pF

WORD-WIDE READ CYCLE[1]



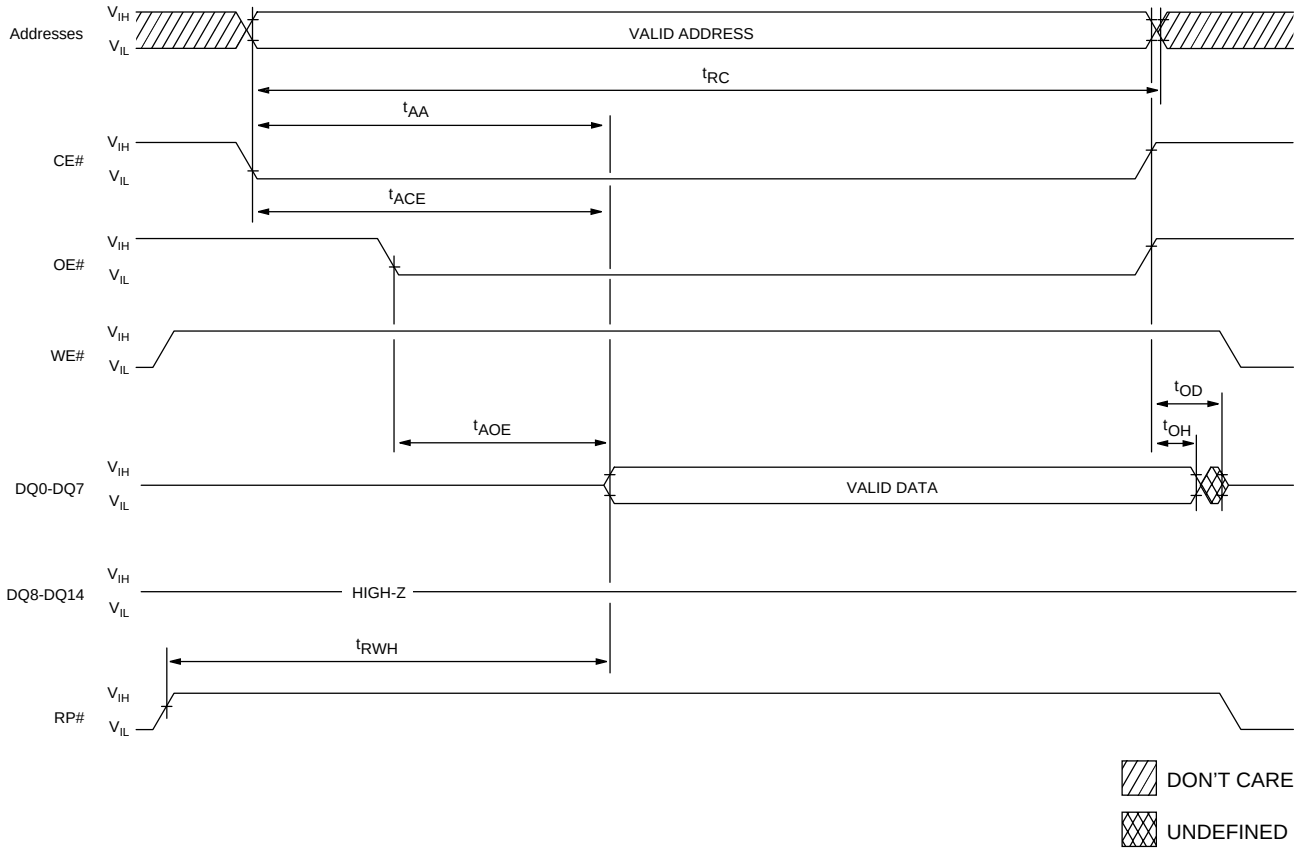
5V AND 3.3V TIMING PARAMETERS

SYMBOL	-8 MIN	-8 MAX	UNITS
^tRC (5V)[2]	80		ns
^tRC (3.3V)[3]	110		ns
^tACE (5V)[2]		80	ns
^tACE (3.3V)[3]		110	ns
^tAOE (5V)[2]		40	ns
^tAOE (3.3V)[3]		55	ns
^tAA (5V)[2]		80	ns

SYMBOL	-8 MIN	-8 MAX	UNITS
^tAA (3.3V)[3]		110	ns
^tRWH (5V)[2]		500	ns
^tRWH (3.3V)[3]		1,000	ns
^tOD (5V)[2]		20	ns
^tOD (3.3V)[3]		30	ns
^tOH (5V)[2]	0		ns
^tOH (3.3V)[3]	0		ns

NOTE: 1. BYTE# = HIGH.
2. Measurements tested under AC Test Condition 1, V_{CC} = 5V ±10%.
3. Measurements tested under AC Test Condition 2, V_{CC} = 3.3V ±0.3V.

BYTE-WIDE READ CYCLE[1]



5V AND 3.3V TIMING PARAMETERS

SYMBOL	-8 MIN	-8 MAX	UNITS
t_{RC} (5V)[2]	80		ns
t_{RC} (3.3V)[3]	110		ns
t_{ACE} (5V)[2]		80	ns
t_{ACE} (3.3V)[3]		110	ns
t_{AOE} (5V)[2]		40	ns
t_{AOE} (3.3V)[3]		55	ns
t_{AA} (5V)[2]		80	ns

SYMBOL	-8 MIN	-8 MAX	UNITS
t_{AA} (3.3V)[3]		110	ns
t_{RWH} (5V)[2]		500	ns
t_{RWH} (3.3V)[3]		1,000	ns
t_{OD} (5V)[2]		20	ns
t_{OD} (3.3V)[3]		30	ns
t_{OH} (5V)[2]	0		ns
t_{OH} (3.3V)[3]	0		ns

NOTE: 1. BYTE# = LOW.
2. Measurements tested under AC Test Condition 1, V_{CC} = 5V ±10%.
3. Measurements tested under AC Test Condition 2, V_{CC} = 3.3V ±0.3V.

RECOMMENDED DC WRITE/ERASE CONDITIONS[1]

(0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ±10% or +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
V_{PP} WRITE/ERASE lockout voltage	V_{PPLK}	–	1.5	V	2
V_{PP} voltage during WRITE/ERASE operation	V_{PPH1}	4.5	5.5	V	3
V_{PP} voltage during WRITE/ERASE operation	V_{PPH2}	11.4	12.6	V	
Boot block unlock voltage	V_{HH}	11.4	12.6	V	
V_{CC} WRITE/ERASE lockout voltage	V_{LKO}	2	–	V	

WRITE/ERASE CURRENT DRAIN (5V V_{CC})

(0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	5V V_{PP} MAX	12V V_{PP} MAX	UNITS	NOTES
WORD WRITE CURRENT: V_{CC} SUPPLY	I_{CC9}	25	45	mA	
WORD WRITE CURRENT: V_{PP} SUPPLY	I_{PP4}	50	20	mA	
BYTE WRITE CURRENT: V_{CC} SUPPLY	I_{CC10}	20	45	mA	
BYTE WRITE CURRENT: V_{PP} SUPPLY	I_{PP5}	50	15	mA	
ERASE CURRENT: V_{CC} SUPPLY	I_{CC11}	20	30	mA	
ERASE CURRENT: V_{PP} SUPPLY	I_{PP6}	50	15	mA	
ERASE SUSPEND CURRENT: V_{CC} SUPPLY (ERASE suspended)	I_{CC12}	10	10	mA	4
ERASE SUSPEND CURRENT: V_{PP} SUPPLY (ERASE suspended)	I_{PP7}	200	200	µA	

WRITE/ERASE CURRENT DRAIN (3.3V V_{CC})

(0°C ≤ T_A ≤ +70°C; V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	5V V_{PP} MAX	12V V_{PP} MAX	UNITS	NOTES
WORD WRITE CURRENT: V_{CC} SUPPLY	I_{CC13}	15	25	mA	
WORD WRITE CURRENT: V_{PP} SUPPLY	I_{PP8}	50	25	mA	
BYTE WRITE CURRENT: V_{CC} SUPPLY	I_{CC14}	15	25	mA	
BYTE WRITE CURRENT: V_{PP} SUPPLY	I_{PP9}	50	20	mA	
ERASE CURRENT: V_{CC} SUPPLY	I_{CC15}	15	25	mA	
ERASE CURRENT: V_{PP} SUPPLY	I_{PP10}	50	25	mA	
ERASE SUSPEND CURRENT: V_{CC} SUPPLY (ERASE suspended)	I_{CC16}	8	8	mA	4
ERASE SUSPEND CURRENT: V_{PP} SUPPLY (ERASE suspended)	I_{PP11}	200	200	µA	

NOTE:
1. WRITE operations are tested at V_{CC}/V_{PP} voltages equal to or less than the previous ERASE, and READ operations are tested at V_{CC} voltages equal to or less than the previous WRITE operation.
2. Absolute WRITE/ERASE protection when $V_{PP} \leq V_{PPLK}$.
3. When 5V V_{CC} and V_{PP} are used, V_{CC} cannot exceed V_{PP} by more than 500mV during WRITE and ERASE operations.
4. Parameter is specified when device is not accessed. Actual current draw will be I_{CC12} (5V V_{CC}) or I_{CC16} (3.3V V_{CC}) plus READ current if a READ is executed while the device is in erase suspend mode.

SPEED-DEPENDENT WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

TEST CONDITION 1 (5V)

(0°C ≤ T_A ≤ +70°C; Vcc = +5V ±10%)

AC CHARACTERISTICS		-8			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
WRITE cycle time	^tWC	80		ns	1
WE# HIGH pulse width	^tWPH	30		ns	1
CE# HIGH pulse width	^tCPH	30		ns	1
CE# pulse width	^tCP	50		ns	1
WE# pulse width	^tWP	50		ns	1

TEST CONDITION 2 (3.3V)

(0°C ≤ T_A ≤ +70°C; Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS		-8			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
WRITE cycle time	^tWC	110		ns	2
WE# HIGH pulse width	^tWPH	20		ns	2
CE# HIGH pulse width	^tCPH	20		ns	2
Address setup time to WE# or CE# HIGH	^tAS	80		ns	2
Data setup time to WE# or CE# HIGH	^tDS	80		ns	2
WE# pulse width	^tWP	80		ns	2
CE# pulse width	^tCP	80		ns	2

NOTE: 1. Measurements tested under AC Test Condition 1.
2. Measurements tested under AC Test Condition 2.

WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS: WE#-CONTROLLED WRITES

(0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-8			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Address setup time to WE# HIGH	^tAS	50		ns	
Address hold time from WE# HIGH	^tAH	0		ns	
Data setup time to WE# HIGH	^tDS	50		ns	
Data hold time from WE# HIGH	^tDH	0		ns	
CE# setup time to WE# LOW	^tCS	0		ns	
CE# hold time from WE# HIGH	^tCH	0		ns	
V_{PP} setup time to WE# HIGH	$^tVPS1$	200		ns	1
V_{PP} setup time to WE# HIGH	$^tVPS2$	100		ns	2
RP# HIGH to WE# LOW delay	^tRS	500		ns	
RP# at V_{HH} or WP# HIGH setup time to WE# HIGH	^tRHS	100		ns	3
WRITE duration (WORD or BYTE WRITE)	$^tWED1$	6		µs	4
Boot BLOCK ERASE duration	$^tWED2$	300		ms	3, 4
Parameter BLOCK ERASE duration	$^tWED3$	300		ms	4
Main BLOCK ERASE duration	$^tWED4$	600		ms	4
WE# HIGH to busy status (SR7 = 0)	^tWB	200		ns	5
V_{PP} hold time from status data valid	^tVPH	0		ns	4
RP# at V_{HH} or WP# HIGH hold time from status data valid	^tRHH	0		ns	3
Boot block relock delay time	^tREL		100	ns	6

NOTE:
1. Measured with V_{PP} = V_{PPH1} = 5V.
2. Measured with V_{PP} = V_{PPH2} = 12V.
3. RP# should be held at V_{HH} or WP# held HIGH until boot block WRITE or ERASE is complete.
4. WRITE/ERASE times are measured to valid status register data (SR7 = 1).
5. Polling status register before ^tWB is met may falsely indicate WRITE or ERASE completion.
6. ^tREL is required to relock boot block after WRITE or ERASE to boot block.

WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS: CE#-CONTROLLED WRITES

(0°C ≤ T_A ≤ +70°C; V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-8			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Address setup time to CE# HIGH	^tAS	50		ns	
Address hold time from CE# HIGH	^tAH	0		ns	
Data setup time to CE# HIGH	^tDS	50		ns	
Data hold time from CE# HIGH	^tDH	0		ns	
WE# setup time to CE# LOW	^tWS	0		ns	
WE# hold time from CE# HIGH	^tWH	0		ns	
V_{PP} setup time to CE# HIGH	$^tVPS1$	200		ns	1
V_{PP} setup time to CE# HIGH	$^tVPS2$	100		ns	2
RP# HIGH to CE# LOW delay	^tRS	500		ns	
RP# at V_{HH} or WP# HIGH setup time to CE# HIGH	^tRHS	100		ns	3
WRITE duration (WORD or BYTE WRITE)	$^tWED1$	6		µs	4
Boot BLOCK ERASE duration	$^tWED2$	300		ms	3, 4
Parameter BLOCK ERASE duration	$^tWED3$	300		ms	4
Main BLOCK ERASE duration	$^tWED4$	600		ms	4
CE# HIGH to busy status (SR7 = 0)	^tWB	200		ns	5
V_{PP} hold time from status data valid	^tVPH	0		ns	4
RP# at V_{HH} or WP# HIGH hold time from status data valid	^tRHH	0		ns	3
Boot block relock delay time	^tREL		100	ns	6

NOTE:
1. Measured with V_{PP} = V_{PPH1} = 5V.
2. Measured with V_{PP} = V_{PPH2} = 12V.
3. RP# should be held at V_{HH} or WP# held HIGH until boot block WRITE or ERASE is complete.
4. WRITE/ERASE times are measured to valid status register data (SR7 = 1).
5. Polling status register before ^tWB is met may falsely indicate WRITE or ERASE completion.
6. ^tREL is required to relock boot block after WRITE or ERASE to boot block.

WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS: WE#-CONTROLLED WRITES

(0°C ≤ T_A ≤ +70°C; V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-8			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Address hold time from WE# HIGH	^tAH	0		ns	
Data hold time from WE# HIGH	^tDH	0		ns	
CE# setup time to WE# LOW	^tCS	0		ns	
CE# hold time from WE# HIGH	^tCH	0		ns	
V_{PP} setup time to WE# HIGH	$^tVPS1$	200		ns	1
V_{PP} setup time to WE# HIGH	$^tVPS2$	100		ns	2
RP# HIGH to WE# LOW delay	^tRS	1,000		ns	
RP# at V_{HH} or WP# HIGH setup time to WE# HIGH	^tRHS	200		ns	3
WRITE duration (WORD or BYTE WRITE)	$^tWED1$	6		µs	4
Boot BLOCK ERASE duration	$^tWED2$	300		ms	3, 4
Parameter BLOCK ERASE duration	$^tWED3$	300		ms	4
Main BLOCK ERASE duration	$^tWED4$	600		ms	4
WE# HIGH to busy status (SR7 = 0)	^tWB	200		ns	5
V_{PP} hold time from status data valid	^tVPH	0		ns	4
RP# at V_{HH} or WP# HIGH hold time from status data valid	^tRHH	0		ns	3
Boot block relock delay time	^tREL		200	ns	6

WRITE/ERASE AC TIMING CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS: CE#-CONTROLLED WRITES

(0°C ≤ T_A ≤ +70°C; V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS		-8			
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**UNITS**	**NOTES**
Address hold time from CE# HIGH	^tAH	0		ns	
Data hold time from CE# HIGH	^tDH	0		ns	
WE# setup time to CE# LOW	^tWS	0		ns	
WE# hold time from CE# HIGH	^tWH	0		ns	
V_{PP} setup time to CE# HIGH	$^tVPS1$	200		ns	1
V_{PP} setup time to CE# LOW delay	$^tVPS2$	100		ns	2
RP# HIGH to CE# LOW delay	^tRS	1,000		ns	
RP# at V_{HH} or WP# HIGH setup time to CE# HIGH	^tRHS	200		ns	3
WRITE duration (WORD or BYTE WRITE)	$^tWED1$	6		µs	4
Boot BLOCK ERASE duration	$^tWED2$	300		ms	3, 4
Parameter BLOCK ERASE duration	$^tWED3$	300		ms	4
Main BLOCK ERASE duration	$^tWED4$	600		ms	4
CE# HIGH to busy status (SR7 = 0)	^tWB	200		ns	5
V_{PP} hold time from status data valid	^tVPH	0		ns	4
RP# at V_{HH} or WP# HIGH hold time from status data valid	^tRHH	0		ns	3
Boot block relock delay time	^tREL		200	ns	6

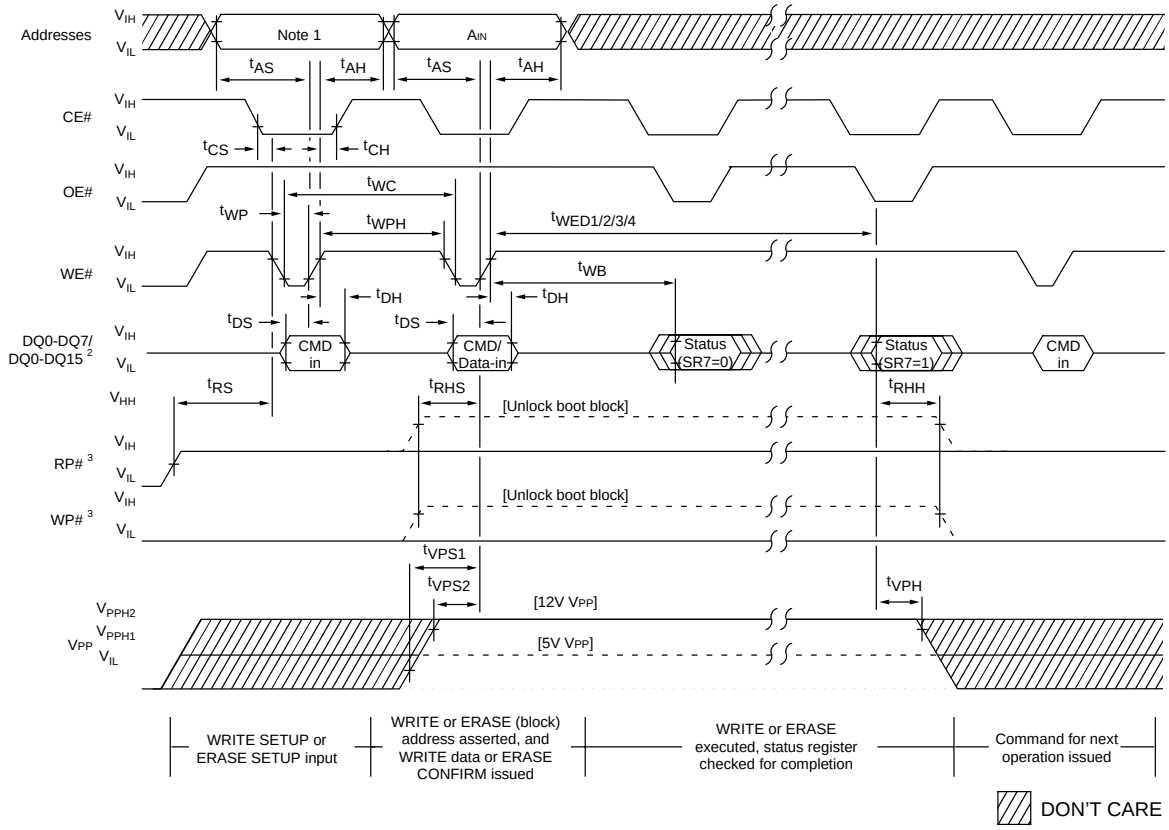
NOTE:
1. Measured with V_{PP} = V_{PPH1} = 5V.
2. Measured with V_{PP} = V_{PPH2} = 12V.
3. RP# should be held at V_{HH} or WP# held HIGH until boot block WRITE or ERASE is complete.
4. WRITE/ERASE times are measured to valid status register data (SR7 = 1).
5. Polling status register before ^tWB is met may falsely indicate WRITE or ERASE completion.
6. ^tREL is required to relock boot block after WRITE or ERASE to boot block.

WORD/BYTE WRITE AND ERASE DURATION CHARACTERISTICS

	5V V_{PP}				12V V_{PP}					
	3.3V V_{CC}		5V V_{CC}		3.3V V_{CC}		5V V_{CC}			
PARAMETER	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	UNITS	NOTES
Boot/parameter BLOCK ERASE time	0.8	7	0.8	7	0.5	7	0.5	7	s	1
Main BLOCK ERASE time	2	14	2	14	1.1	14	1.1	14	s	1
Main BLOCK WRITE time (byte mode)	1.8	–	1.8	–	1	–	1	–	s	1, 2, 3
Main BLOCK WRITE time (word mode)	1.1	–	1.1	–	0.6	–	0.6	–	s	1, 2, 3

NOTE: 1. Typical values measured at T_A = +25°C.
2. Assumes no system overhead.
3. Typical WRITE times use checkerboard data pattern.

WRITE/ERASE CYCLE
WE#-CONTROLLED WRITE/ERASE



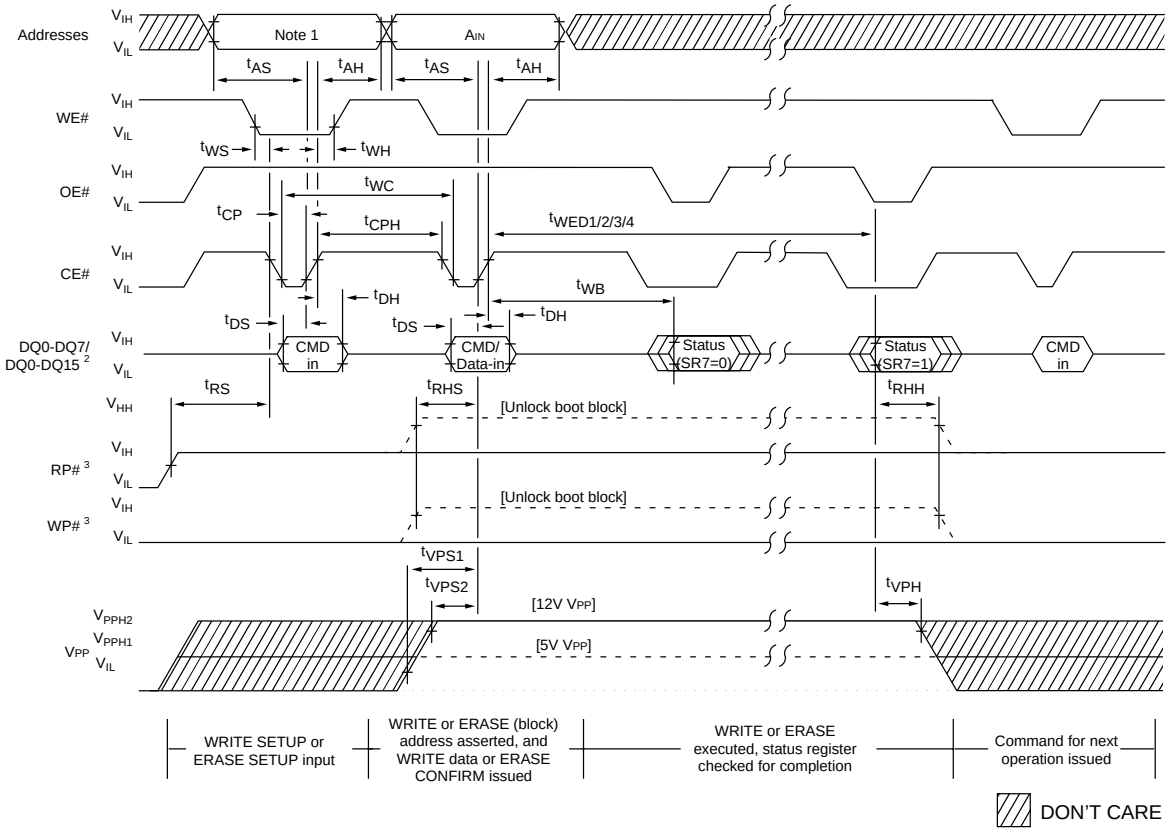
5V AND 3.3V TIMING PARAMETERS

SYMBOL	-8 MIN	-8 MAX	UNITS
tWC (5V)[4]	80		ns
tWC (3.3V)[5]	110		ns
tWPH (5V)[4]	30		ns
tWPH (3.3V)[5]	20		ns
tWP (5V)[4]	50		ns
tWP (3.3V)[5]	80		ns
tAS (5V)	50		ns
tAS (3.3V)[5]	80		ns
tAH	0		ns
tDS (5V)	50		ns
tDS (3.3V)[5]	80		ns
tDH	0		ns
tCS	0		ns
tCH	0		ns

SYMBOL	-8 MIN	-8 MAX	UNITS
tVPS1	200		ns
tVPS2	100		ns
tRS (5V)	500		ns
tRS (3.3V)	1,000		ns
tRHS (5V)	100		ns
tRHS (3.3V)	200		ns
tWED1	6		µs
tWED2	300		ms
tWED3	300		ms
tWED4	600		ms
tWB	200		ns
tVPH	0		ns
tRHH	0		ns

NOTE: 1. Address inputs are "Don't Care" but must be held stable.
2. If BYTE# is LOW, data and command are 8-bit. If BYTE# is HIGH, data is 16-bit and command is 8-bit.
3. Either RP# at VHH or WP# HIGH unlocks the boot block.
4. Measurements tested under AC Test Condition 1, VCC = 5V ±10%.
5. Measurements tested under AC Test Condition 2, VCC = 3.3V ±0.3V.

WRITE/ERASE CYCLE
CE#-CONTROLLED WRITE/ERASE



5V AND 3.3V TIMING PARAMETERS

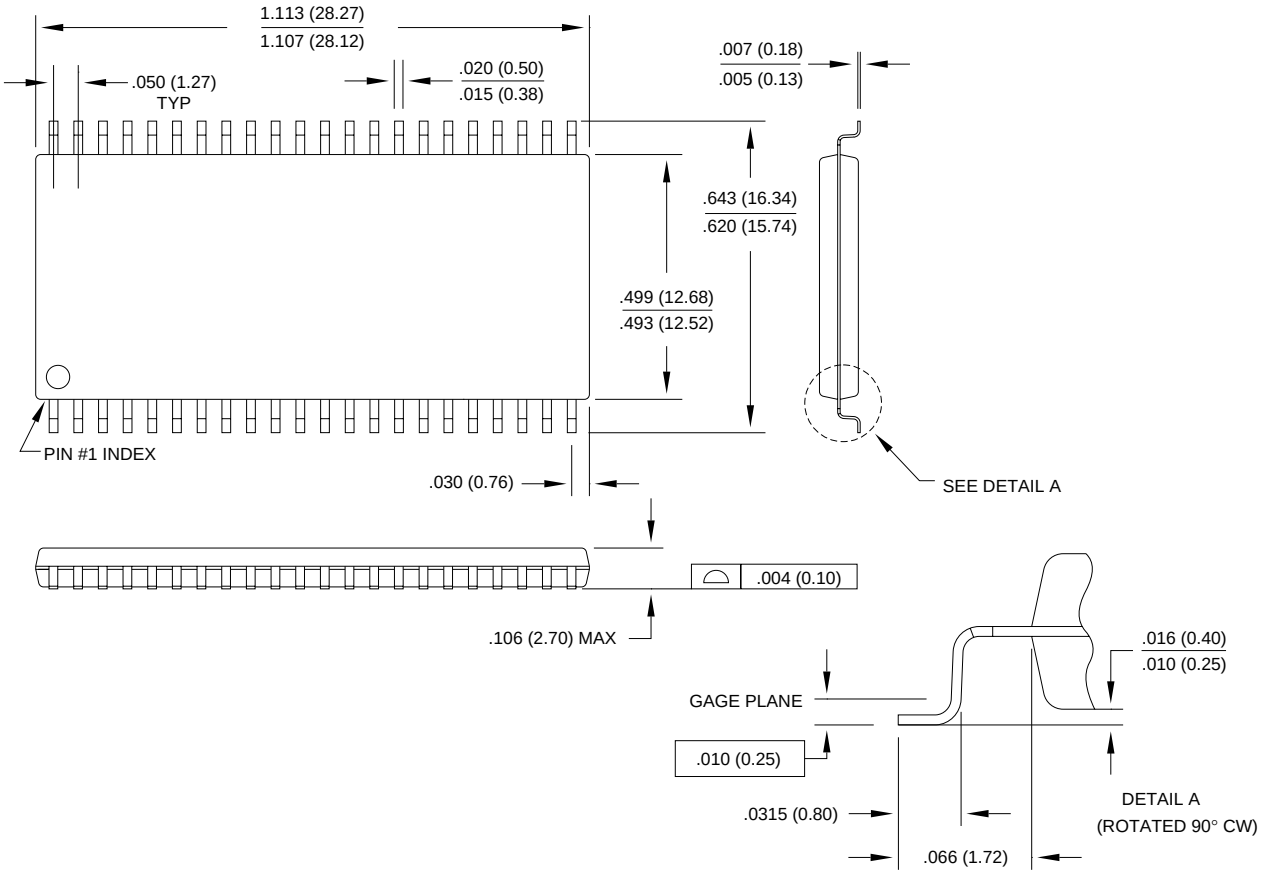
SYMBOL	-8 MIN	-8 MAX	UNITS
tWC (5V)[4]	80		ns
tWC (3.3V)[5]	110		ns
tCPH (5V)[4]	30		ns
tCPH (3.3V)[5]	20		ns
tCP (5V)[4]	50		ns
tCP (3.3V)[5]	80		ns
tAS (5V)	50		ns
tAS (3.3V)[5]	80		ns
tAH	0		ns
tDS (5V)	50		ns
tDS (3.3V)[5]	80		ns
tDH	0		ns
tWS	0		ns
tWH	0		ns

SYMBOL	-8 MIN	-8 MAX	UNITS
tVPS1	200		ns
tVPS2	100		ns
tRS (5V)	500		ns
tRS (3.3V)	1,000		ns
tRHS (5V)	100		ns
tRHS (3.3V)	200		ns
tWED1	6		µs
tWED2	300		ms
tWED3	300		ms
tWED4	600		ms
tWB	200		ns
tVPH	0		ns
tRHH	0		ns

NOTE: 1. Address inputs are "Don't Care" but must be held stable.
2. If BYTE# is LOW, data and command are 8-bit. If BYTE# is HIGH, data is 16-bit and command is 8-bit.
3. Either RP# at VHH or WP# HIGH unlocks the boot block.
4. Measurements tested under AC Test Condition 1, VCC = 5V ±10%.
5. Measurements tested under AC Test Condition 2, VCC = 3.3V ±0.3V.

44-PIN PLASTIC SOP (600 mil)

B-1

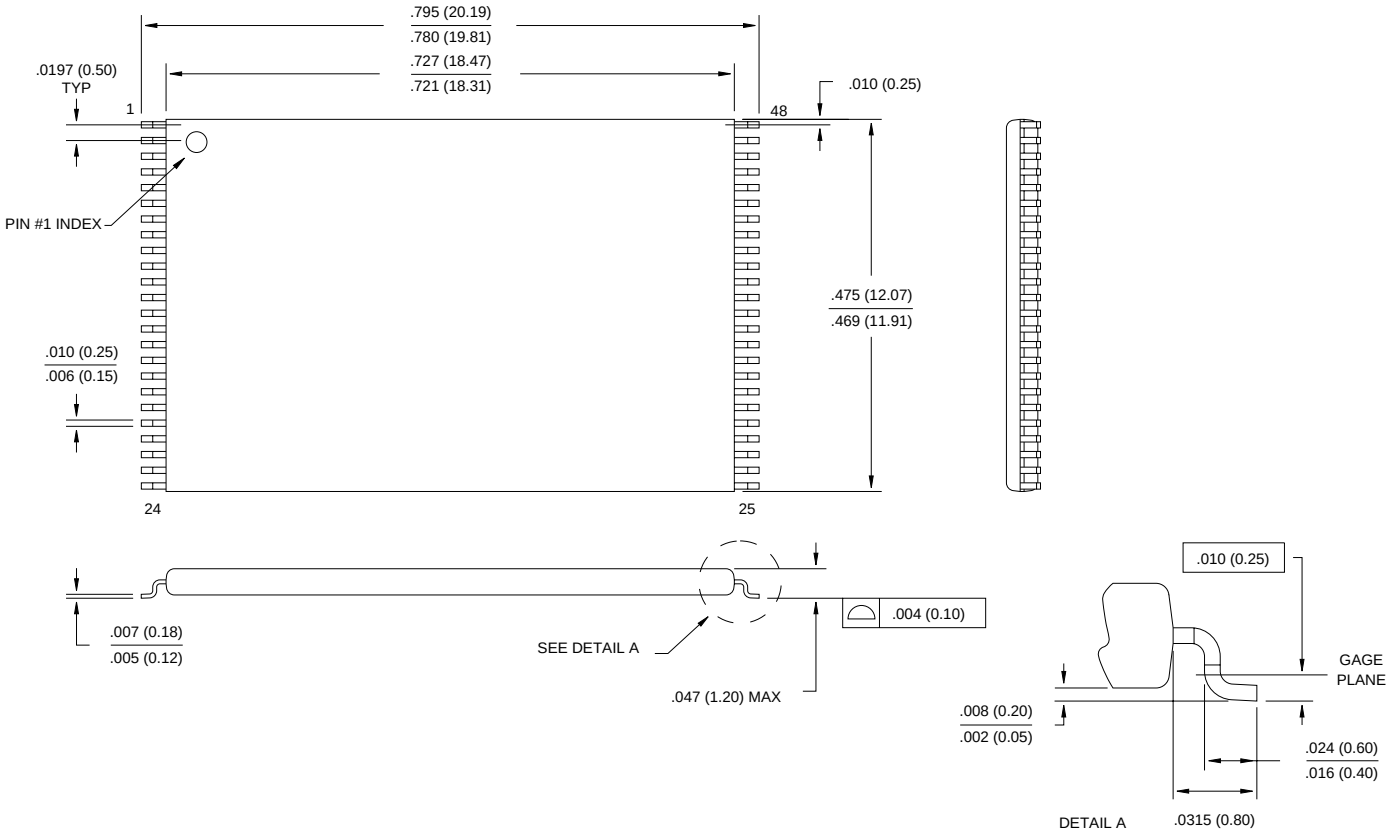


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01” per side.

48-PIN PLASTIC TSOP I (12mm x 20mm)

C-3



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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