MP1230A/31A/32A

CMOS Microprocessor Compatible
Double-Buffered 12-Bit
Digital-to-Analog Converter

FEATURES

- **Superior Ruggedized 1230 Series: 2 KV ESD**
- **Four Quadrant Multiplication**
- **Stable, More Accurate Segmented DAC Approach**
  - **0.2 ppm/°C Linearity Tempco**
  - **2 ppm/°C Max Gain Error Tempco**
  - **Lowest Sensitivity to Amplifier Offset**
  - **Lowest Output Capacitance (C_{OUT} = 80pF)**
  - **Lower Glitch Energy**
- **Monotonic over Temperature Range**
- **Lower Data Bus Feedthrough @ $\overline{CS}$ = 1**
- **V_{DD} from +11 V to +16 V**
- **Latch-Up Free CMOS Technology**
- **12-Bit Bus Version: MP1208/1209/1210**
- **16-Bit Upgrade: MP7636A**

GENERAL DESCRIPTION

The MP1230A series are superior pin for pin replacements for the 1230 series. The MP1230A series is manufactured using advanced thin film resistors on a double metal CMOS process which promotes significant improvements in reliability, latch-up free performance and ESD protection.

The MP1230A series incorporates a unique decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. 12-bit linearity is achieved without trimming. Outstanding features include:

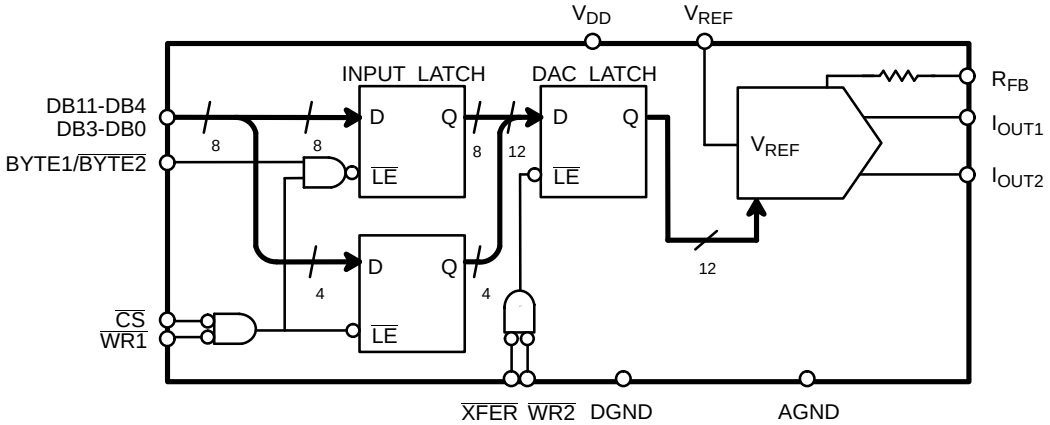
– Stability: integral and differential linearity tempcos are rated at 0.2 ppm/°C typical. Monotonicity is guaranteed over all temperature ranges. Scale factor tempco is a low 2 ppm/°C maximum.

– Low Output Capacitance: Due to smaller MOSFET switch geometries allowed by decoding, the output capacitance at I_{OUT1} and I_{OUT2} is a low 80pF / 40pF and 25pF / 65 pF. This less than half the competitive DAC 1230 series. Lower capacitance allows the MP1230A series to achieve settling times faster than 1 µs for a 10 V step.

– Low Sensitivity to Output Amplifier Offset: The linearity error caused by amplifier offset is reduced by a factor of 2 in the MP1230A series over conventional R-2R DACs.

The MP1230A series uses a circuit which reduces transients in the supplies caused by DATA bus transitions at $\overline{CS}$ = 1.

SIMPLIFIED BLOCK DIAGRAM

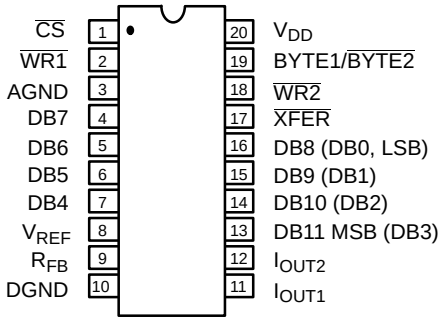


ORDERING INFORMATION

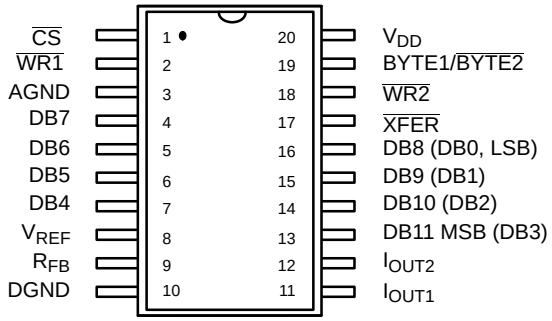
Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	–40 to +85°C	MP1230ABN	±1/2	±3/4	±0.4
Plastic Dip	–40 to +85°C	MP1231ABN	±1	±1	±0.4
Plastic Dip	–40 to +85°C	MP1232ABN	±2	±2	±0.4
SOIC	–40 to +85°C	MP1230ABS	±1/2	±3/4	±0.4
SOIC	–40 to +85°C	MP1231ABS	±1	±1	±0.4
SOIC	–40 to +85°C	MP1232ABS	±2	±2	±0.4

PIN CONFIGURATIONS

See Packaging Section for Package Dimensions



20 Pin PDIP (0.300”)
N20



20 Pin SOIC (Jedec, 0.300”)
S20

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION
1	$\overline{CS}$	Chip Select (Active Low)
2	$\overline{WR1}$	Write 1 (Active Low)
3	AGND	Analog Ground
4	DB7	Data Input Bit 7
5	DB6	Data Input Bit 6
6	DB5	Data Input Bit 5
7	DB4	Data Input Bit 4
8	V_{REF}	Reference Input Voltage
9	R_{FB}	Feedback Resistor
10	DGND	Digital Ground
11	I_{OUT1}	Current Output 1

PIN NO.	NAME	DESCRIPTION
12	I_{OUT2}	Current Output 2
13	DB11 (DB3)	Data Input Bit 11 (MSB) Data Input Bit 3
14	DB10 (DB2)	Data Input Bit 10 Data Input Bit 2
15	DB9 (DB1)	Data Input Bit 9 Data Input Bit 1
16	DB8 (DB0)	Data Input Bit 8 Data Input Bit 0 (LSB)
17	$\overline{XFER}$	Transfer Control Signal (Active Low)
18	$\overline{WR2}$	Write 2 (Active Low)
19	BYTE1/ $\overline{BYTE2}$	Byte Sequence Control
20	V_{DD}	Positive Power Supply

ELECTRICAL CHARACTERISTICS
(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE[1]								FSR = Full Scale Range
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
MP1230ABN/ATD/ABS				±1/2		±1/2		
MP1231ABN/ATD/ABS				±1		±1		
MP1232ABN/ATD/ABS				±2		±2		
Differential Non-Linearity	DNL						LSB	
MP1230ABN/ATD/ABS				±3/4		±3/4		
MP1231ABN/ATD/ABS				±1		±1		
MP1232ABN/ATD/ABS				±2		±2		
Gain Error	GE			±0.4		±0.4	% FSR	Using Internal R_{FB}
Gain Temperature Coefficient[2]	TC_{GE}		0.5			±2	ppm/°C	ΔGain/ΔTemperature
Power Supply Rejection Ratio	PSRR		5	±20		±20	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 0.25V
Output Leakage Current	I_{OUT}		1	±10		±200	nA	
DYNAMIC PERFORMANCE[2]								R_L=100Ω, C_L=13pF
Current Settling Time	t_S		1.0				µsec	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT1}	F_T		1.0				mV p-p	V_{REF}=100kHz, 20Vp-p, sinewave
REFERENCE INPUT								
Input Resistance	R_{IN}	5	10	20	5	20	kΩ	
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	3.0	2.4		3.0		V	
Logical "0" Voltage	V_{IL}			0.8		0.8	V	
Input Leakage Current	I_{LKG}			±1		±1	µA	V_{IN} = 0, 5 V
Input Capacitance[2]			10				pF	
ANALOG OUTPUTS[2]								
Output Capacitance								
	C_{OUT1}		80	100		100	pF	DAC Inputs all 1's
	C_{OUT1}		40	60		60	pF	DAC Inputs all 0's
	C_{OUT2}		65	85		85	pF	DAC Inputs all 1's
	C_{OUT2}		25	45		45	pF	DAC Inputs all 0's
POWER SUPPLY								
Functional Voltage Range[4]	V_{DD}	+4.5		+16	+4.5	+16	V	
Supply Current	I_{DD}		1.2	2.0		2.0	mA	All digital inputs = 0 V or all = 5 V

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
SWITCHING CHARACTERISTICS[2, 3]								
Chip Select to Write Set-Up Time	t_{CS}	200	100				ns	
Chip Select to Write Hold Time	t_{CH}	10	0				ns	
Data Valid to Write Set-Up Time	t_{DS}	100	50				ns	
Data Valid to Write Hold Time	t_{DH}	90	70				ns	
Write Pulse Width,	t_{WR}	100	50				ns	

NOTES:

1 Full Scale Range (FSR) is 10V.
2 Guaranteed but not production tested.
3 See timing diagram.
4 Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2]

V_{DD} to GND ..... +17 V
Digital Input Voltage to GND .... GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to +6.5 V
V_{REF} to GND ..... ±25 V
V_{RFB} to GND ..... ±25 V
AGND to DGND ..... ±1 V
(Functionality Guaranteed ±0.5 V)

Storage Temperature ..... –65°C to +150°C

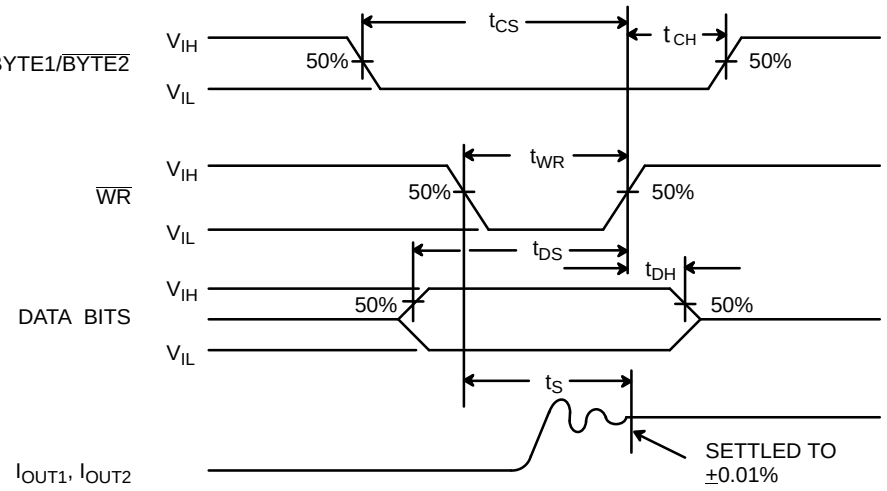
Lead Temperature (Soldering, 10 seconds) ..... +300°C

Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC 900mW
Derates above 75°C ..... 12mW/°C

NOTES:

1 Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
2 Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.
3 GND refers to AGND and DGND.

TIMING DIAGRAM



DEFINITION OF CONTROL SIGNALS:

$\overline{CS}$: Chip Select.(Active low)
It will enable $\overline{WR1}$.

$\overline{WR1}$: Write 1 (Active low)
The $\overline{WR1}$ is used to load the digital data bits (DB) into the input latch.

BYTE1/$\overline{BYTE2}$: Byte sequence control.
The BYTE1/$\overline{BYTE2}$ control pin is used to select both MSB and LSB input latches.

$\overline{WR2}$: Write 2 (Active low)
It will enable $\overline{XFER}$.

$\overline{XFER}$: Transfer control signal (Active low)
This signal in combination with $\overline{WR2}$ causes the 16-bit data which is available in the input latches to transfer to the DAC register

DB0 to DB11: Digital Inputs.
DB0 is the least significant digital input (LSB) and DB11 is the most significant digital input (MSB).

I_{OUT1}: DAC Current Output 1 Bus.
I_{OUT1} is a maximum for a digital code of all 1's in the DAC register, and is zero for all 0's in the DAC register.

I_{OUT2}: DAC Current Output 2 Bus.
I_{OUT2} is a complement of I_{OUT1}.

R_{FB}: Feedback Resistor.
This internal feedback resistor should always be used (not an external resistor) since it matches the resistors in the DAC and tracks these resistors over temperature.

V_{REF}: Reference Voltage Input.
This input connects an external precision voltage source to the internal DAC. The V_{REF} can be selected over the range of +25V to –25V or the analog signal for a 4-quadrant multiplying mode application.

V_{DD}: Power Supply Voltage.
This is the power supply pin for the part. The V_{DD} can be from +5 V DC to +15 V DC, however optimum voltage is +12 to +15 V DC.

AGND: Analog Ground
Back gate of the DAC N-channel current steering switches.

DGND: Digital Ground

THEORY OF OPERATION

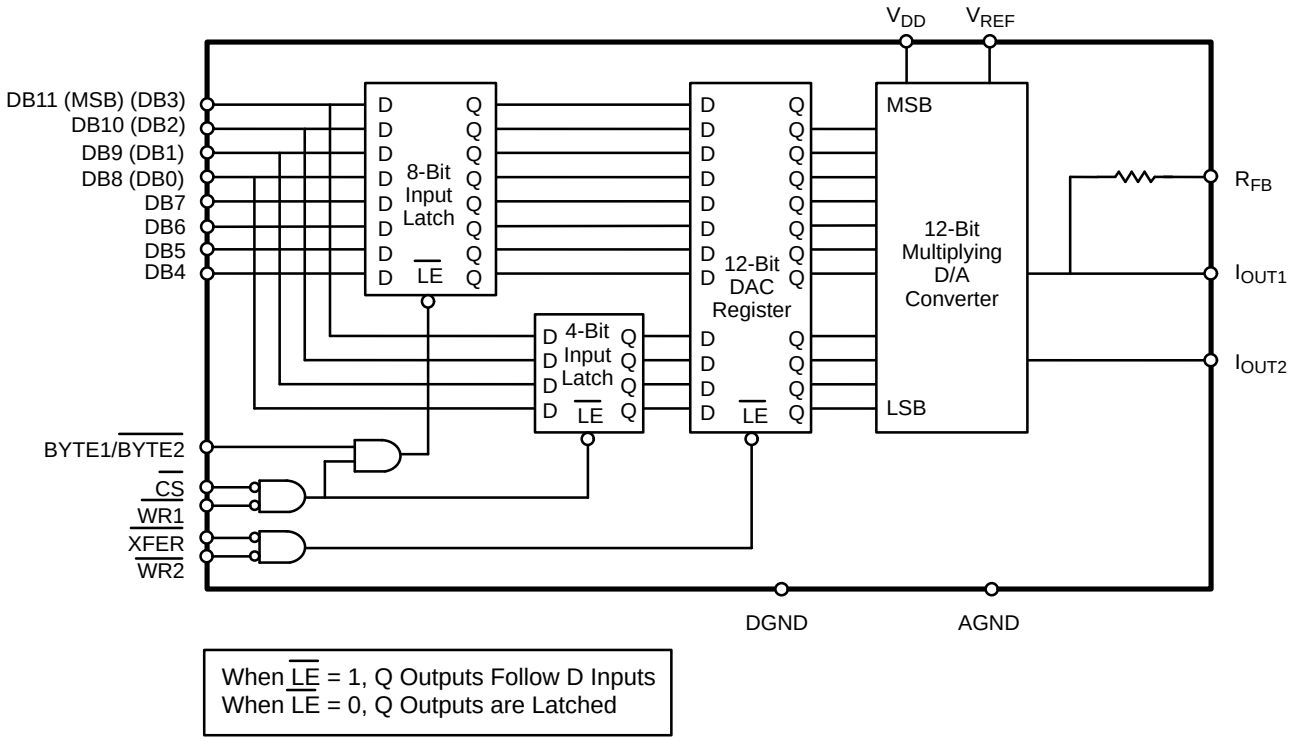


Figure 1. Functional Diagram

Digital Interface

Figure 1. shows the internal control logic that controls the writing of the input latches. It is easy to understand how the MP1230A/31A/32A works by understanding each basic operation.

Writing to Input Latches

The condition BYTE1/$\overline{BYTE2}$= high, $\overline{CS}$ = $\overline{WR1}$ = 0 loads the data bus DB11-DB4 into both input latches.

A second cycle with BYTE1/$\overline{BYTE2}$ = low (*Figure 2.*) loads the pins DB11-DB8 (DB3-DB0) into the 4-bit input latch.

Timing diagrams show the inputs $\overline{CS}$ and DB11-DB0 to be stable during the entire writing cycle. In reality all the above signals can change (*Figure 2.*) as long as they meet the timing conditions specified in the Electrical Characteristic Table.

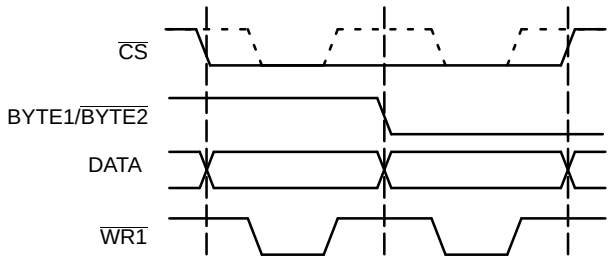


Figure 2. Write Cycles to Input Latches

Transferring Data to the DAC Latches

Once one or all the input latches have been loaded, the condition $\overline{XFER}$= $\overline{WR2}$= low transfers the content of the input latches in the DAC latch. The outputs of the DAC latch change and the DAC current (I_{OUT}) will reach a new stable value within the settling time t_S (*Figure 3.*).

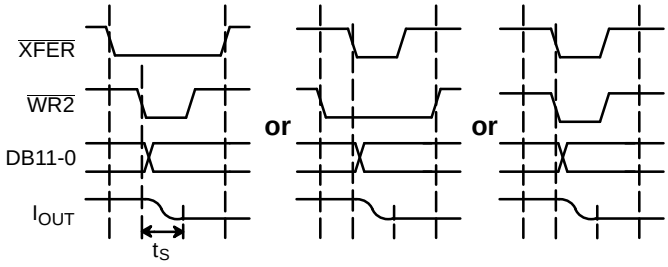
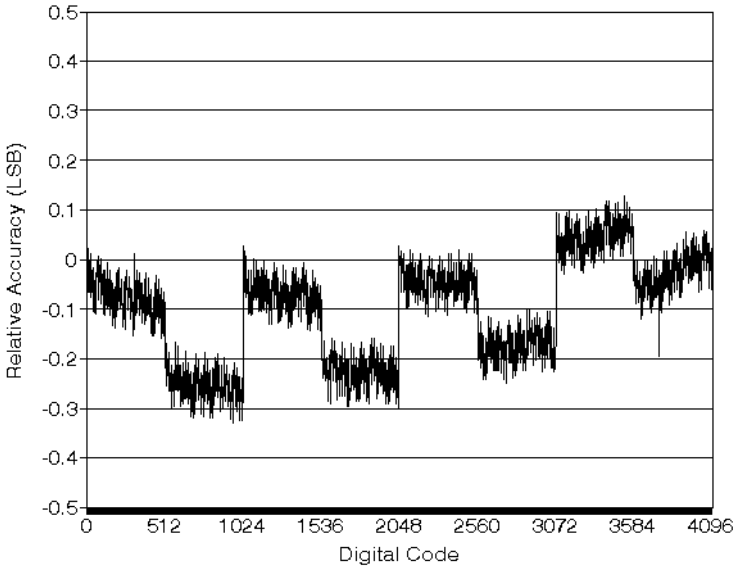


Figure 3. Transfer Cycles from Input Latches to DAC Latches

PERFORMANCE CHARACTERISTICS

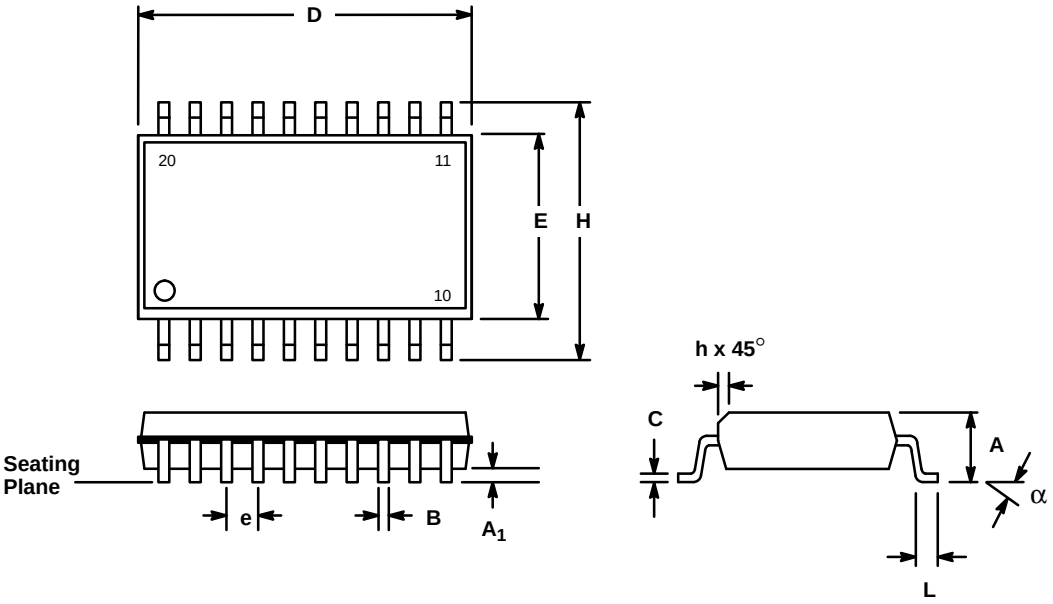


Graph 1. Relative Accuracy vs. Digital Code

APPLICATION NOTES

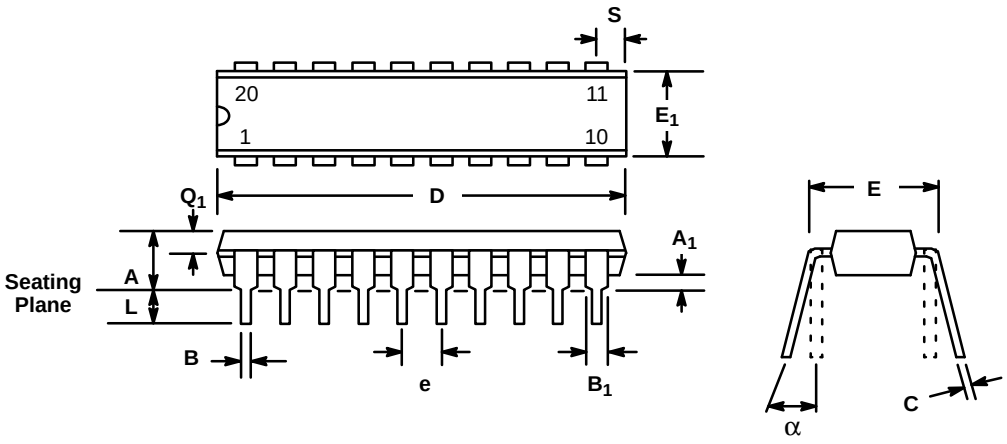
Refer to Section 8 for Applications Information

20 LEAD SMALL OUTLINE
(300 MIL JEDEC SOIC)
S20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.097	0.104	2.464	2.642
A_1	0.0050	0.0115	0.127	0.292
B	0.014	0.019	0.356	0.483
C	0.0091	0.0125	0.231	0.318
D	0.500	0.510	12.70	12.95
E	0.292	0.299	7.42	7.59
e	0.050 BSC		1.27 BSC	
H	0.400	0.410	10.16	10.41
h	0.010	0.016	0.254	0.406
L	0.016	0.035	0.406	0.889
α	0°	8°	0°	8°

20 LEAD PLASTIC DUAL-IN-LINE
(300 MIL PDIP)
N20



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	—	0.200	—	5.08
A_1	0.015	—	0.38	—
B	0.014	0.023	0.356	0.584
B_1 (1)	0.038	0.065	0.965	1.65
C	0.008	0.015	0.203	0.381
D	0.945	1.060	24.0	26.92
E	0.295	0.325	7.49	8.26
E_1	0.220	0.310	5.59	7.87
e	0.100 BSC		2.54 BSC	
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°
Q_1	0.055	0.070	1.40	1.78
S	0.040	0.080	1.02	2.03

Note: (1) The minimum limit for dimensions B1 may be 0.023" (0.58 mm) for all four corner leads only.

Notes

Notes

NOTICE

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