Micro Linear

ML4816

High Frequency Multi-Mode Resonant Controller

GENERAL DESCRIPTION

The ML4816 controller IC is suitable for a wide range of resonant converter topologies. This controller can be used with Zero Current Switched (ZCS) Quasi-Resonant Converters (QRC) requiring constant on-time and modulated off-time, as well as frequency modulated converters, such as Series Resonant Converters operating above resonance.

The ML4816's oscillator features independent control of charging and discharging currents (on-time and off-time). Output frequency can be determined either directly proportional, or inversely proportional, to the controlling voltage. In addition both upper and lower frequency limits (f_{MIN} and f_{MAX}) can be independently set.

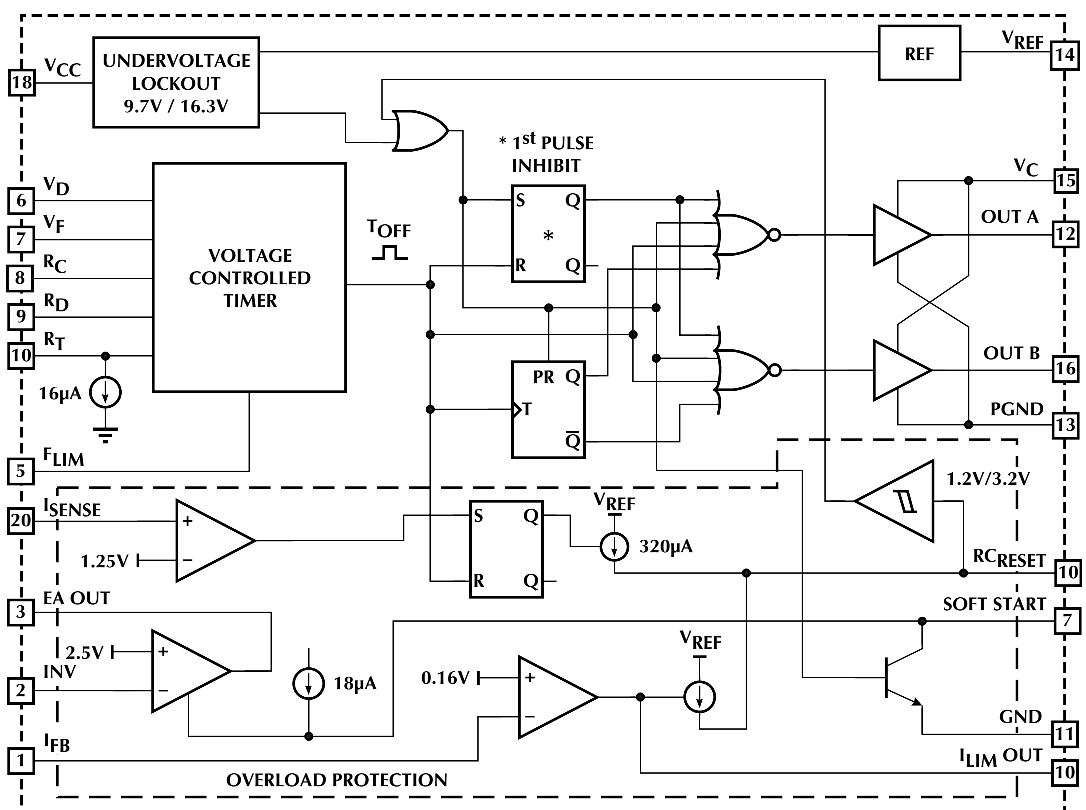
Both pulse-by-pulse and DC current limiting are available. Overload protection (shutdown) is triggered after a programmable delay time. Restart after overload shutdown can be delayed by a programmable time. Internal logic disables the gate drive until the oscillator is stable.

The ML4816 includes under-voltage lockout with 6V hysteresis, and high current high speed totem pole output drivers for external MOSFETs.

FEATURES

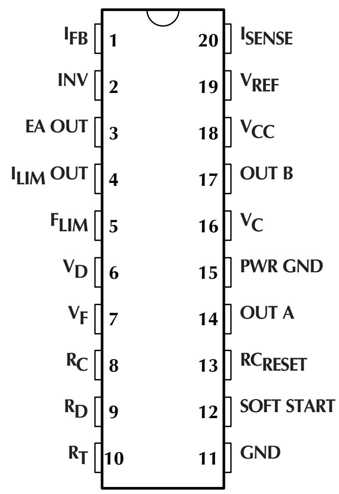
- Supports Zero Current Switched (ZCS) quasi-resonant converters
- Supports Series Resonant (ZVS) converters operating above resonance
- Wide oscillator frequency range
- Programmable f_{MIN} and f_{MAX} limits
- Practical operation to 2.5MHz (f_{OSC})
- Low start up current and under voltage lockout circuits support off line operation
- Pulse-by-pulse or DC current limiting
- Integrating soft start reset (fault integration) with programmable restart delay
- High current (1.5A peak) totem-pole output drive
- Precision buffered 5V reference (±1%)

BLOCK DIAGRAM



PIN CONFIGURATION

ML4816
20-Pin PDIP (P20)
20-Pin SOIC (S20)



TOP VIEW

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	I_{FB}	Input for load current limit
2	INV	Inverting input to error amplifier
3	EA OUT	Output of error amplifier
4	I_{LIM} OUT	Output for the load current limit amplifier
5	F_{LIM}	A voltage input sets the maximum on time for the timer
6	V_D	Controls the C_T discharge current and oscillator off time. Connected to error amplifier output for off time modulation and to V_{REF} for constant off time.
7	V_F	Controls the charging current and oscillator on time. Connected to the error amplifier for on time modulation, or connected to GND for constant on time.
8	R_C	External timing resistor to either GND or V_{REF} sets the charging current (oscillator on time). This pin can either source or sink current.
9	R_D	External resistor from this pin to GND sets the oscillator discharge current (off time)
10	R_T	Timing capacitor for oscillator
11	GND	Signal ground
12	SOFT START	Normally connected to soft start capacitor
13	RC_{RESET}	Timing elements tor Integrating fault detection and reset delay circuits
14	OUT A	High current totem pole output
15	PWR GND	Return for the high current totem pole outputs
16	V_C	Supply for the high current totem pole outputs
17	OUT B	High current totem pole output
18	V_{CC}	Positive supply
19	V_{REF}	Buffered output for the 5.0V voltage reference
20	I_{SENSE}	Primary current sense input for current limit

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_{CC} and V_C 30V
Soft Start Output Current
DC 0.5A
Pulse (0.5µs) 1.5A
Analog Inputs .... GND – 0.3V to 6.3V
Amplifier Output Current 5mA

R_C Current 100µA
R_D Current 100µA
Junction Temperature .... 150°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 260°C
Thermal Resistance (θ_{JA}) .... 65°C/W

OPERATING CONDITIONS

Temperature Range .... 0°C to 70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{CC} = 15V, CT = 470pF, T_A = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE						
V_{OH}	Output Voltage	T_A = 25ºC, I_O = –1mA	4.90	5.00	5.10	V
	Line Regulation	12V < V_{CC} < 25V		2	20	mV/V
	Load Regulation	1mA < I_O < 10mA		5	20	mV/V
	Temperature Stability	$T_{MIN} \leq T_A \leq T_{MAX}$		0.2	0.4	mV/ºC
	Total Variation	Line, load, temp	4.85		5.15	V
	Output Noise Voltage	10Hz < f < 10kHz		50		µV
	Long Term Stability	T_J = 125ºC, 1000 hours		5	25	mV
	Short Circuit Current	V_{REF} = 0	–40	–70	–100	mA
ERROR AMPLIFIER						
V_{NI}	Non-Inverting Input Voltage		2.37	2.47	2.57	V
	Input Bias Current				3	µA
	Open Loop Gain	1V ≤ V_O ≤ 4V	60			mV
	Unity Gain Bandwidth		2.5	2.8		MHz
	PSRR	12V ≤ V_{CC} ≤ 25V	65			dB
	Output Sink Current	INV = 2.7V, EA OUT = 1V	1	2.8		mA
	Output Source Current	INV = 2.3V, EA OUT = 4V	–0.5	–2.2		mA
V_{OH}	Output High Voltage	EA OUT = –0.5mA	5.0	5.5	6.0	V
V_{OL}	Output Low Voltage	EA OUT = 1mA		0.5	1	V
	Slew Rate			8.5		V/µs
CURRENT LIMITING AMPLIFIER						
	Non-Inverting Input Voltage		0.145	0.17	0.2	V
	Input Bias Current				3	µA
	Open Loop Gain	1V ≤ V_O ≤ 4V	65			dB
	Unity Gain Bandwidth		1.0	1.5		MHz
	PSRR	12V ≤ V_{CC} ≤ 25V	65		0.8	dB
	Output Sink Current	I_{FB} = I_{LIM} OUT = 1V	1.0	1.6		mA

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT LIMITING AMPLIFIER (Continued)						
	Output Source Current	I_{FB} = 0V, I_{LIM} OUT = 4V	–0.5	–1.1		mA
V_{OH}	Output High Voltage	I_{LIM} OUT = –0.5mA	6.0	7.2	8.0	V
V_{OL}	Output Low Voltage	I_{LIM} OUT = 1mA		0.7	1.0	V
	Slew Rate			0.9		V/µs
CURRENT SENSE						
	Input Bias Current	I_{SENSE} = 0V			–2	µA
	Current Sense Threshold		1.20	1.25	1.30	V
	Delay to RC_{RESET}			80	150	ns
SOFT START						
	Discharging Current	SOFT START = 1V, RC_{RESET} = 4V	20	35		mA
	Charging Current	SOFT START = 1V, RC_{RESET} = 0V	–16	–21	–26	µA
OVERLOAD PROTECTION						
	Overload Threshold		3.0	3.2	3.5	V
	Restart Threshold		1.0	1.2	1.4	V
	Pulse-by-Pulse Charging Current	RC_{RESET} = 2V, I_{SENSE} = 1.35V		–320		µA
	Current Limit Amplifier Controlled Current	I_{FB} = 0V, RC_{RESET} = 2V, I_{LIM} OUT = 1V I_{LIM} OUT = 2.5V		 –2.2 –0.9		 mA mA
VOLTAGE CONTROLLED TIMER						
	C_T Minimum Discharging Current	V_D = 0V, C_T = 3V	14.0	18.5	22.0	µA
	C_T Peak Voltage			3.75		V
	C_T Valley Voltage					V
	R_C Minimum Voltage/V_{REF} Ratio	F_{LIM} = V_F = 0V, 25kΩ R_C to GND	0.446	0.455	0.464	
	R_C Voltage/V_{REF} Ratio	F_{LIM} = 8V + 11V_{REF}, V_F = 5V, 25kΩ R_C to GND	0.713	0.720	.742	
	R_D Minimum Voltage/V_{REF} Ratio	V_D = 0V, 3kΩ R_D to GND			0	V
	R_D Maximum Voltage/V_{REF} Ratio	V_D = 5V, 3kΩ R_D to GND	0.425	0.450	0.475	
T_{ON}	At Ambient	F_{LIM} = V_F = 0V, V_D = 3V, 25kΩ R_C to GND, 3kΩ R_D to GND	0.62	0.68	0.75	µs
T_{ON}	Total Variation	12V ≤ V_{CC} ≤ 25V, T_{MIN} ≤ T_A ≤ T_{MAX}	0.60	0.71	0.79	µs
O_D	Output Deadtime At Ambient	F_{LIM} = V_F = 0V, V_D = 5V, 25kΩ R_C to GND, 3kΩ R_D to GND	100	120	145	ns
O_D	Output Deadtime , Total Variation	12V ≤ V_{CC} ≤ 25V, T_{MIN} ≤ T_A ≤ T_{MAX}	100	120	155	ns

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VOLTAGE CONTROLLED TIMER (Continued)						
F_{MAX}	Maximum Frequency	$F_{LIM} = V_F = 0V$, $V_D = 5V$, 25kΩ R_C to GND, 3kΩ R_D to GND	1.0	1.2	1.4	MHz
		$F_{LIM} = 8V + 11V_{REF}$, $V_D = 5V$, $V_F = 2V$, 22kΩ R_C to V_{REF}, 3kΩ R_D to GND	1.1	1.33	1.55	MHz
F_{MIN}	Minimum Frequency	$F_{LIM} = V_F = 0V$, $V_D = 1.4V$, 25kΩ R_C to GND, 3kΩ R_D to GND	17	22	28	kHz
		$F_{LIM} = 8V + 11V_{REF}$, $V_D = 5V$, $V_F = 2V$, 22kΩ R_C to V_{REF}, 3kΩ R_D to GND	650	800	850	kHz
UNDER VOLTAGE LOCKOUT						
	Start Threshold		15.0	16.3	16.8	V
	Stop Threshold		9.2	9.7	10.2	V
SUPPLY CURRENT						
	Start Up Current	$V_{CC} = 15V$	1.2	1.75	2.3	mA
I_{CC}	Operating Supply Current	$F_{LIM} = V_F = 0V$, $V_D = 5V$, 25kΩ R_C to GND, 3kΩ R_D to GND, $C_{LA} = C_{LB} = 0F$, $T_A = 25ºC$	26	32	38	mA
		$T_{MIN} \leq T_A \leq T_{MAX}$			53	mA
OUTPUT						
	Output Low Level	$I_{SINK} = 20mA$		0.1	0.4	V
		$I_{SINK} = 200mA$		0.7	2.2	V
	Output High Level	$I_{SOURCE} = 20mA$	12.0	13.5		V
		$I_{SOURCE} = 200mA$	11.5	13.0		V
t_R	Rise Time	$C_{LA} = C_{LB} = 1nF$			60	ns
t_F	Fall Time	$C_{LA} = C_{LB} = 1nF$			60	ns

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case conditions

FUNCTIONAL DESCRIPTION

OSCILLATOR

Refer to Figure 1a. The oscillator is the core of the ML4816 and is designed to allow maximum flexibility. This oscillator can be used in two basic modes of operation:

1. On time proportional to V_{IN} and fixed off time with a maximum on time limit (where V_{IN} is the output of the error amplifier).

2. Off time inversely proportional to V_{IN} and fixed on time.

The internal CLOCK signal (Figure 1b) turns the outputs off at its rising edge. The clock signal remains high and the outputs stay off as long as C_T is discharging. The discharge time T_{OFF} of C_T is:

$$T_{OFF} = \frac{165 \times C_T \times R_D}{10 \times (V_D - 2V) + 16\mu A \times R_D} \quad (1)$$

Variable Off Time, Constant On Time

Refer to Figure 2. When using a variable off time control, V_D is tied to the output of the error amplifier. Off time is given by equation (1). The 16µA current sink prevents the off time from becoming infinite, thereby providing an upper limit to T_{OFF} of

$$T_{OFFMAX} = C_T \times 103 \times 10^5 \quad (2)$$

The on time is given by:

$$T_{ON} = 0.0605 \times R_C \times C_T \quad (3)$$

Variable On Time, Constant Off Time

The on time (T_{ON}) is controlled by the current flowing from V_{REF} through R_C into buffer B2. The output of B2 is internally limited to be no less than 2.27V and no greater than F_{LIM}.

The on time for Figure 3 is given by:

$$T_{ON} = \frac{0.138 \times R_C \times CT}{V_{REF} - V_F} \quad (4)$$

Where F_{LIM} > 2.27V the maximum on time is given by:

$$T_{ONMAX} = \frac{0.138 \times R_C \times CT}{V_{REF} - F_{LIM}} \quad (5)$$

The minimum on time is:

$$T_{ONMIN} = 0.0506 \times R_C \times C_T \quad (6)$$

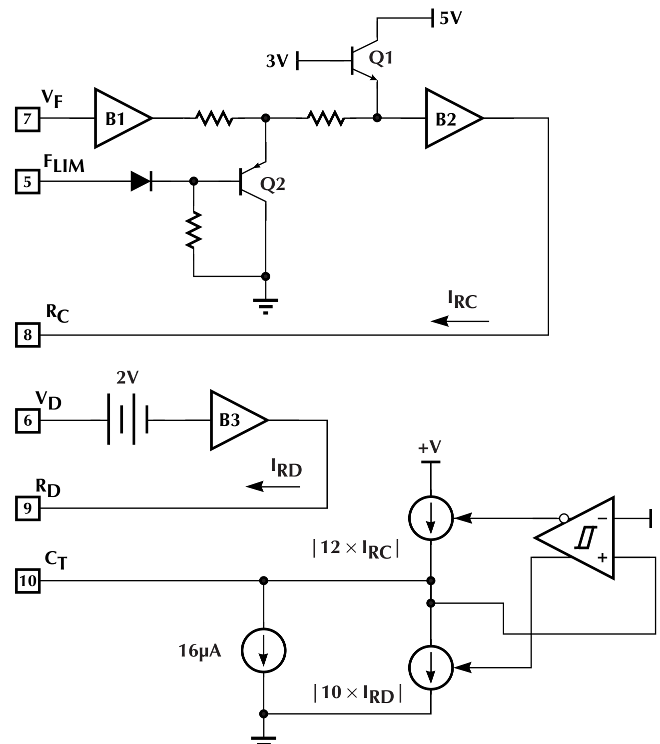


Figure 1a. Oscillator Block Diagram

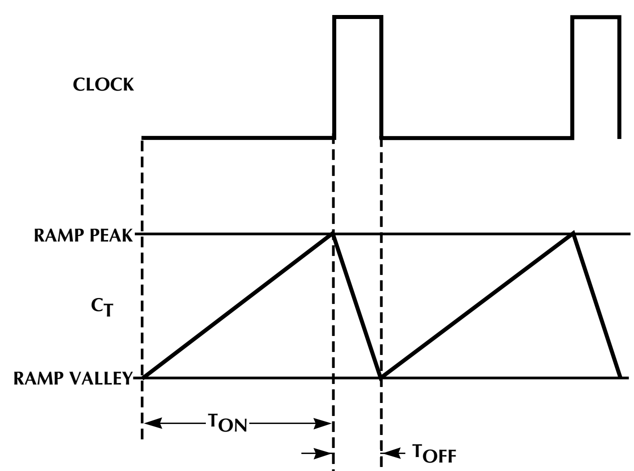


Figure 1b. Oscillator Waveform

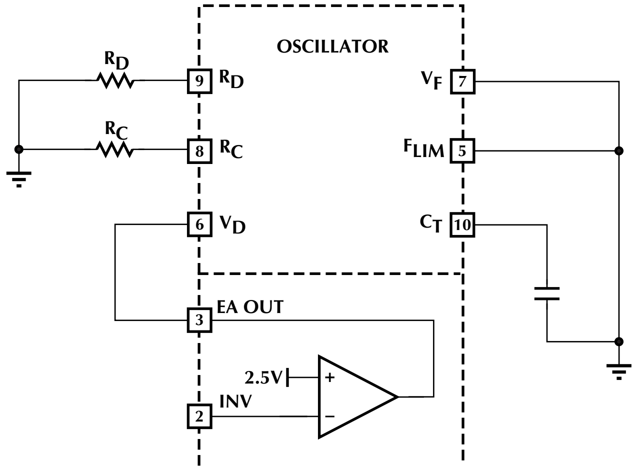


Figure 2. Variable Off Time, Constant On Time Oscillator

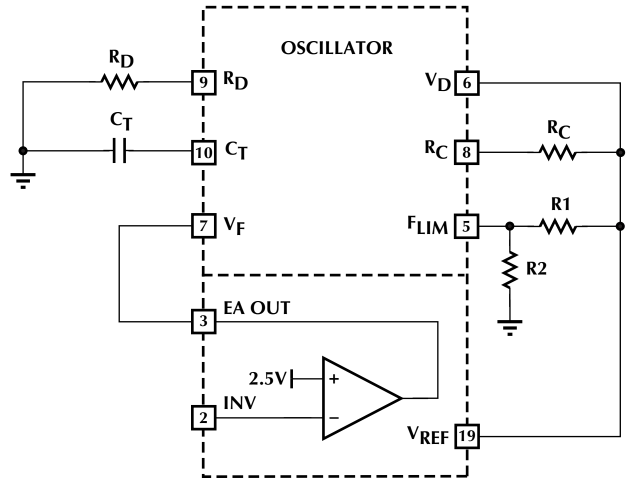


Figure 4. Variable On Time, Constant Off Time Oscillator Connections

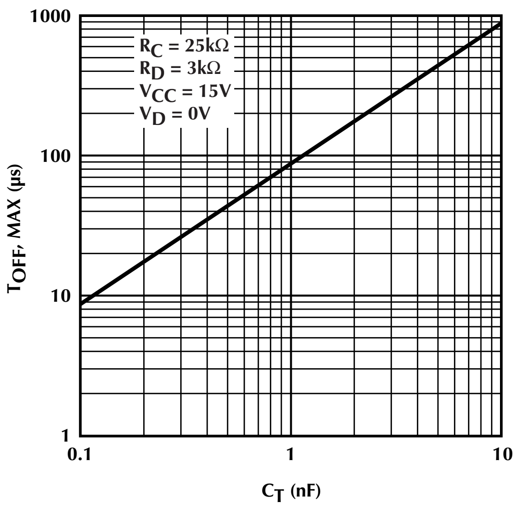


Figure 3a. Maximum Off Time as a Function of Capacitance

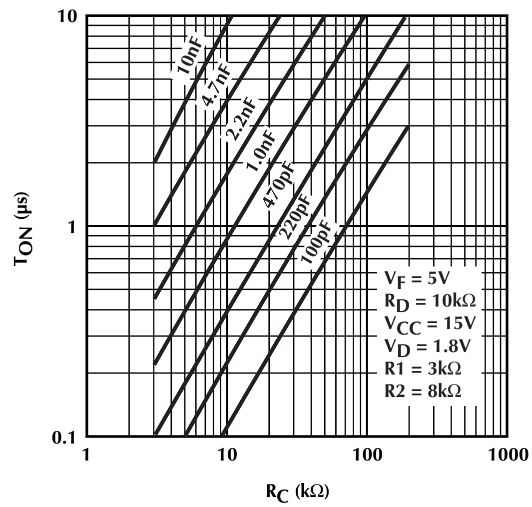


Figure 5. Minimum On Time for Constant Off Time

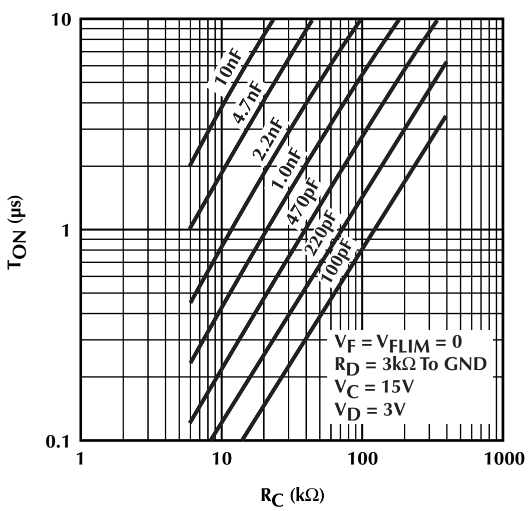


Figure 3b. On Time as a Function of Resistance

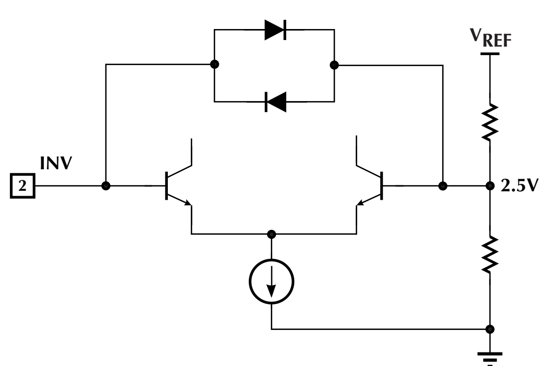


Figure 6. Error Amplifier Input

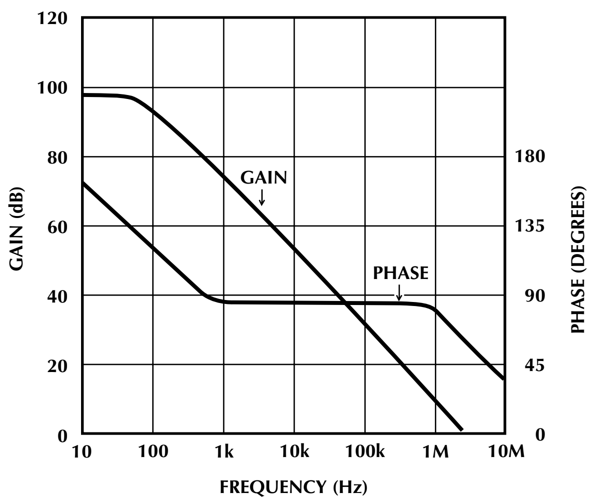


Figure 7. Error Amplifier Open Loop Gain and Phase

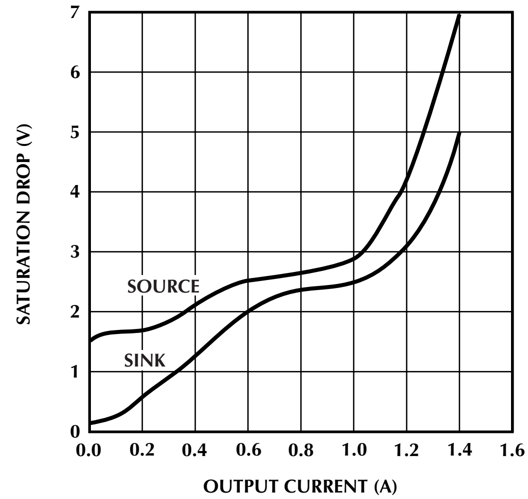


Figure 10. Output Saturation Voltage vs Current

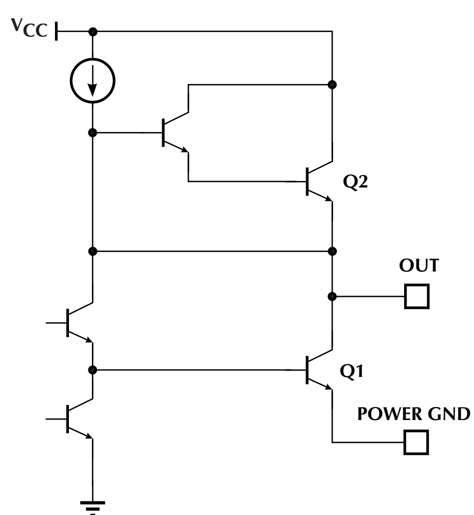


Figure 8. Power Driver Simplified Schematic

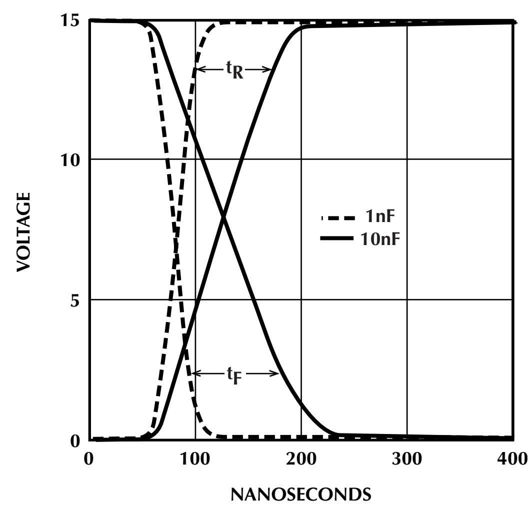


Figure 11. Rise and Fall Times

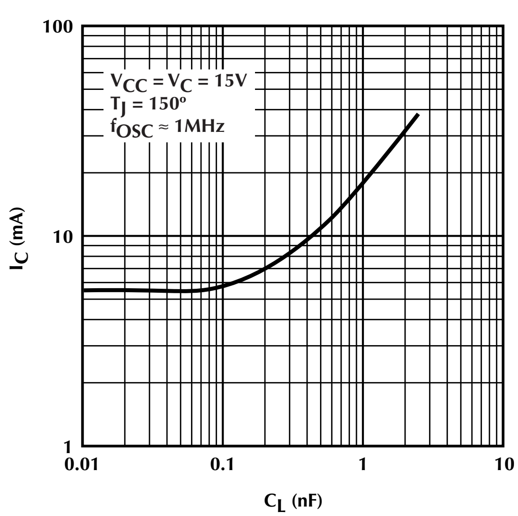


Figure 9. Output Driver Current Consumption vs Load

FUNCTIONAL DESCRIPTION (Continued)

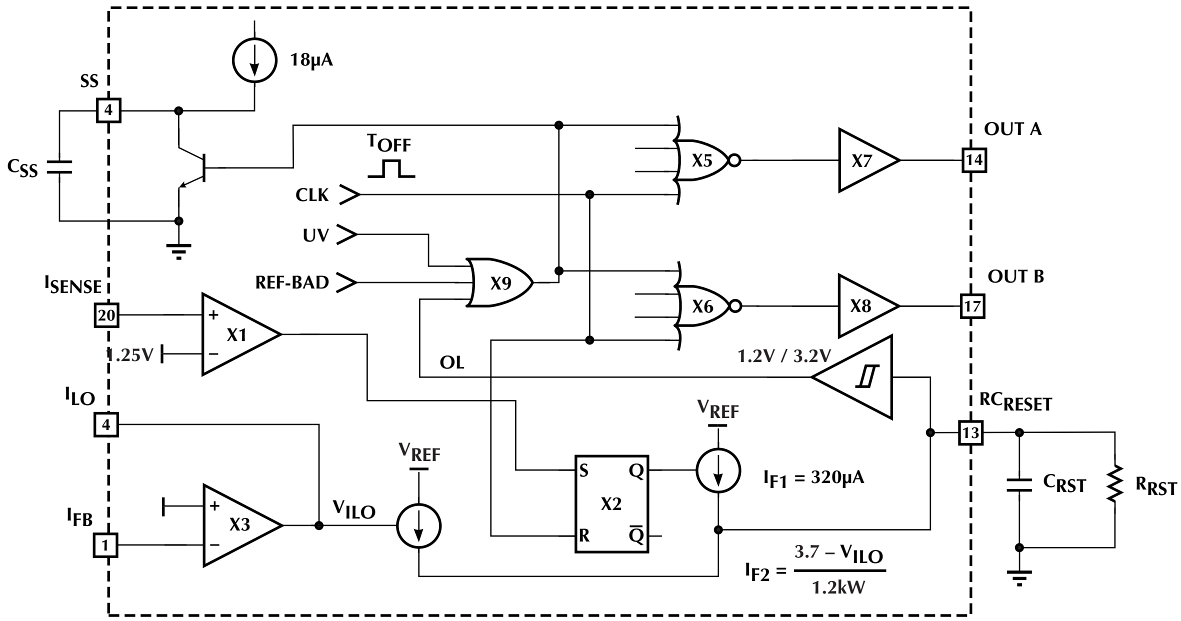


Figure 12. Overload Protection and Fault Management

ERROR AMPLIFIER

The ML4816 error amplifier is a 2.5MHz bandwidth, 8.5V/µs slew rate op amp with provision for limiting its positive output voltage swing to implement the soft start function.

The error amplifier input contains protection diodes as shown in Figure 6. Signal INV should not be driven lower than 2.5V – V_{BE} or higher than 2.5V + V_{BE}.

OUTPUT DRIVER STAGE

The ML4816 has two high current, high speed totem pole output drivers, each capable of 1.5A peak output, designed to quickly switch the gates of capacitive loads, such as power MOSFET transistors. See Figure 8.

CURRENT LIMIT, FAULT DETECTION, AND SOFT START

The ML4816 has two modes of current limiting: Primary pulse-by-pulse over current protection, and secondary DC average current limiting.

Primary Pulse-by-Pulse Current Limit Circuit

Refer to Figure 14. In this mode the primary current is compared with a 1.25V threshold in comparator X1. When the I_{SENSE} level exceeds the 1.25V threshold of comparator X1, the R-S latch at X2 is SET, turning on the 320µA current source (I_{F1}) to charge C_{RST}, and I_{F1} remains on until CLK goes high (T_{OFF}). When C_{RST} has charged to 3.2V a soft start reset occurs. The number of times the outputs reach current limit are "remembered" on C_{RST}. Over time C_{RST} is discharged by R_{RST} providing a measure of "forgetting" when the over current condition no longer occurs. If the output fault is removed before

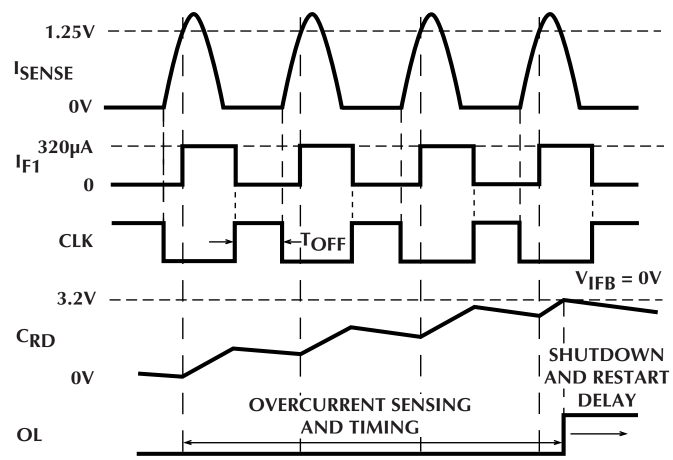


Figure 13. Over Current Sensing, Overload Shutdown, and Restart Sequence

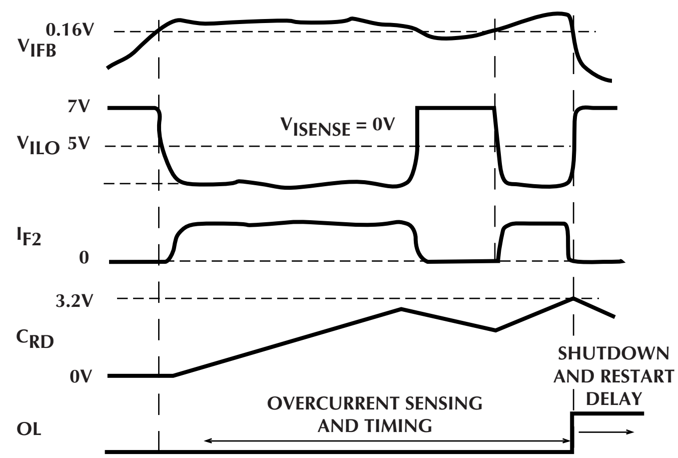


Figure 14. Secondary DC Current Sensing, Overload Shutdown, and Restart Sequence

FUNCTIONAL DESCRIPTION (Continued)

C_{RST} reaches 3.2V, C_{RST} discharges slowly through R_{RST} and normal operation resumes.

Secondary DC Current Limit Circuit

In secondary DC current limiting the currents in the output rectifiers are sensed, full wave rectified, and smoothed. The smoothed signal is fed into the current limiting amplifier X3. If the sensed current is below the 0.16V threshold the output of X3 will go above V_{REF} and I_{F2} will be off. As the sensed current exceeds the current limit threshold, V_{ILO} starts to fall and I_{F2} turns on.

$$I_{F2} \approx \frac{V_{REF} - V_{ILO} - 2V_{BE}}{1200\Omega} \quad (7)$$

I_{F2} charges C_{RST} towards the overload threshold (3.2V) of X4. C_{RST} charging and temporary recovery through R_{RST} here are similar to the pulse-by-pulse over current sensing case except that I_{F2} is continuous.

Under persistent output short circuit with either form of over current protection, C_{RST} is charged until it reaches 3.2V. The gate drives are immediately terminated and the soft start capacitor Css is discharged. C_{RST} then discharges through R_{RST} toward the restart threshold (1.2V). Gate drives remain off until C_{RST} is discharged below 1.2V. The time taken for C_{RST} to discharge to the restart threshold is the restart delay time. This delay reduces the average power delivered to the load during overload, thus protecting both the load and the controller. If overload persists the controller will continue to hiccup until the cause of the overload is removed. The controller undergoes soft start at each restart.

The overload shutdown and restart sequences for both overcurrent protection schemes with non-bootstrapped V_{CC} are illustrated in Figures 12 and 13.

For a bootstrapped converter, where controller V_{CC} is obtained from an auxiliary winding of the main transformer (see Figure 15), overload shutdown causes both the converter output and the controller V_{CC} to collapse. Undervoltage lockout (UVLO) is activated and the onchip bandgap reference is disabled. The ML4816 only dissipates 1.5mA during shutdown. Since I_{BLEED} is higher than the startup current, C_S will be charged towards the UVLO start threshold. When this happens the entire controller becomes operational, except that the gate drives remain off and I_{CC} jumps to its full operational value. Since V_{CC} bootstrapping is not yet available I_{CC} will discharge C_S below the UVLO stop threshold. The on-chip reference will again be disabled with the controller supply current reduced to 1.5mA. I_{BLEED} will again charge C_S towards the UVLO start threshold. The process repeats until C_{RST} is discharged below the restart threshold. The shutdown and restart sequence is illustrated in Figure 16.

The over current timing and shutdown sequence can be disabled by grounding the RC_{RESET} pin.

Auxiliary Output Current Limiting (RC_{RESET}) Grounded

A constant current at the power inverter output can be obtained by utilizing the current limit amplifier with RC_{RESET} shorted to ground. The I_{LO} signal is connected to the EAO signal through two external ORing diodes (Figure 17). R_1 is used as a pullup resistor. If the voltage at the inverting input I_{FB} of the current limit amplifier exceeds the 160mV threshold the current limiting loop activates and takes control, and ILO is pulled below EAO. The schematic shows that either the main error amplifier or the current limiting amplifier controls the switching frequency of the converter. The voltage to the I_{FB} pin

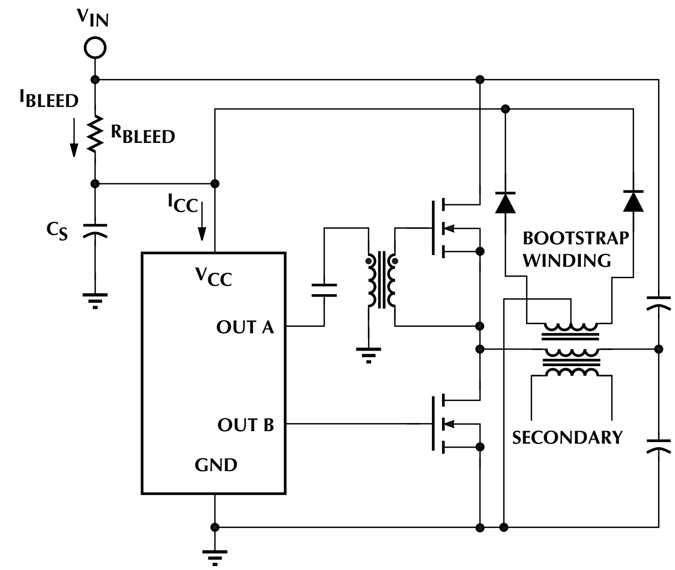


Figure 15. Simplified VCC Bootstrappuing Scheme in Half Bridge Configuration

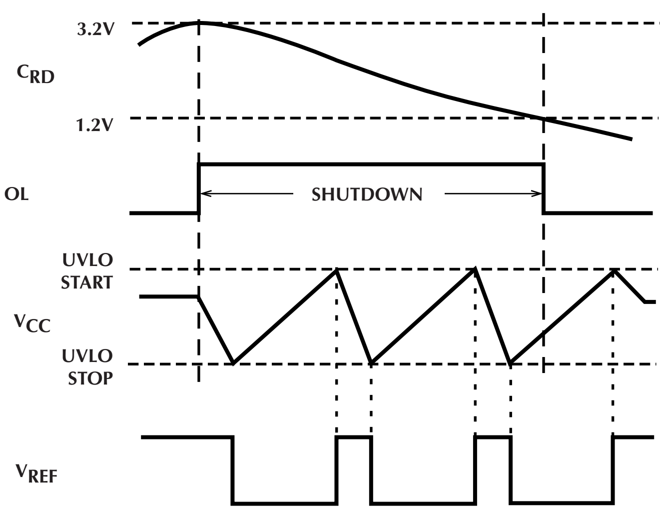


Figure 16. Overload Shutdown, UVLO, and Restart Sequence

FUNCTIONAL DESCRIPTION (Continued)

comes from the output of a current sensor which produces a signal proportional to the output current.

First Pulse Inhibit

The ML4816 features a scheme to prevent the input transformer from saturating during initial startup. The bandgap reference is disabled before V_{CC} rises above the undervoltage lockout (UVLO) start threshold. The timing capacitor C_T remains fully discharged because the bias circuit of the timer requires a reference output of at least $4V_{BE}$ to operate. See Figure 19. As V_{CC} crosses the UVLO start threshold the reference becomes enabled. The reference output rises at a rate determined by the reference short circuit current and the external bypass capacitor. C_T remains discharged until V_{REF} exceeds $4{\times}V_{BE}$. There is no gate drive until V_{REF} reaches 4.4V (the “reference good” level). Once V_{REF} exceeds $4{\times}V_{BE}$ — t_1 — C_T is charged towards the upper threshold of the oscillator/timer. Although the gate drives are enabled at t_2 the first pulse inhibit latch continues to blank the outputs. This latch is reset when C_T voltage crosses the upper oscillator threshold at t_3. OUTA is then gated on after the CLK pulse ends.

Without the first pulse inhibit circuit the first OUTA pulse would be on for time T_{ONI} which could be as much as 2 to 3 times longer than the desired T_{ON} time. The first pulse inhibit latch ensures no abnormally long first gate drive pulse, which is independent of the V_{REF} rise time.

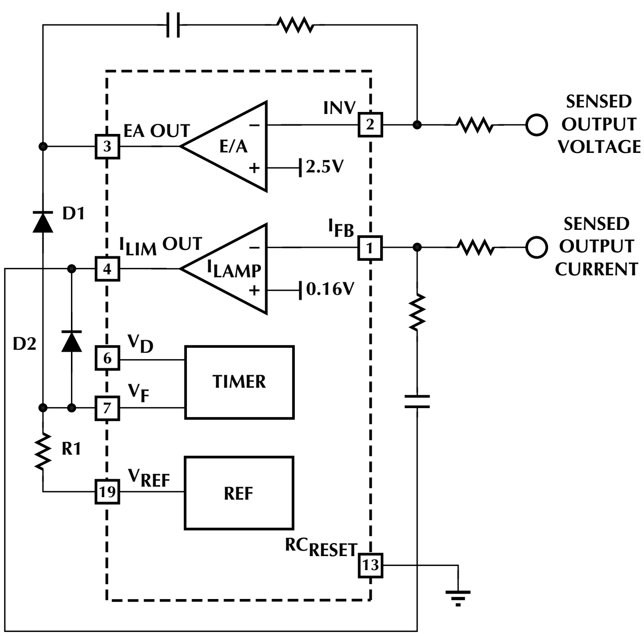


Figure 17. Auziliary Output Current Limiting

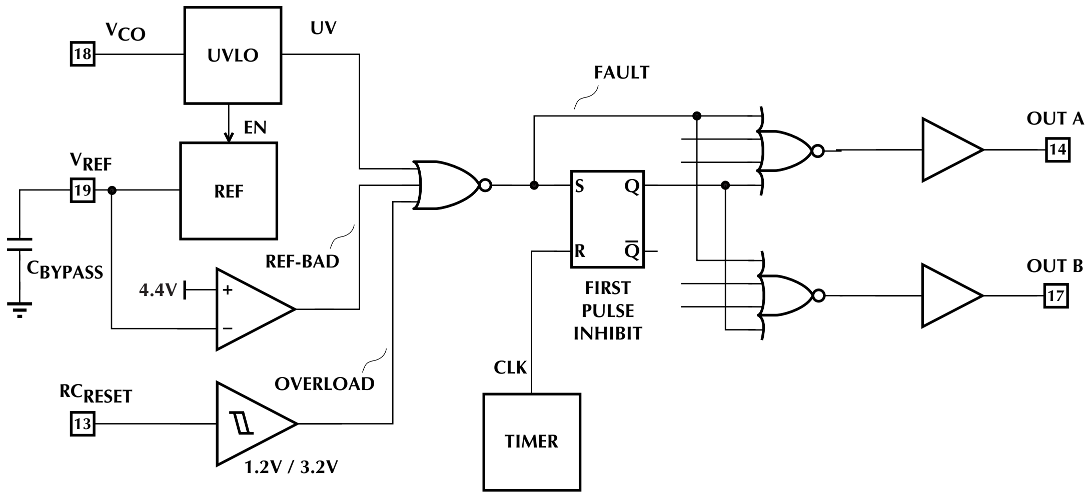


Figure 18. Operation of UVLO and the First Pulse Inhibit Circuit

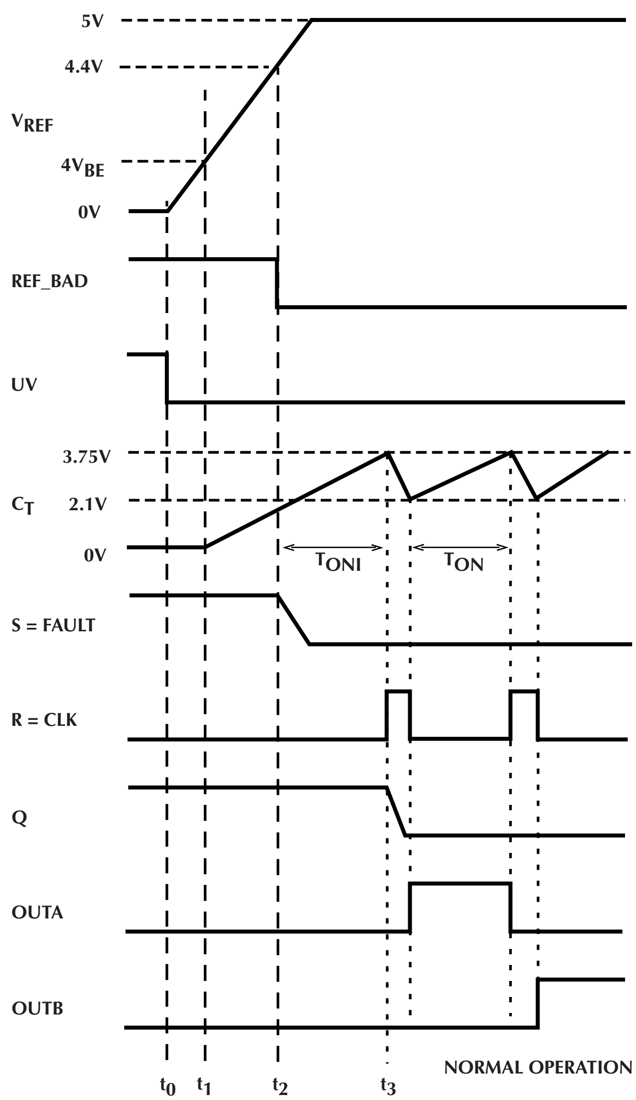


Figure 19. Initial Startup and First Pulse Inhibit

FUNCTIONAL DESCRIPTION (Continued)

TEST FIXTURE

The test fixture illustrated in Figure 20 is used with the ML4816 to exercise many of its functions and provides opportunities to measure its specifications. Careful grounding and bypass procedures should be followed since it is a wideband circuit. The use of a ground plane is highly recommended.

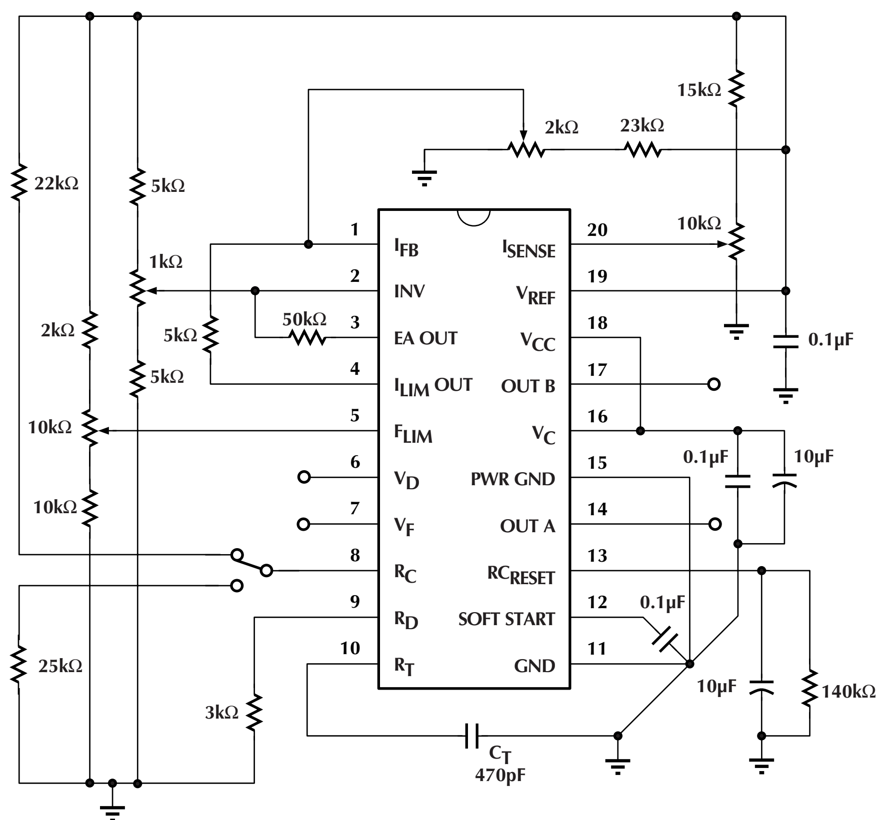
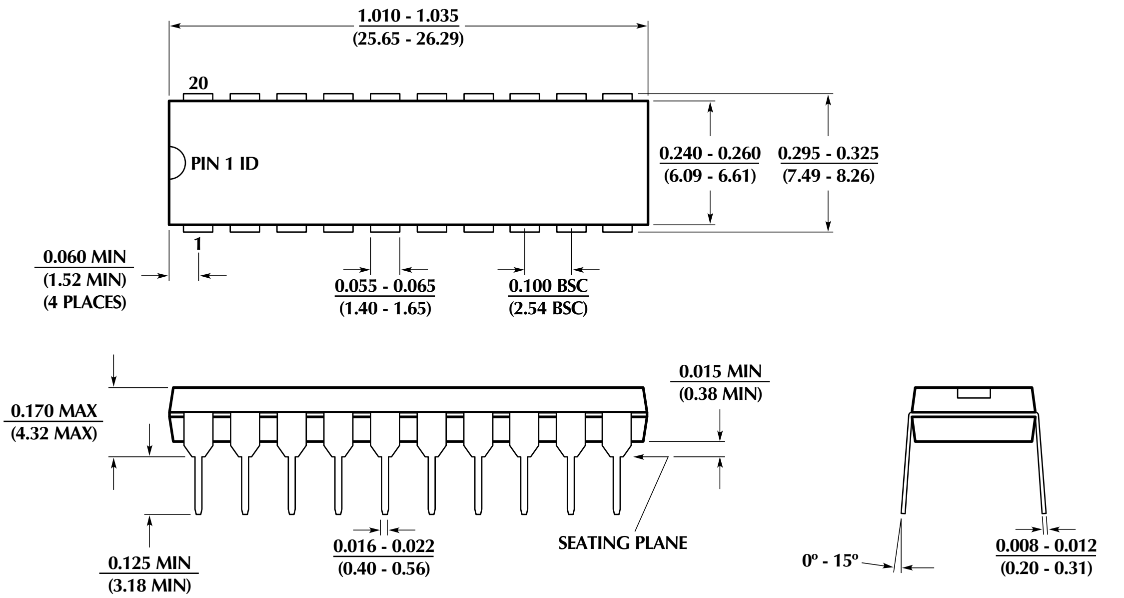


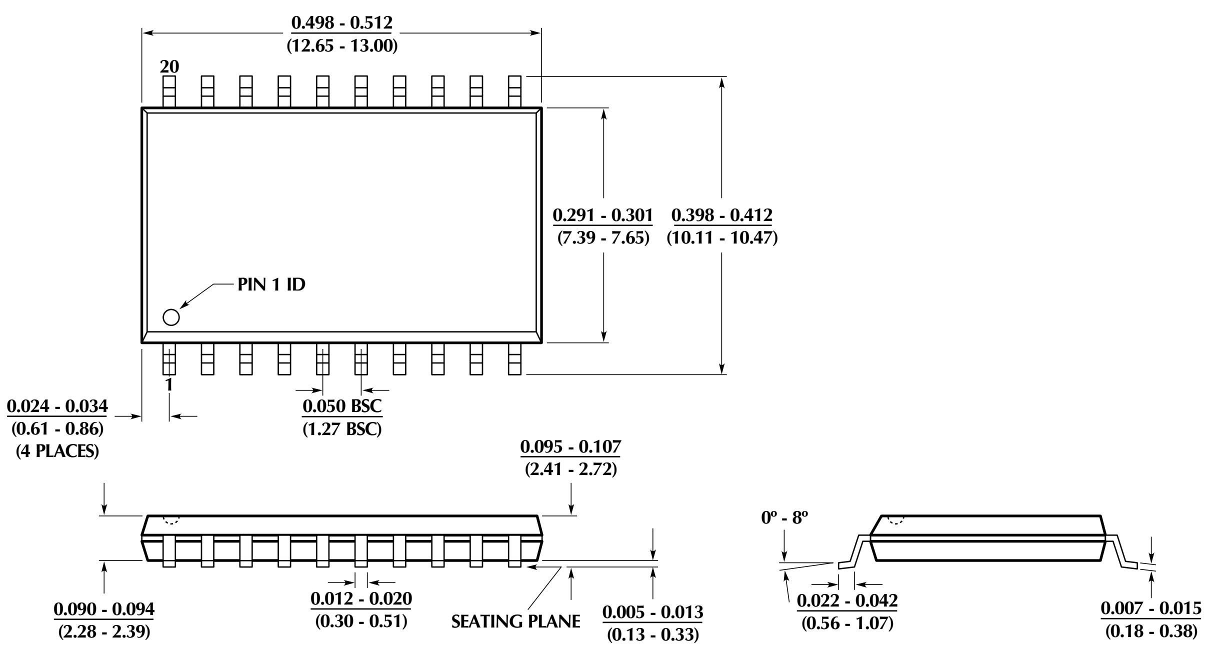
Figure 20. ML4816 Test Fixture Connections

PHYSICAL DIMENSIONS inches (millimeters)

Package: P20
20-Pin PDIP



Package: S20
20-Pin SOIC



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4816CP	0°C to 70°C	20 Pin PDIP (P20)
ML4816CS	0°C to 70°C	20 Pin SOIC (S20)

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