MHS
MATRA-HARRIS SEMICONDUCTEURS

data sheet

MA 0250-MA 0400
MA 0800-MA 1200

JANUARY 1986

3μ/1 METAL LAYER HIGH SPEED CMOS GATE ARRAYS
(UP TO 25 MHz INTERNAL OPERATING FREQUENCY)

Features

- HIGH SPEED CMOS : 2 NS/GATE TYPICAL PROPAGATION DELAY.
- LOW CONSUMPTION :
  - STAND BY CURRENT 10 nA/GATE
  - OPERATING CURRENT 5μA/GATE/MHz
- 250 TO 1200 2-INPUT GATE COMPLEXITY.
- 8 TO 68 PIN PACKAGES (PLASTIC DIL, CERDIP, LCC, PLCC).
- POWER SUPPLY RANGE : 3 TO 7 V.
- WIDE TEMPERATURE RANGE : — 55°C TO + 125°C.
- COMPLETE INPUT/OUTPUT FLEXIBILITY.
- TTL/CMOS INPUT COMPATIBILITY.
- TTL OUTPUT COMPATIBILITY : 3 TTL LOADS (OR 15 TTL/LS LOADS).
- INPUT PROTECTION NETWORK.
- EXTENSIVE LS OR HCMOS SSI/MSI FUNCTIONS LIBRARY.
- COMPLETE CAD SOFTWARE PACKAGE.
- AVAILABILITY ON CAE WORKSTATIONS :
  - DAISY SYSTEMS
  - MENTOR GRAPHICS

Description

The MA 0250-MA 0400-MA 0800-MA 1200 Gate Array product family from Matra-Harris Semiconducteurs is using "state of the art" advanced silicon gate CMOS technology. This process, called Scaled SAJI IV, features drawn channel lengths of maximum 2.5 μ and 3 μ respectively for N and P channels.

Designed for digital applications, the Matra-Harris array structure presents an internal predefined matrix organized in rows of uncommitted basic cells and interconnect routing channels, the matrix being surrounded by flexible input/output cells.

These gate arrays are used to implement combinatorial and sequential logic functions (registered in the MHS cell library) on the same chip and connect them with a unique metal layer corresponding to the user's own specific requirements.

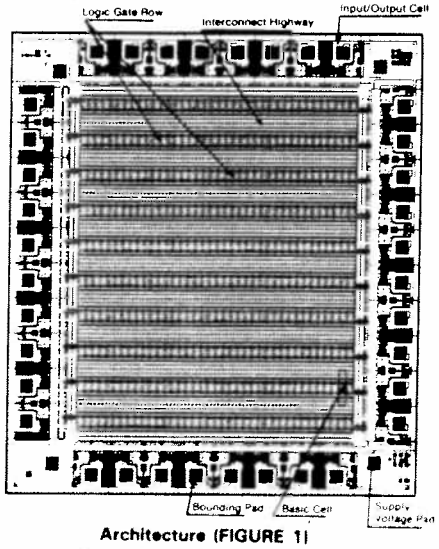
The use of MHS CAD softwares permits users to achieve this goal within a fast and reliable design cycle time.

MA 0250-MA 0400-MA 0800-MA 1200 FAMILY :

PART NUMBER	GATE COUNT	I/O PADS	INPUT/POWER PADS	TOTAL PADS	METAL LEVEL	PACKAGE PIN OPTIONS	N CHANNEL LENGTH
MA-0250	228	28	4	32	1	8 to 40	2.5 μ
MA-0400	380	36	4	40	1	8 to 44	2.5 μ
MA-0800	754	50	4	54	1	22 to 68	2.5 μ
MA-1200	1139	62	4	66	1	24 to 68	2.5 μ

NOTE : 1 gate is the equivalent of a 2 input NAND or NOR gate (It means 2 N and 2 P channel transistors).

GATE ARRAY PRODUCT DESCRIPTION :



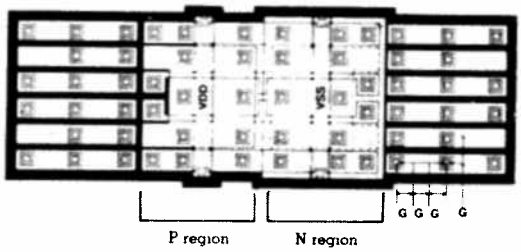
Architecture (FIGURE 1)

ARCHITECTURE

The MHS gate array structure presents as an internal matrix of uncommitted logic gates organized in rows. Each row is separated from the other by an interconnect highway area where metal channels are routed.

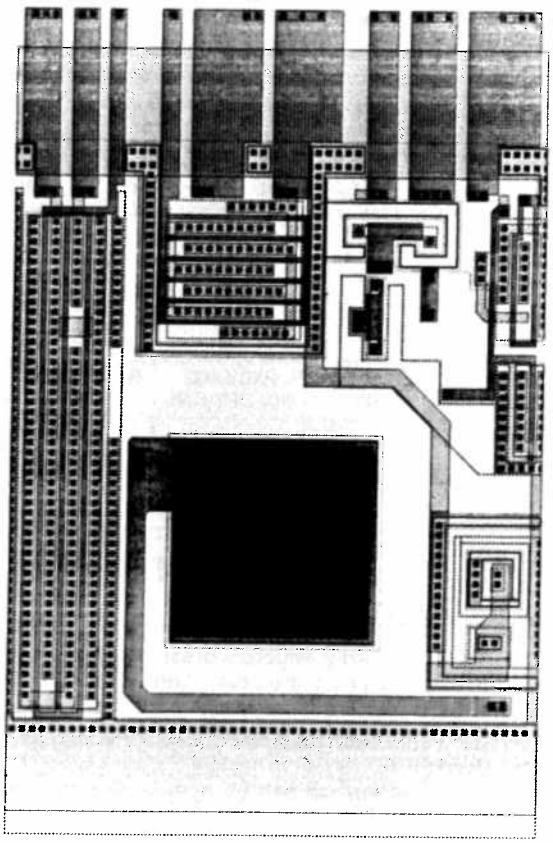
The matrix is surrounded by peripheral cells allowing the gate array to interface with external circuitry.

BASIC CELL



The basic cell (gate) consists of 2 pairs of N and P channels MOS transistors associated with 2 feed-thru in low resistivity polysilicon. An all metal supply distribution is achieved within the cell by 2 wide Aluminium lines able to support strong current surges that may be required at high frequency operation of a circuit. One contact per cell between these supply lines and the substrate and the P-well achieves a regular bias all through the matrix.

PERIPHERAL CELL



Peripheral cell (FIGURE 3)

The peripheral cell confirms the versatility of MHS array by providing an additional and total flexibility on input/output configurations.

The peripheral cell can be customized as :

- TTL input
- CMOS input
- Direct input (for Schmitt trigger input)
- Output buffer :
  All outputs are capable of driving 3 TTL or 15 LS TTL loads. Additional drive capability may be obtained by connecting output buffers in parallel (up to 30 LS TTL loads).
- Open Drain Output
- Tri-State Output
- Bidirectional input/output
- VDD or VSS Supply

Furthermore, the peripheral cell contains :

- 2 High impedance transistors which can be used as pull-up or pull-down (140 K ohm typically)
- an input protection network against parasitic phenomenons such as electrostatic damage and latch up triggering

PROCESS DESCRIPTION :

MHS High Speed CMOS Gate Arrays are constructed using the self-aligned junction isolated (Scaled SAJI IV) process

The association of a 3 microns lithography and a self aligned CMOS processing provides electrical parameters which permit the realization of fast digital circuits.

By using local oxidation to separate adjacent active regions, a high packing density of chips is achieved together with a lowering of field and side wall capacitances. Self aligned field implants are utilized to increase the field transistor threshold and to lower the N- substrate and P- well resistance which contribute to latch up behavior improvement.

MHS, SSI/MSI CELL LIBRARY :

The MA- series of arrays is supported by a complete and extended library of precharacterized and predefined SSI/MSI logic functions. The user will find in this cell library equivalent logic functions to 74 LS or 74 HC SSI/MSI standard products.

In this library any cell has its own data sheet including logic specification and diagram topological characteristics, electrical data and logic simulator reference as it can be seen on Fig. 6.

The propagation delay of each cell is given as a function of 3 parameters which are Fan Out of the cell, operating temperature, and power supply. Typical and worst cases values are given.

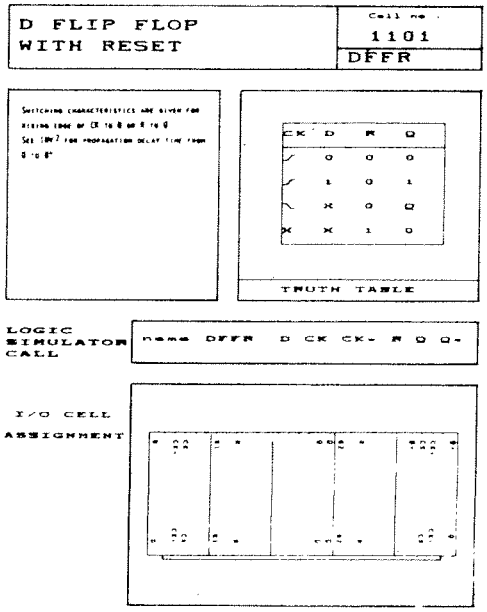
The library of internal cells provides more than 80 SSI/MSI logic functions like :

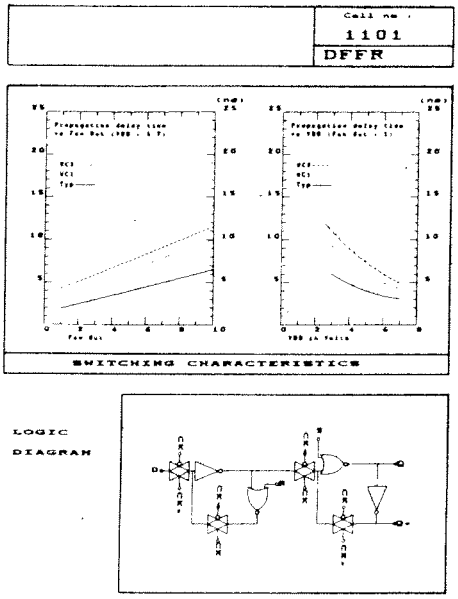
- Combinatorial logic functions
- Sequential logic functions
- MSI complex functions.

The peripheral cell library offers a wide range of interfacing external circuitry to the array :

- TTL or CMOS compatible input
- Output buffers (tri-state, open drain...)
- Bidirectionnal input/output
- Oscillator buffers (interfacing with external oscillator...) : See AN 1023 "A design guide for oscillator using MHS gate arrays".

A complete list of MHS cell library is given on Fig. 7.





Data sheet of library cell (D Flip Flop) (FIGURE 6)

MHS MACROCELL LIBRARY DESCRIPTION : (FIGURE 7)

MACROCELL	GATE EQUIVALENT
Combinatorial logic functions	
- 2 input NAND	1
- 3 input NAND	2
- 3 input NAND + 1 Inverter	2
- 4 input NAND	2
- 5 input NAND	3
- 8 input NAND	6
- 2 input NOR	1
- 3 input NOR	2
- 3 input NOR + 1 Inverter	2
- 4 input NOR	2
- 5 input NOR	4
- 8 input NOR	6
- 2 input AND	2
- 2 input AND + 1 Inverter	2
- 3 input AND	2
- 4 input AND	3
- 4 input AND + 1 Inverter	3
- 2 input OR	2
- 2 input OR + 1 Inverter	2
- 3 input OR	2
- 4 input OR	3
- 4 input OR + 1 Inverter	3
- 2 input Exclusive OR	3
- 2 input Exclusive NOR	3
- Inverter	1
- Dual Inverter	1
- Serial Inverters	1
- Power Inverter	1
- 2 input AND into 2 input OR-Invert	2
- Dual 2 input AND's into 2 input OR-Invert	3
- Dual 3 input AND's into 2 input OR-Invert	3
- Dual 4 input AND's into 2 input OR-Invert	4
- 2 input OR/AND into 2 input OR-Invert	2
- Dual 2 input OR's into 2 input AND-Invert	2
- Dual 3 input OR's into 2 input AND-Invert	3
- 2 input OR into 2 input AND into 2 input OR-Invert	2
- 2 input OR/3 input OR/4 input OR into 4 input AND-Invert	5
- 2 input AND into 2 input OR/ 2 input OR into 2 input AND-Invert	3
- 1 bit full adder with carry	7
- 1 bit full adder with fast carry path	9
- 1 bit simple adder	4
Sequential Logic Functions	
- Latch	2
- Latch with R (reset)	3
- Latch with $\underline{S}$ (set)	3
- Latch with $\overline{R}$	3
- Latch with $\overline{S}$	3
- D Flip Flop	4
- D Flip Flop with R (reset)	5
- D Flip Flop with $\underline{S}$ (set)	5
- D Flip Flop with $\overline{R}$	5
- D Flip Flop with $\overline{S}$	5
- D Flip Flop with R and $\underline{S}$	6
- D Flip Flop with $\overline{R}$ and $\overline{S}$	6
- D Flip Flop with 1 clock	5
- JK Flip Flop	7
- JK Flip Flop with R (reset)	8
- JK Flip Flop with $\underline{S}$ (set)	8
- JK Flip Flop with $\overline{R}$	8
- JK Flip Flop with $\overline{S}$	8
- JK Flip Flop with $\underline{S}$ and R	9
- JK Flip Flop with $\overline{S}$ and $\overline{R}$	9
- RS Flip Flop with NAND	2
- RS Flip Flop with NOR	2

MACROCELL	GATE EQUIVALENT
Sequential Logic Functions (cont'd)	
- Toggle Flip Flop with asynchronous parallel load	12
Interface and Special Functions	
- TTL compatible Schmitt Trigger	6
- CMOS compatible Schmitt Trigger	2
- Enable command for 3 state Output Buffer	5
- Retriggerable resetable Monostable (with external RC)	10
- Transfer Gate	1
- Bidirectional 2-1 (de-) multiplexer	1
- Inverting 3 state internal bus driver	2
- Non-inverting 3 state internal bus driver	3

MACROCELL	GATE EQUIVALENT
MSI functions	
- 4 bit full adder (4008)	68
- 4 bit static shift register (4015) (serial input/parallel output)	24
- 4 bit static shift register (4035) (parallel input/parallel output)	46
- 14 bit binary counter (4020)	75
- Decode counter/divider (4017) (+ 10 decoded decimal outputs)	54
- 4 bit binary counter (4163) (with synchronous clear)	56
- Binary up/down counter (4516)	76
- Binary up counter (4520)	30
- Binary to 1-of-4 decoder (4556)(Inverting)	8
- 4 bit magnitude comparator (4585)	30

MHS CAD SOFTWARE SUPPORT :

MHS developed a complete CAD Software package in order to insure a fast and efficient gate array development with minimal risks.

MHS CAD Softwares provide :

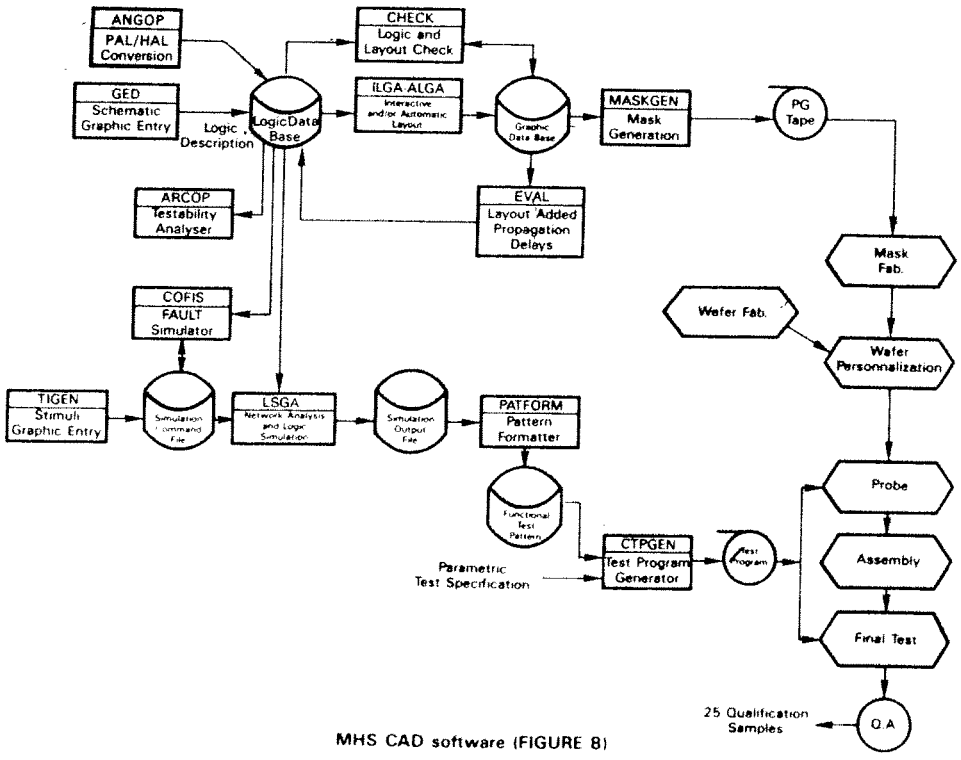
- A way for a system, rather than a circuit, designer to integrate his logic circuit into silicon
- A full continuity between the different design steps from logic architecture description to chip testing
- A circuit development without breadboard realization, thanks to a logic simulation using realistic propagation delays. It has been made possible by a precise, but user's transparent, modelization of the device and network behaviour
- Documentation aids (schematic, simulation results, symbolic lay out, mask plots).

MHS CAD Softwares use 2 common data bases :

- A logic data base containing the complete description of customer circuit. Used as reference file. Most of the programs access this data base allowing to issue a logic simulation fitting with the physical reality and to generate a test program
- A Graphic Data Base containing the lay-out in symbolic form is generated by interactive and/or automatic placement and routing program. Software use this file to make correspondences :
  - from Graphic symbolic to logic
  - from Graphic symbolic to mask

MHS CAD SOFTWARE SUPPORT :

MHS available software are presented in Fig. 8.



MHS CAD software (FIGURE 8)

Above development flow shows very clearly the different steps in a gate array design. Two parallel ways with interactive links are taken in order to achieve a full gate array design : Lay-out and Test. The finalization of such a design is the issue of :

- a PG tape for mask tooling
- a Test Program magnetic tape for probe and Final Test of the silicon.

The heart of this Gate Array development flow is the logic data base.

MHS CAD SOFTWARE SUPPORT:

GED : Graphic Editor :
Provides a graphic entry of logic schematic. Outputs are a connection list and plots for production documents.

LSGA : Logic Simulator for Gate Arrays :
In addition to normal possibilities of a modern interactive or batch mode logic simulator working with 12 logic states (i.e, timing control and spikes detection) it offers some extra features :
- a unit delay (pseudo functional) simulation mode
- a network analyser and operating conditions scaler calculating separate rise and fall propagation delay times
- a test option verifying toggle ; it assures that all nodes in the network have been exercised
- a logic analyser output (WAVE) permitting to analyse the functionality of the circuit and by changing the sampling period to check propagation delay times.

ARCOP : Testability Evaluation Program :
It's a controllability/observability program, allowing users to improve testability of the circuit.

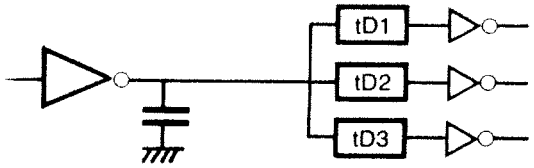
COFIS : Fault Simulator :
Is a concurrent Fault simulator using tables generated from the logic description to perform a single stuck-at fault generation and fault analysis and produce a full detection report.

ILGA : Interactive Placement and Routing :
Is a graphic editor providing easy way to place and move the cells, to route metal interconnect channels. Routing task is facilitated because special symbols indicate I/O in the current connection. Partial or total symbolic plots of the circuit can be drawn for documentation use.

CHECK : Lay-Out and Design Rule Checker :
Is ILGA's complement. It checks correspondence between logic description and lay-out and detects design rules violations. Intermediate checking capabilities limits the risk of serious mistakes and ensures a good final lay-out.

ALGA : Automatic Placement and Routing :
Automatic Placement and Routing in 1 level of interconnect is automatically performed. ILGA is therefore useful to preplace cells (pads for instance), to check the lay-out and to route some possible unrouted connections. 80 % silicon use is normally expected with fully automatic routing.

EVAL : EVAL is computing the delays of the interconnect nets from the topology of the network after performing layout. Delays are based on resistance as well as capacitance of the interconnection nets. The EVAL software is making an accurate computation of delays : EVAL is taking into account the branches of the net. EVAL is bringing back the total net capacitance to the output of the driving cell and is reporting an extra delay to the input of the driven cells (see fig. 9).



RC delay extraction example (FIGURE 9)

After the RC delay information is extracted, these delays are inserted into the network data base for post-layout ARCIS simulation and then critical path analysis, thus providing an excellent tool for first silicon success.

PATFORM: Test Pattern Formatter :
Logic simulation output file is the basis of functional testing which is made on Sentry test equipment. PATFORM is an intelligent translater generating and compacting bit patterns and inserting logical mask to prevent erroneous sampling.

CTPGEN : Conversational Test Program Generator ;
Is an editor permitting easy construction of test program by assembling the functional test generated by PATFORM to other modules for DC and AC standard parametric test measurements.

All these programs are running on VAX 11/8600 DEC computer using Tektronix Graphic Terminals (41XX series).

HAL SUPPORT (ANGOP) :

As 74LS/7400/4000/74HC series SSI/MSI functions can be implemented on MHS gate array chip, it is possible to concert PAL/FPLA design to gate arrays.

The MA0250 is well suited for these HAL (Hard Array Logic) applications : the HAL is for PAL, what the ROM is for PROM.

ANGOP software will perform the direct translation from boolean expression to logic data base and then to final HAL product.

* *Trademarks : PAL is a trademark of Monolithic Memories Incorporated.*

MHS/CUSTOMER INTERFACE : MHS DESIGN APPROACHES :

In order to give customer an easy access to CAD facilities, MHS offers a broad range of Design approach solutions. Each approach offered by MHS is well suited to customer needs according to customer CAD design resources, CAD design know how, CAD equipment facilities.

MHS proposes :

1) for customers willing to design their circuit themselves.
   - remote mode access to Nantes CAD center via modem phone line (1200/2400 BPS) and/or specialized data transmission network (9600 BPS).
   - local mode capabilities by transfering to customer, having its own CAD center, the graphic data base and softwares
   - Local mode design by using stand alone CAE workstations (Daisy Systems, Mentor Graphics, Valid).
   - MHS Regional Design Centers where customer will find equipment and technical support.
2) For customers willing to sub-contract the design of their circuit
   - MHS local design resources capabilities in Nantes CAD Center and Regional Design Centers
   - Qualified Distributors having in house technical expertise.

The Fig.10 summarizes the MHS Design Approaches

DESIGN APPROACHES	OPTIONS	AVAILABILITY DATE	EQUIPMENT NEEDED AT CTM LOCATION	DEVELOPMENT CHARGES
Design done by customer on remote mode - Modem phone line (1200-2400 BPS) - Data transmission network (4800-9600 BPS)	At customer location	Available	• TEKTRONIX graphic terminal • Modem	• Training course • CAD development • Test
	At MHS plant (direct access) - 4113A/4014/4114 4115/4109 graphic terminal - Work station	Available	None	• Training course • CAD development • Test • Tektronix rental
	At MHS regional office - 4113 A graphic terminal - Work station	See Gate Center list	None	• Training course • CAD development • Test • Telephone line rental • Tektronix rental
Design done by customer on local mode	By using Stand alone CAE Work stations	Daisy: SIMULATION Avail., LAYOUT Avail. Mentor: SIMULATION Avail. Valid: SIMULATION Avail.	• Stand alone CAE work station	• Training course • Handling + mask charges • Test
	By using his own CAD softwares	Available	• Computer • Graphic system (calma preferable)	• Gate array matrix + cell library transfer • Handling + mask charges
	By using MHS CAD softwares	Available	• VAX 11 computer • Tektronix graphic terminal	• Training course • Gate array matrix + cell library transfer • CAD software transfer • Handling + mask charges • Test
Design done by	MHS	Available	None	• CAD development • Engineering charges • Test
	MHS representative : - Design House - Distributor	Available (see Distributors List)	None	• Representative charges

MHS Gate Array Design Approaches (FIGURE 10)

HIGH SPEED CMOS GATE ARRAY CHARACTERISTICS :

ABSOLUTE MAXIMUM RATINGS :

PARAMETER	SYMBOL	LIMITS	UNIT
DC Supply Voltage	VDD	− 0.5 to + 7	Volt
Input/Output Voltage	V_{IN}/V_{OUT}	− 0.5 to VDD + 0.5	Volt
Input Current	I_{IN}	± 10	mA
Storage Temperature	T_{stg}	− 65 to + 150	°C

RECOMMENDED OPERATING CONDITIONS :

PARAMETER	SYMBOL	LIMITS	UNIT
DC Supply Voltage	VDD	3 to 6	Volt
Input/Output Voltage	V_{IN}/V_{OUT}	0 to VDD	Volt
Operating Temperature Range	Military (− 2) Mil 883B (− 8) Industrial (− 9) Commercial (− 5)	− 55 to + 125 − 55 to + 125 − 40 to + 85 0 to + 70	°C

DC ELECTRICAL CHARACTERISTICS :

(Specified at VDD = 5 V ± 10 % and all temperature ranges unless otherwise notified)

PARAMETER	MIN	TYP*	MAX	UNIT	CONDITIONS
Low Level Input Voltage VIL CMOS (BUFIN MOS) VIL TTL (BUFIN TTL)			 1.5 0.8	 V V	
High Level Input Voltage VIH CMOS (BUFIN MOS) VIH TTL (BUFIN TTL)	 3.5 2 2.2			 V V V	 (0/+ 70° C) (− 40/+85° C)(− 55/+125° C)
Low Level Output Voltage VOL (BUFOUT)			0.4	V	IOL = − 3.2 mA
High Level Output Voltage VOH (BUFOUT)	3.9			V	IOH = 100 µA
High Level Output Voltage VOH (BUFOUT)	2.4			V	IOH = 5 mA
Input Leakage Current IIL, IIH (without pull-up)	 − 1 − 3 − 5		 + 1 + 3 + 5	 µA	VIN = VDD or 0 V 0° C to + 70° C − 40° C to + 85° C − 55° C to + 125° C
3 State Output Leakage current IOZ	 − 1 − 3 − 5		 + 1 + 3 + 5	 µA	VIN = VDD or 0 V 0° C to + 70° C − 40° C to + 85° C − 55° C to + 125° C
Output Short Circuit Current IOS (BUFOUT) (1)	25 − 20		80 − 75	mA	VDD = Max, VOUT = VDD VDD = Max, VOUT = 0V
Standby Current IDDSB		10		nA/gate	VIN = VDD or VSS
Operating Current IDDOP		5		µA/gate /MHz	VIN = VDD or VSS

** Typical values are given at VDD = 5V, TA = 25° C.*

Note (1) : Not more than one output may be shorted at a time for a maximum duration of one second.

AC ELECTRICAL CHARACTERISTICS :

(Specified at VDD = + 5 V)

PARAMETER		0° C to + 70° C		- 40° C to + 85° C		- 55° C to + 125° C		UNIT
		TYP	MAX		MAX		MAX	
Inverter Propagation Delay tp	(1)(2)	1.3	3		3.5		4	ns
2 input NAND Prop. Delay tp (NAND2)	(1)(2)	1.8	4		4.5		5	ns
2 input NOR Prop. Delay tp (NOR2)	(1)(2)	2.1	5.5		6		7	ns
4 input NAND Prop. Delay tp (NAND2)	(1)(2)	1.9	4.5		5		6	ns
4 input NOR Prop. Delay tp (NOR4)	(1)(2)	4	10		10.5		11	ns
D Flip Flop with R Prop. Delay tp (DFFR*)	(1)(2)(3)	4	12		13.5		16	ns
CMOS compatible input buffer Prop. Delay tp (BUFIN MOS)	(1)(2)	2.2	7		7.5		9	ns
TTL compatible input buffer Prop. Delay tp (BUFIN TTL)	(1)(2)	2.2	7		7.5		9	ns
Output Buffer Prop. Delay tp (BUFOUT)	(1)(4)	13	20		22		25	ns
Output Buffer Rise Time (10 % - 90 %) tr (BUFOUT)	(4)	18	25		27		32	ns
Output Buffer Fall Time (90 % - 10 %) tf (BUFOUT)	(4)	15	20		22.5		28	ns

AC TEST CONDITIONS :

(1) All propagation delay times are average values between input signal and output signal.

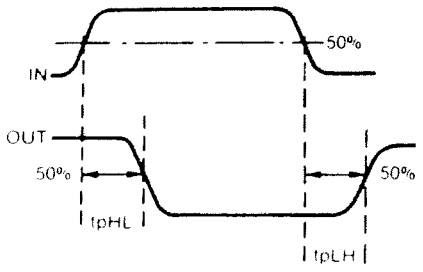
Propagation delay values given in this table are average values between tpLH and tpHL.

$$tp = \frac{tpLH + tpHL}{2}$$

Signal levels are

VIL = 0 Volt

VIH = VDD (except VIH = 3 V for TTL input buffer).



(2) Propagation delays of internal cells and input buffers are given under following conditions :

Fan out = 2 + 500 μm metal interconnect + 480 μm of polysilicon.

(3) D Flip Flop (with R) propagation delay is corresponding to propagation delay between clock (CK) and output (Q)

(4) BUFOUT cell test conditions are :
Load Capacitance CL = 50 pF

PACKAGING :

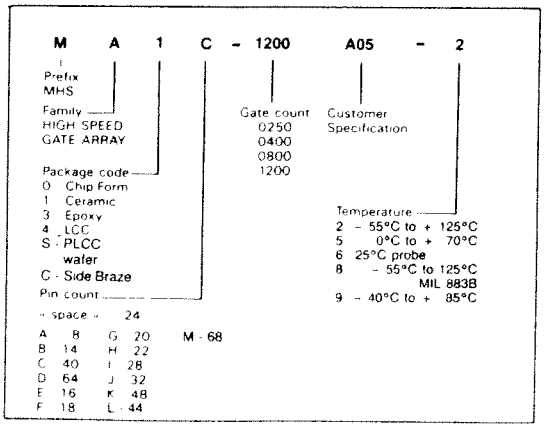
MHS High speed CMOS gate arrays package options

PACKAGE TYPE	LEAD COUNT	MA 0250	MA 0400	MA 0800	MA 1200
Plastic DIL	8	X	X		
	14	X	X		
	16	X	X		
	18	X	X		
	20	X	X		
	22	X	X		
	24	X	X	X	X
	28	X	X	X	X
	40	X	X	X	X
	48			X	X
Ceramic DIL	16	X	X		
	18	X	X		
	20	X	X		
	22	X	X	X	
	24	X	X	X	X
	28	X	X	X	X
	40	X	X	X	X
	48 (side brazed)			X	X
	64 (side (brazed)				X
Ceramic LCC	28	X	X		
	32	X	X	X	
	40		X	X	X
	44		X	X	X
	48			X	X
	64			X	X
	68			X	X
Plastic LCC	38	X	X	X	
	44	X	X	X	X
	68			X	X
Quad. pack	68			X	X

A wide variety of packages is offered for the 1 metal layer MHS gate array product family. Other packages may be available on customer request after MHS approval.

MHS can also deliver gate array products in dice or wafer form.

PRODUCT DEFINITION :



HIGH SPEED CMOS EVALUATION TEST VEHICLE :

The MA1D-1200A00 is the test vehicle of the 1 metal layer MHS array family. It has been specifically patterned in order to evaluate AC and DC characteristics of these products.

The main patterns implemented on this chip are :

- Input/Output Buffers
- Transfer Gate
- Ring Oscillator
- Frequency Divider by 8
- 4 bit Shifter
- 120 Bit Static Shift Register

This test vehicle is available in small sample quantities.

A data log is delivered with the samples.