National Semiconductor

January 2006

LM101AQML Operational Amplifiers

General Description

The LM101A is a general purpose operational amplifier which features improved performance over industry standards such as the LM709. Advanced processing techniques make possible an order of magnitude reduction in input currents, and a redesign of the biasing circuitry reduces the temperature drift of input current. Improved specifications include:

- Offset voltage 3 mV maximum over temperature
- Input current 100 nA maximum over temperature
- Offset current 20 nA maximum over temperature
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10V/μs as a summing amplifier

  This amplifier offers many features which make its application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, and freedom from oscillations and compensation with a single 30 pF capacitor. It has advantages over internally compensated amplifiers in that the frequency compensation can be tailored to the particular application. For example, in low frequency circuits it can be overcompensated for increased stability margin. Or the compensation can be optimized to give more than a factor of ten improvement in high frequency performance for most applications.

  In addition, the device provides better accuracy and lower noise in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and a drift at a lower cost.

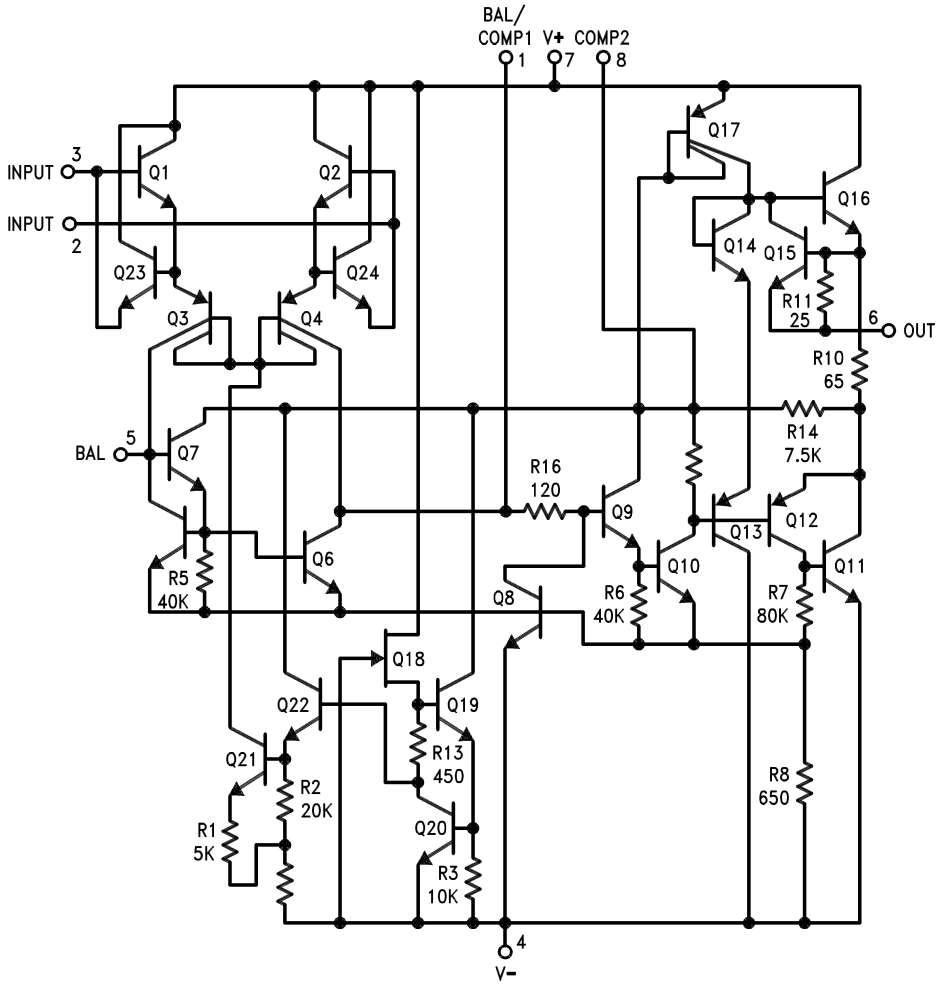
Features

- Available with radiation guarantee
- Offset voltage 3 mV maximum over temperature
- Input current 100 nA maximum over temperature
- Offset current 20 nA maximum over temperature
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10 V/μS as a summing amplifier

Ordering Information

NS Part Number	SMD Part Number	NS Package Number	Package Description
LM101AH/883		H08C	8LD Metal Can
LM101AJ/883		J08A	8LD CERDIP
LM101AW/883		W10A	10LD CERPACK
LM101AH-QMLV	5962–9951501VGA	H08C	8LD Metal Can
LM101AHLQMLV	5962L9951501VGA 50k rd(Si)	H08C	8LD Metal Can
LM101AHRQMLV	5962R9951501VGA 100k rd(Si)	H08C	8LD Metal Can
LM101AJLQMLV	5962L9951501VPA 50k rd(Si)	J08A	8LD CERDIP
LM101AJ-QMLV	5962–9951501VPA	J08A	8LD CERDIP
LM101AW-QMLV	5962–9951501VHA	W10A	10LD CERPACK
LM101AWLQMLV	5962L9951501VHA 50k rd(Si)	W10A	10LD CERPACK

Schematic (Note 11)



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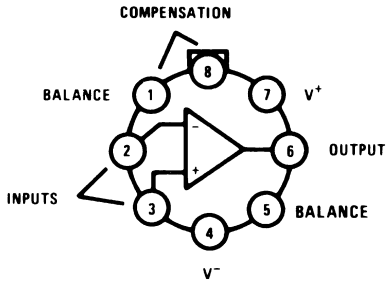
Connection Diagrams

(Top View)
Metal Can Package



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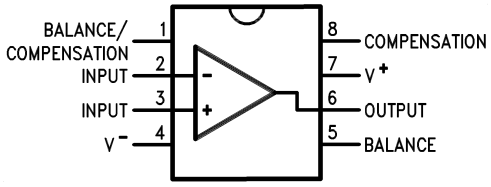
See NS Package Number H08C
Note: Pin 4 connected to case.

(Top View)
Dual-In-Line Package



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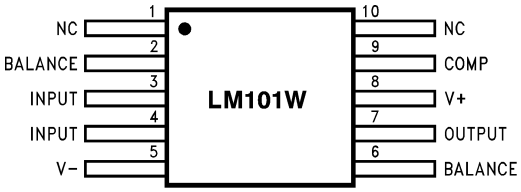
See NS Package Number J08A

Connection Diagrams (Continued)

(Top View)
Ceramic Flatpack Package



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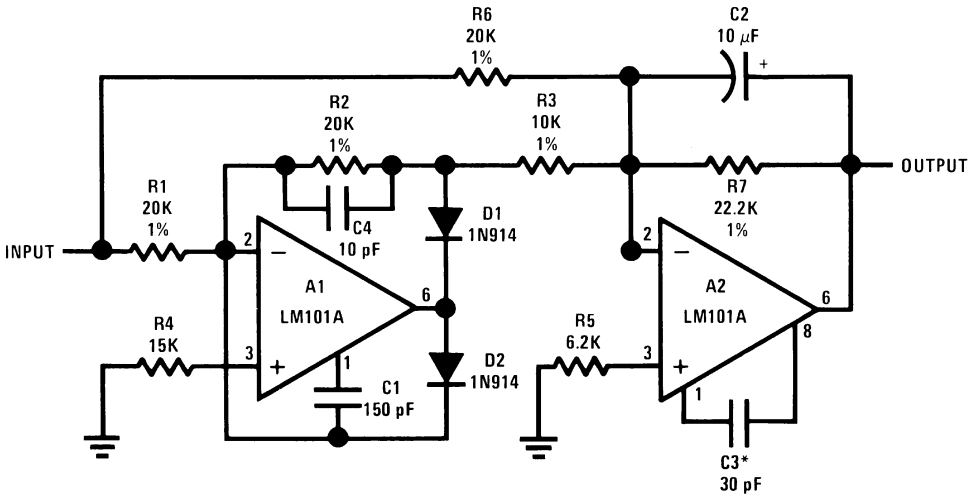
See NS Package Number W10A

Fast AC/DC Converter



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Note 1: Feedforward compensation can be used to make a fast full wave rectifier without a filter.

Absolute Maximum Ratings (Note 2)

Supply Voltage	±22V
Differential Input Voltage	±30V
Input Voltage (Note 3)	±15V
Output Short Circuit Duration	Continuous
Operating Ambient Temp. Range	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$
T_J Max	150˚C
Power Dissipation at $T_A = 25^{\circ}C$ (Note 4)	
H-Package	
(Still Air)	750 mW
(500 LF / Min Air Flow)	1200 mW
J-Package	
(Still Air)	1000 mW
(500 LF / Min Air Flow)	1500 mW
W-Package	
(Still Air)	500mW
(500 LF / Min Air Flow)	800mW
Thermal Resistance	
θ_{JA}	
H-Package	
(Still Air)	165˚C/W
(500 LF / Min Air Flow)	89˚C/W
J-Package	
(Still Air)	128˚C/W
(500 LF / Min Air Flow)	75˚C/W
W-Package	
(Still Air)	233˚C/W
(500 LF / Min Air Flow)	155˚C/W
θ_{JC} (Typical)	
H-Package	39˚C/W
J-Package	26˚C/W
W-Package	26˚C/W
Storage Temperature Range	$-65^{\circ}C \leq T_A \leq +150^{\circ}C$
Lead Temperature (Soldering, 10 sec.)	300˚C
ESD Tolerance (Note 5)	3000V

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55

LM101A 883 Electrical Characteristics

DC Parameters

The following conditions apply to all parameters, unless otherwise specified

V_{CC} = ±20V, V_{CM}= 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage	V_{CM} = -15V, R_S = 50Ω		-2.0	2.0	mV	1
				-3.0	3.0	mV	2, 3
		V_{CM} = 15V, R_S = 50Ω		-2.0	2.0	mV	1
				-3.0	3.0	mV	2, 3
		R_S = 50Ω		-2.0	2.0	mV	1
				-3.0	3.0	mV	2, 3
		V_{CC} = ±5V, R_S = 50Ω		-2.0	2.0	mV	1
				-3.0	3.0	mV	2, 3
I_{IO}	Input Offset Current	V_{CM} = -15V		-10	10	nA	1
				-20	20	nA	2, 3
		V_{CM} = 15V		-10	10	nA	1
				-20	20	nA	2, 3
				-10	10	nA	1
				-20	20	nA	2, 3
		V_{CC} = ±5V		-10	10	nA	1
				-20	20	nA	2, 3
$±I_{IB}$	Input Bias Current	V_{CM} = -15V		1.0	75	nA	1
				1.0	100	nA	2, 3
		V_{CM} = 15V		1.0	75	nA	1
				1.0	100	nA	2, 3
				1.0	75	nA	1
				1.0	100	nA	2, 3
		V_{CC} = ±5V		1.0	75	nA	1
				1.0	100	nA	2, 3
PSRR+	Power Supply Rejection Ratio	+V_{CC} = +20V and +5V, -V_{CC}=-20V, R_S=50Ω		80		dB	1, 2, 3
PSRR-	Power Supply Rejection Ratio	+V_{CC} = +20V, -V_{CC}= -20V and -5V, R_S=50Ω		80		dB	1, 2, 3
CMRR	Common Mode Rejection Ratio	-15V ≤ V_{CM} ≤ 15V, R_S = 50Ω		80		dB	1, 2, 3

LM101A 883 Electrical Characteristics (Continued)

DC Parameters (Continued)

The following conditions apply to all parameters, unless otherwise specified

V_{CC} = ±20V, V_{CM}= 0V

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
I_{CC}	Supply Current				3.0	mA	1
					2.5	mA	2
					3.5	mA	3
$+V_{IO}$ Adj	Input Offset Voltage Adjust			4.0		mV	1, 2, 3
$-V_{IO}$ Adj	Input Offset Voltage Adjust				-4.0	mV	1, 2, 3
$+I_{OS}$	Short Circuit Current			-45	-7.0	mA	1, 2, 3
$-I_{OS}$	Short Circuit Current			7.0	45	mA	1, 2, 3
V_I	Input Voltage Range	V_{CC} = ±20V	(Note 6)	-15	15	V	1, 2, 3
$+A_{VS}$	Large Signal Gain	V_{CC} = ±15V, R_S = 0, R_L=2KΩ, V_O =10V		50		V/mV	4
				25		V/mV	5, 6
$-A_{VS}$	Large Signal Gain	V_{CC} = ±15V, R_S = 0, R_L=2KΩ, V_O =-10V		50		V/mV	4
				25		V/mV	5, 6
R_I	Input Resistance		(Note 7)	1.5		MΩ	4
			(Note 7)	0.5		MΩ	5, 6
$+V_{OP}$	Output Voltage Swing	R_L = 10KΩ		16		V	4, 5, 6
		R_L = 2KΩ		15		V	4, 5, 6
		R_L = 10KΩ, V_{CC} = ±15V		12		V	4, 5, 6
		R_L = 2KΩ, V_{CC} = ±15V		10		V	4, 5, 6
$-V_{OP}$	Output Voltage Swing	R_L = 10KΩ			-16	V	4, 5, 6
		R_L = 2KΩ			-15	V	4, 5, 6
		R_L = 10KΩ, V_{CC} = ±15V			-12	V	4, 5, 6
		R_L = 2KΩ, V_{CC} = ±15V			-10	V	4, 5, 6

AC Parameters

The following conditions apply to all parameters, unless otherwise specified

V_{CC} = ±20V, R_L = 2KΩ, A_V = 1

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
+SR	Slew Rate	V_I = -5V to 5V			0.2	V/µS	7
-SR	Slew Rate	V_I = 5V to -5V			0.2	V/µS	7
G_{BW}	Gain Bandwidth	V_I = 50mV_{RMS}, f = 20KHz			0.25	MHz	7

LM101A QML & RH Electrical Characteristics (Note 10)

DC Parameters

The following conditions apply to all parameters, unless otherwise specified

V_{CC} = ±20V, V_{CM} = 0V, R_S = 50Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC}$ = 35V, $-V_{CC}$ = -5V, V_{CM} = -15V		-2.0	+2.0	mV	1
				-3.0	+3.0	mV	2, 3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -35V, V_{CM} = +15V		-2.0	+2.0	mV	1
				-3.0	+3.0	mV	2, 3
		V_{CM} = 0V		-2.0	+2.0	mV	1
				-3.0	+3.0	mV	2, 3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -5V, V_{CM} = 0V		-2.0	+2.0	mV	1
				-3.0	+3.0	mV	2, 3
I_{IO}	Input Offset Current	$+V_{CC}$ = 35V, $-V_{CC}$ = -5V, V_{CM} = -15V, R_S = 100KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -35V, V_{CM} = +15V, R_S = 100KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
		V_{CM} = 0V, R_S = 100KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -5V, V_{CM} = 0V, R_S = 100KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
$\pm I_{IB}$	Input Bias Current	$+V_{CC}$ = 35V, $-V_{CC}$ = -5V, V_{CM} = -15V, R_S = 100KΩ		-0.1	75	nA	1, 2
				-0.1	100	nA	3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -35V, V_{CM} = +15V, R_S = 100KΩ		-0.1	75	nA	1, 2
				-0.1	100	nA	3
		V_{CM} = 0V, R_S = 100KΩ		-0.1	75	nA	1, 2
				-0.1	100	nA	3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -5V, V_{CM} = 0V, R_S = 100KΩ		-0.1	75	nA	1, 2
				-0.1	100	nA	3
+PSRR	Power Supply Rejection Ratio	$+V_{CC}$ = 10V, $-V_{CC}$ = -20V		-50	+50	µV/V	1
				-100	+100	µV/V	2, 3
-PSRR	Power Supply Rejection Ratio	$+V_{CC}$ = 20V, $-V_{CC}$ = -10V		-50	+50	µV/V	1
				-100	+100	µV/V	2, 3
CMRR	Common Mode Rejection Ratio	V_{CC} = ±35V to ±5V, V_{CM} = ±15V		80		dB	1, 2, 3
$+V_{IO}$ Adj	Adjustment for Input Offset Voltage			4.0		mV	1, 2, 3
$-V_{IO}$ Adj	Adjustment for Input Offset Voltage				-4.0	mV	1, 2, 3
$+I_{OS}$	Output Short Circuit Current	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, t ≤ 25mS, V_{CM} = -15V		-60		mA	1, 2, 3
$-I_{OS}$	Output Short Circuit Current	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, t ≤ 25mS, V_{CM} = +15V			+60	mA	1, 2, 3
I_{CC}	Power Supply Current	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V			3.0	mA	1
					2.32	mA	2
					3.5	mA	3
$\Delta V_{IO}/\Delta T$	Temperature Coefficient of Input Offset Voltage	-55˚C ≤ T_A ≤ +25˚C	(Note 8)	-18	+18	µV/˚C	2
		+25˚C ≤ T_A ≤ +125˚C	(Note 8)	-15	+15	uV/˚C	3
$\Delta I_{IO}/\Delta T$	Temperature Coefficient of Input Offset Current	-55˚C ≤ T_A ≤ +25˚C	(Note 8)	-200	+200	pA/˚C	2
		+25˚C ≤ T_A ≤ +125˚C	(Note 8)	-100	+100	pA/˚C	3

LM101A QML & RH Electrical Characteristics (Note 10) (Continued)

DC Parameters (Continued)

The following conditions apply to all parameters, unless otherwise specified

V_{CC} = ±20V, V_{CM} = 0V, R_S = 50Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
$-A_{VS}$	Large Signal (Open Loop) Voltage Gain	R_L = 2KΩ, V_O = -15V	(Note 9)	50		V/mV	4
			(Note 9)	25		V/mV	5, 6
		R_L = 10KΩ, V_O = -15V	(Note 9)	50		V/mV	4
			(Note 9)	25		V/mV	5, 6
$+A_{VS}$	Large Signal (Open Loop) Voltage Gain	R_L = 2KΩ, V_O = +15V	(Note 9)	50		V/mV	4
			(Note 9)	25		V/mV	5, 6
		R_L = 10KΩ, V_O = +15V	(Note 9)	50		V/mV	4
			(Note 9)	25		V/mV	5, 6
A_{VS}	Large Signal (Open Loop) Voltage Gain	V_{CC} = ±5V,R_L = 2KΩ, V_O = ±2V	(Note 9)	10		V/mV	4,5, 6
		V_{CC} = ±5V, R_L = 10KΩ, V_O = ±2V	(Note 9)	10		V/mV	4,5, 6
$+V_{OP}$	Output Voltage Swing	R_L = 10KΩ, V_{CM} = -20V		+16		V	4,5, 6
		RL = 2KΩ, V_{CM} = -20V		+15		V	4,5, 6
$-V_{OP}$	Output Voltage Swing	R_L = 10KΩ, V_{CM} = 20V			-16	V	4,5, 6
		R_L = 2KΩ, V_{CM} = 20V			-15	V	4,5, 6

AC Parameters

The following conditions apply to all parameters, unless otherwise specified

V_{CC} = ±20V, V_{CM} = 0V, R_S = 50Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
+SR	Slew Rate	A_V = 1, V_I = -5V to +5V		0.3		V/µS	7, 8A
				0.2		V/µS	8B
-SR	Slew Rate	A_V = 1, V_I = +5V to -5V		0.3		V/µS	7, 8A
				0.2		V/µS	8B
TR_{TR}	Rise Time	A_V = 1, V_I = 50mV			800	nS	7, 8A, 8B
TR_{OS}	Overshoot	A_V = 1, V_I = 50mV			25	%	7
					35	%	8A, 8B
NI_{BB}	Noise Broadband	BW = 10Hz to 5KHz, R_S = 0Ω			15	μV_{RMS}	7
NI_{PC}	Noise Popcorn	BW = 10Hz to 5KHz, R_S = 100KΩ			80	μV_{PK}	7

DC Parameters Drift Values

The following conditions apply to all parameters, unless otherwise specified

V_{CC} = ±20V, V_{CM} = 0V, R_S = 50Ω

Delta calculations performed on QMLV devices at group B, Subgroup 5 only.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage	V_{CM} = 0V		-0.5	0.5	mV	1
± I_{IB}	Input Bias Current	V_{CM} = 0V, R_S = 100KΩ		-7.5	7.5	nA	1

Notes

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do no guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A) / \theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 5: Human body model, 100 pF discharged through 1.5 kΩ.

Note 6: Parameter guaranteed by the input conditions of several DC parameters

Note 7: Parameter guaranteed, not tested.

Note 8: Calculated parameter

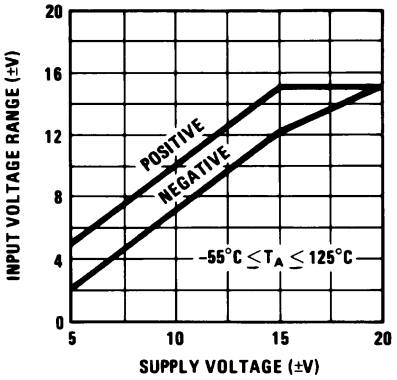
Note 9: Datalog reading of K = V/mV.

Note 10: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in Mil-Std-883, Method 1019

Note 11: Pin connections shown are for 8-pin packages.

Typical Performance Characteristics LM101A

Input Voltage Range



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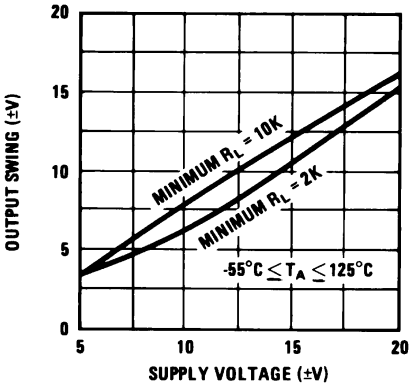
Output Swing



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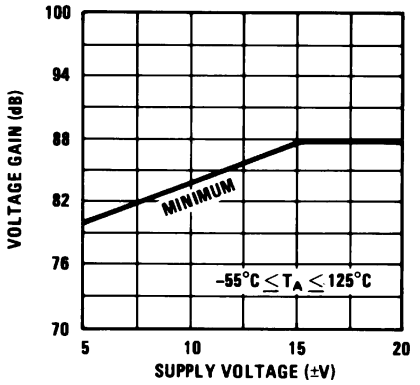
Voltage Gain



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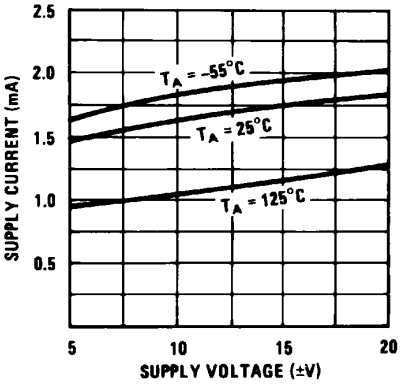
Supply Current



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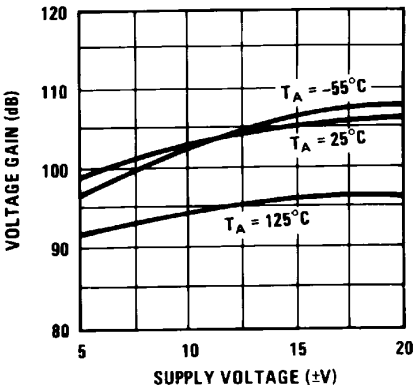
Voltage Gain



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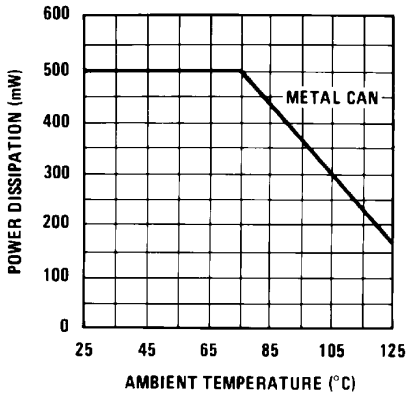
Typical Performance Characteristics LM101A (Continued)

Maximum Power Dissipation



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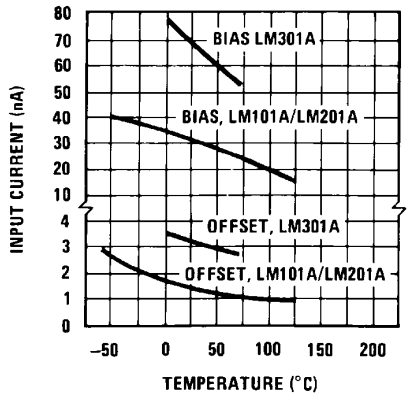
Input Current, LM101A



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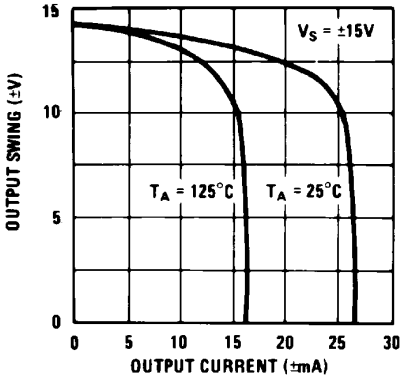
Current Limiting



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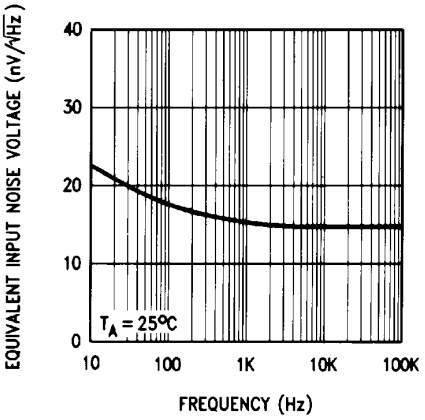
Input Noise Voltage



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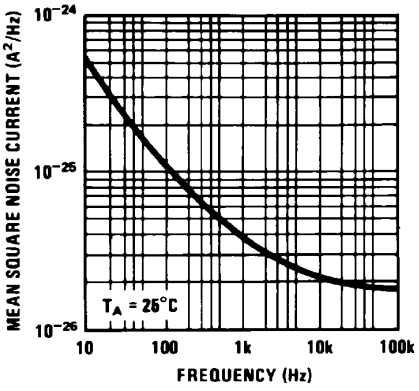
Input Noise Current



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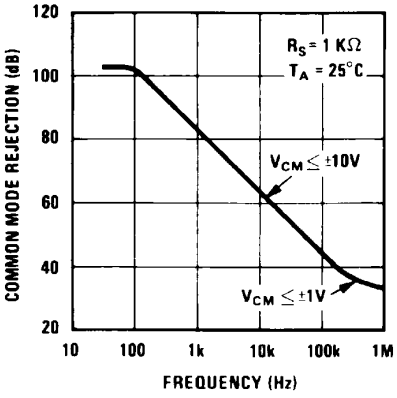
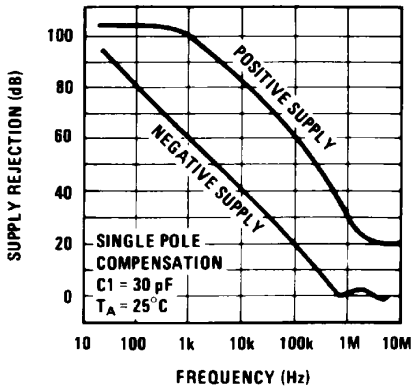
Common Mode Rejection



20122354

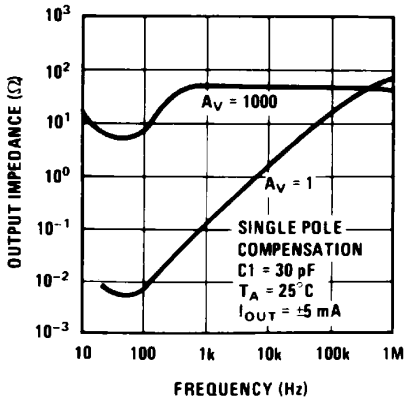
Typical Performance Characteristics LM101A (Continued)

Power Supply Rejection



20122355

Closed Loop Output Impedance

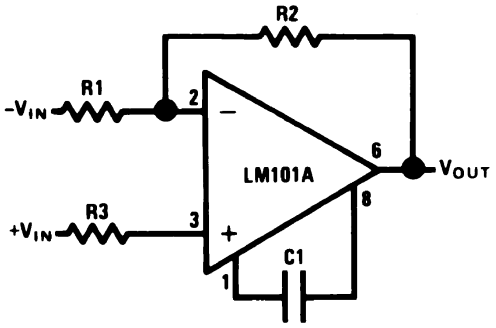


20122356

Typical Performance Characteristics for Various Compensation Circuits

(Note 11)

Single Pole Compensation

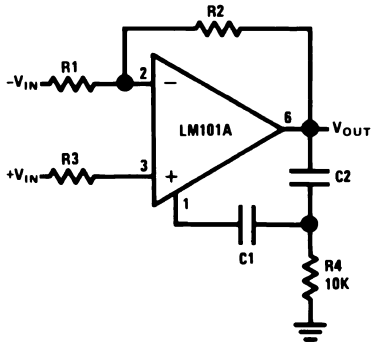


20122308

$$C1 \geq \frac{R1\,C_S}{R1 + R2}$$

C_S= 30 pF

Two Pole Compensation



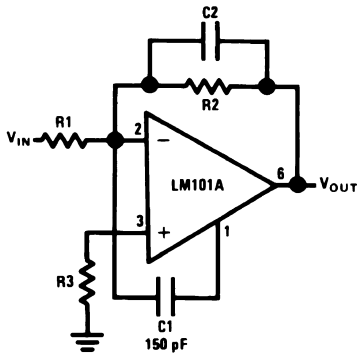
20122312

$$C1 \geq \frac{R1\,C_S}{R1 + R2}$$

C_S= 30 pF

C2 = 10 C1

Feedforward Compensation

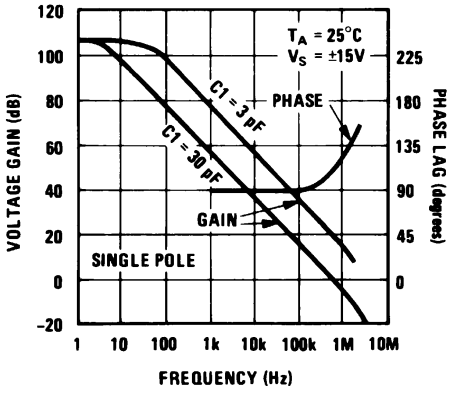


20122316

$$C2 = \frac{1}{2\pi\, f_o\, R2}$$

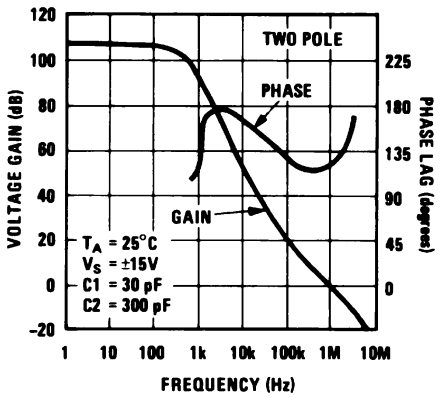
f_o= 3 MHz

Open Loop Frequency Response



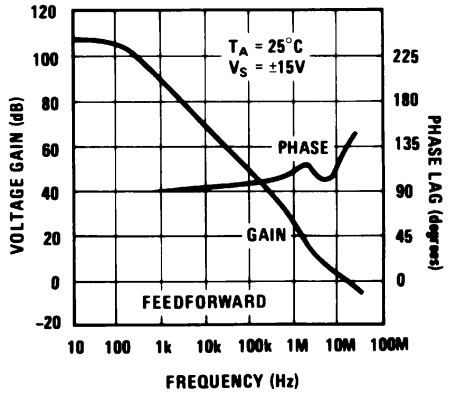
20122309

Open Loop Frequency Response



20122313

Open Loop Frequency Response

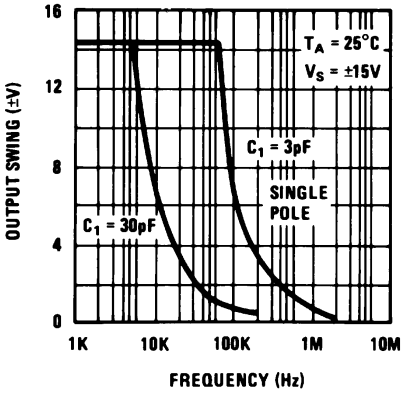


20122317

Typical Performance Characteristics for Various Compensation Circuits

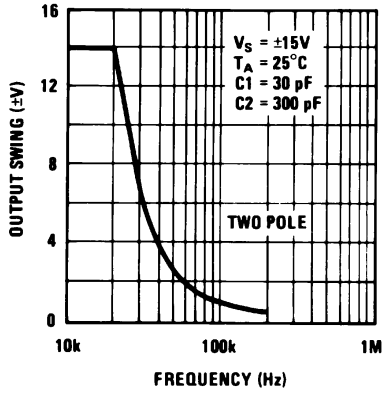
(Note 11) (Continued)

Large Signal Frequency Response



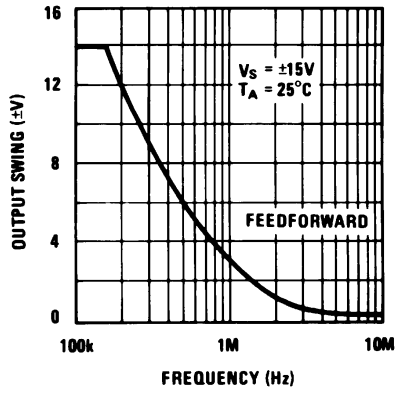
20122310

Large Signal Frequency Response



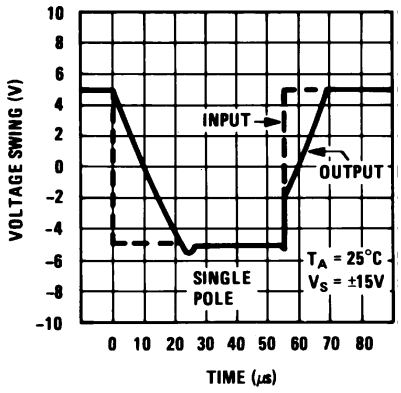
20122314

Large Signal Frequency Response



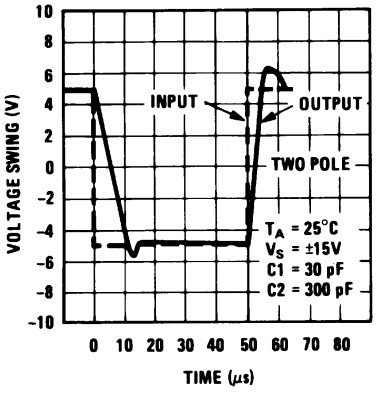
20122318

Voltage Follower Pulse Response



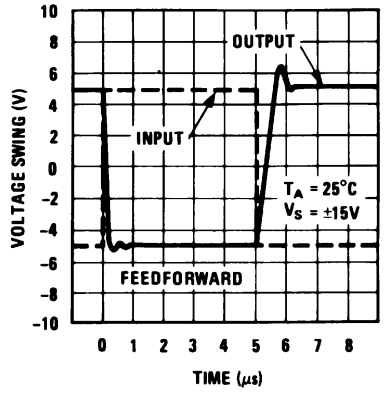
20122311

Voltage Follower Pulse Response



20122315

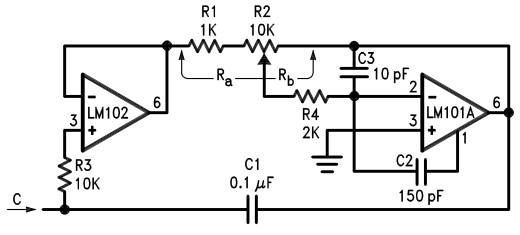
Inverter Pulse Response



20122319

Typical Applications (Note 11)

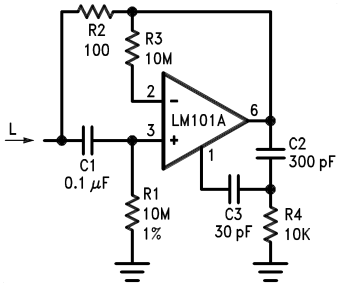
Variable Capacitance Multiplier



20122320

$$C = 1 + \frac{R_b}{R_a} C1$$

Simulated Inductor



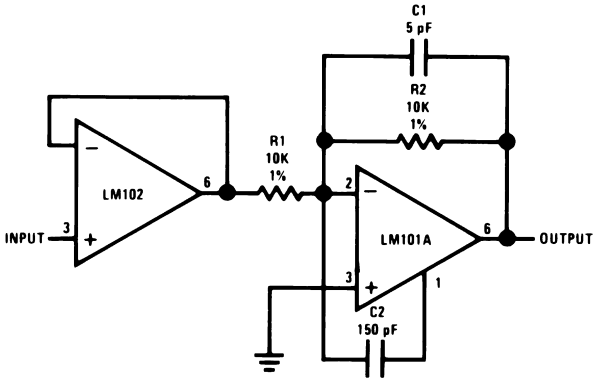
20122321

$L \simeq R1\ R2\ C1$

$R_S = R2$

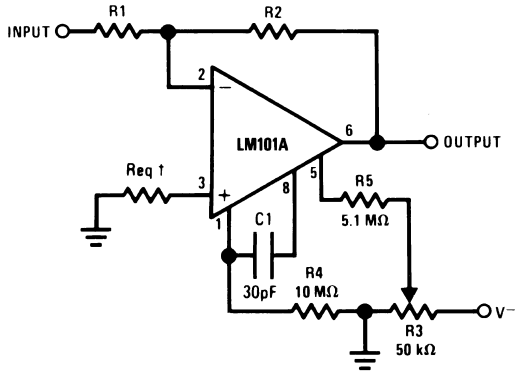
$R_P = R1$

Fast Inverting Amplifier with High Input Impedance



20122322

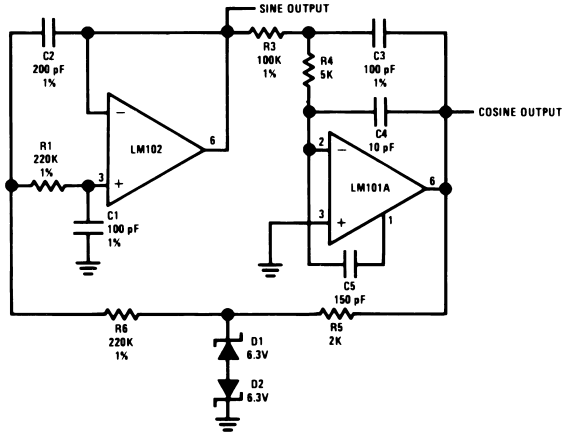
Inverting Amplifier with Balancing Circuit



20122323

†May be zero or equal to parallel combination of R1 and R2 for minimum offset.

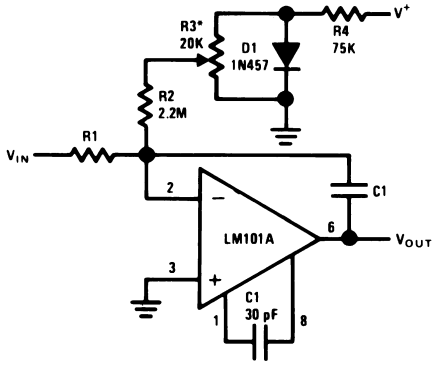
Sine Wave Oscillator



20122324

f_o = 10 kHz

Integrator with Bias Current Compensation

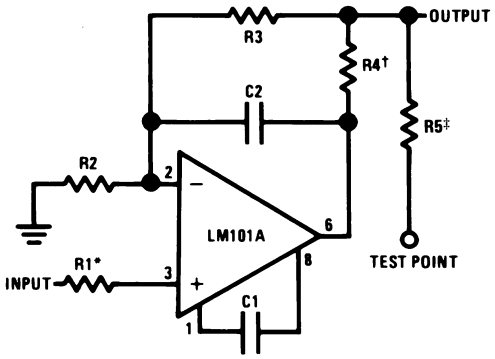


20122325

*Adjust for zero integrator drift. Current drift typically 0.1 nA/°C over −55°C to +125°C temperature range.

Application Hints (Note 11)

Protecting Against Gross Fault Conditions



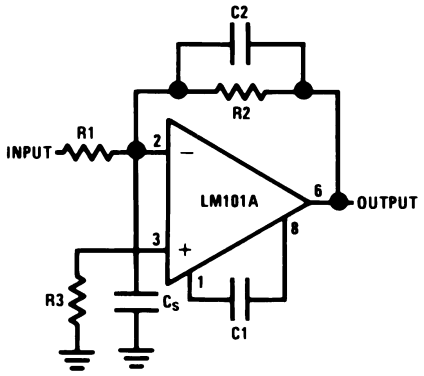
20122326

*Protects input

†Protects output

‡Protects output — not needed when R4 is used.

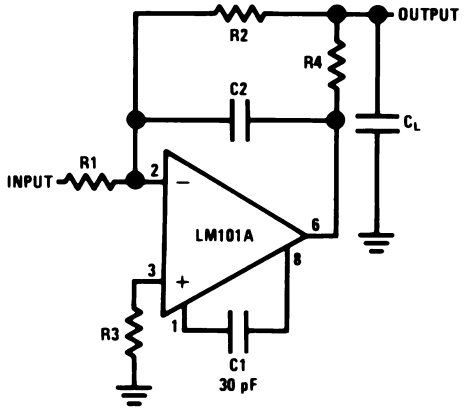
Compensating for Stray Input Capacitances or Large Feedback Resistor



20122327

$$C2 = \frac{R1\,C_S}{R2}$$

Isolating Large Capacitive Loads



20122328

Although the LM101A is designed for trouble free operation, experience has indicated that it is wise to observe certain precautions given below to protect the devices from abnormal operating conditions. It might be pointed out that the advice given here is applicable to practically any IC op amp, although the exact reason why may differ with different devices.

When driving either input from a low-impedance source, a limiting resistor should be placed in series with the input lead to limit the peak instantaneous output current of the source to something less than 100 mA. This is especially important when the inputs go outside a piece of equipment where they could accidentally be connected to high voltage sources. Large capacitors on the input (greater than 0.1 µF) should be treated as a low source impedance and isolated with a resistor. Low impedance sources do not cause a problem unless their output voltage exceeds the supply voltage. However, the supplies go to zero when they are turned off, so the isolation is usually needed.

The output circuitry is protected against damage from shorts to ground. However, when the amplifier output is connected to a test point, it should be isolated by a limiting resistor, as test points frequently get shorted to bad places. Further, when the amplifer drives a load external to the equipment, it is also advisable to use some sort of limiting resistance to preclude mishaps.

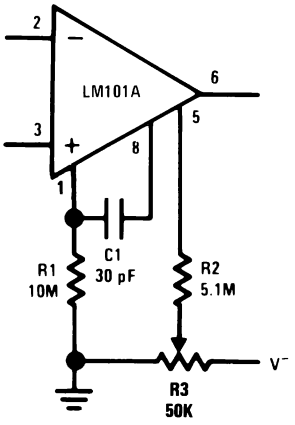
Precautions should be taken to insure that the power supplies for the integrated circuit never become reversed—even under transient conditions. With reverse voltages greater than 1V, the IC will conduct excessive current, fusing internal aluminum interconnects. If there is a possibility of this happening, clamp diodes with a high peak current rating should be installed on the supply lines. Reversal of the voltage between V^+ and V^- will always cause a problem, although reversals with respect to ground may also give difficulties in many circuits.

The minimum values given for the frequency compensation capacitor are stable only for source resistances less than 10 kΩ, stray capacitances on the summing junction less than 5 pF and capacitive loads smaller than 100 pF. If any of these conditions are not met, it becomes necessary to overcompensate the amplifier with a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors or an RC network can be added to isolate capacitive loads.

Although the LM101A is relatively unaffected by supply bypassing, this cannot be ignored altogether. Generally it is necessary to bypass the supplies to ground at least once on every circuit card, and more bypass points may be required if more than five amplifiers are used. When feed-forward compensation is employed, however, it is advisable to bypass the supply leads of each amplifier with low inductance capacitors because of the higher frequencies involved.

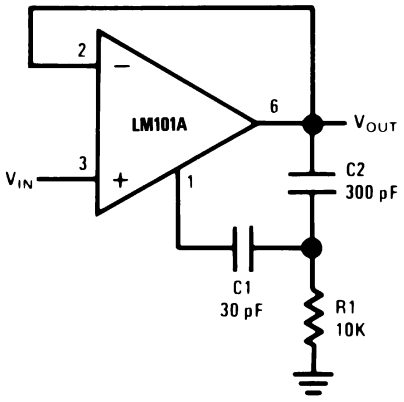
Typical Applications (Note 11)

Standard Compensation and Offset Balancing Circuit



20122329

Fast Voltage Follower

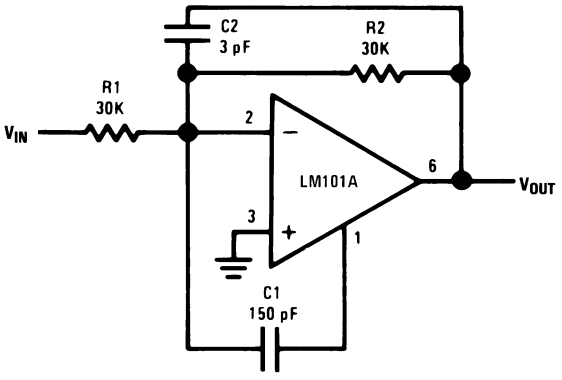


20122331

Power Bandwidth: 15 kHz

Slew Rate: 1V/µs

Fast Summing Amplifier



20122330

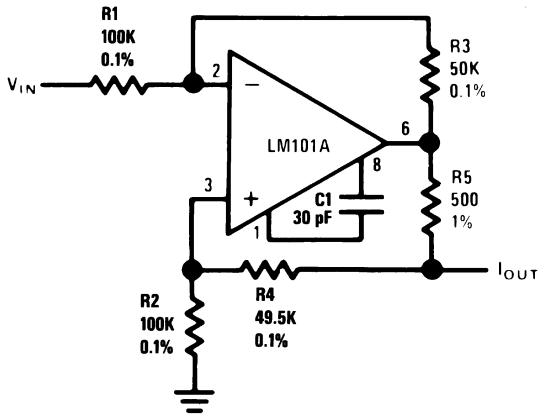
Power Bandwidth: 250 kHz

Small Signal Bandwiidth: 3.5 MHz

Slew Rate: 10V/µs

Typical Applications (Note 11) (Continued)

Bilateral Current Source



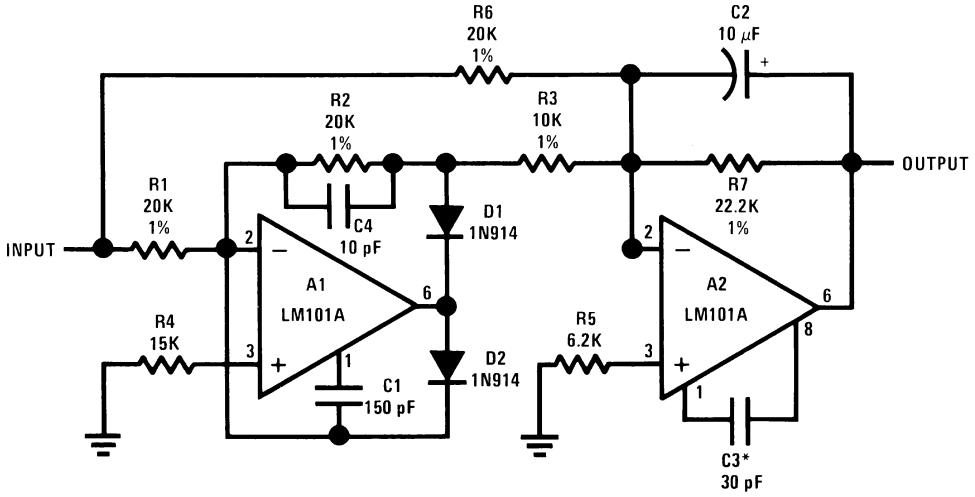
20122332

$$I_{OUT} = \frac{R3\ V_{IN}}{R1\ R5}$$

R3 = R4 + R5

R1 = R2

Fast AC/DC Converter (Note 12)

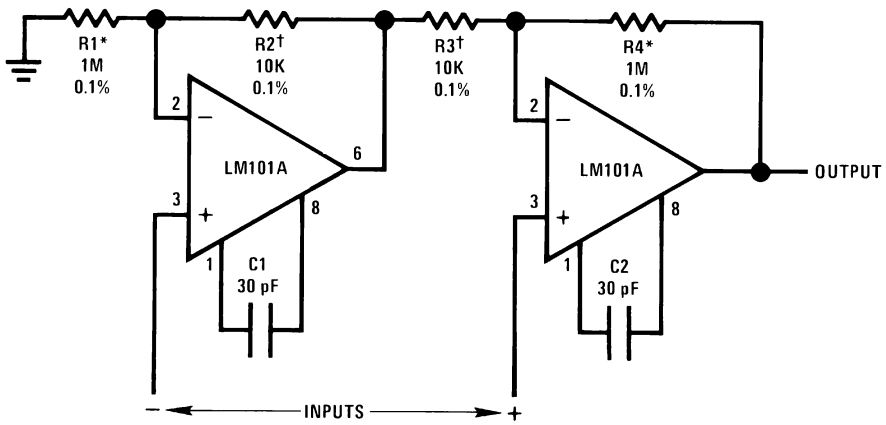


20122333

Note 12: Feedforward compensation can be used to make a fast full wave rectifier without a filter.

Typical Applications (Note 11) (Continued)

Instrumentation Amplifier



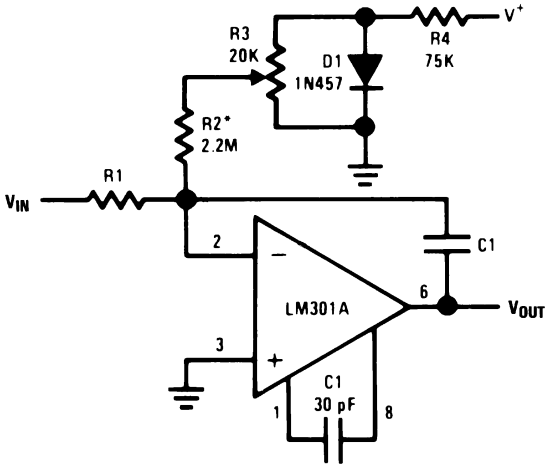
20122334

R1 = R4; R2 = R3

$$A_V = 1 + \frac{R1}{R2}$$

*,† Matching determines CMRR.

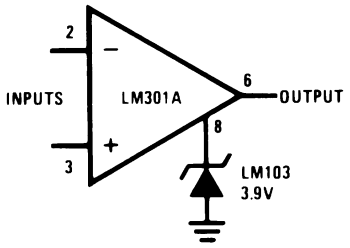
Integrator with Bias Current Compensation



20122335

*Adjust for zero integrator drift. Current drift typically 0.1 nA/˚C over 0˚C to +70˚C temperature range.

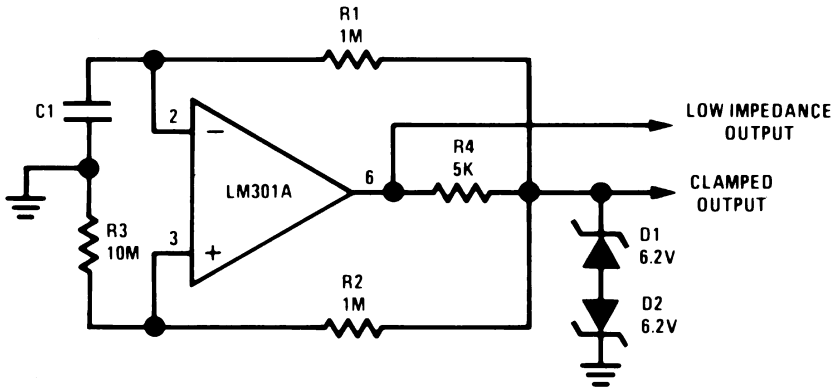
Voltage Comparator for Driving RTL Logic or High Current Driver



20122337

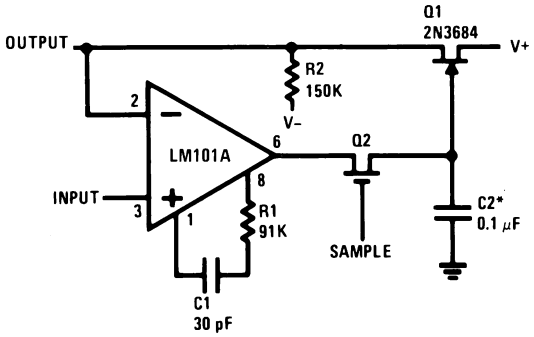
Typical Applications (Note 11) (Continued)

Low Frequency Square Wave Generator



20122336

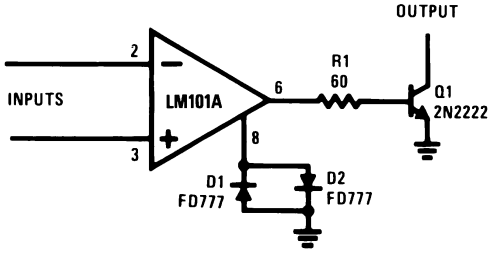
Low Drift Sample and Hold



20122338

*Polycarbonate-dielectric capacitor

Voltage Comparator for Driving DTL or TTL Integrated Circuits

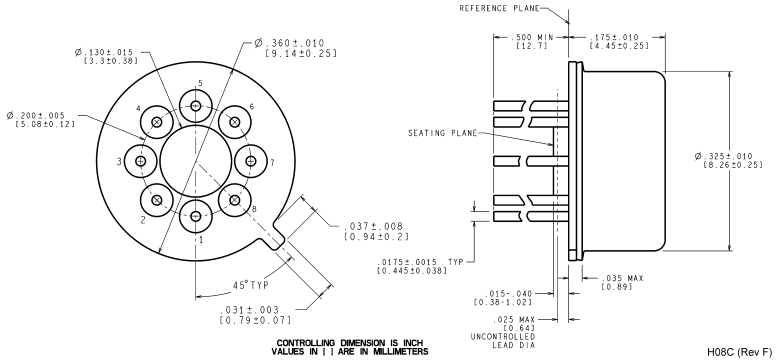


20122339

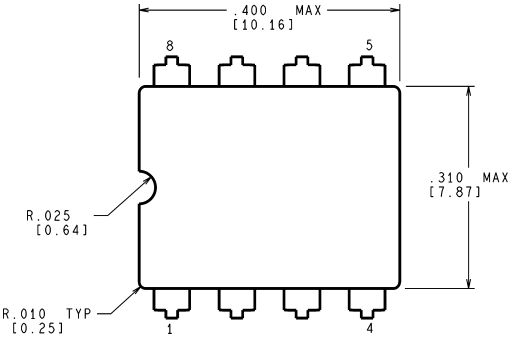
Revision History Section

Date Released	Revision	Section	Originator	Changes
01/05/06	A	New Release to corporate format	L. Lytle	2 MDS datasheets converted into one Corp. datasheet format. MNLM101A-X Rev 0A0 and MRLM101A-X-RH rev 1C2 MDS datasheets will be archived.

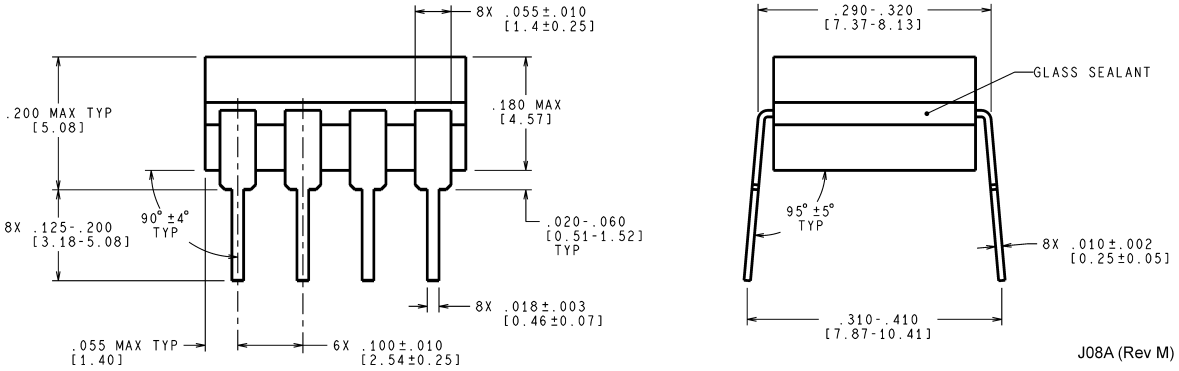
Physical Dimensions inches (millimeters) unless otherwise noted



Metal Can Package (H)
NS Package Number H08C

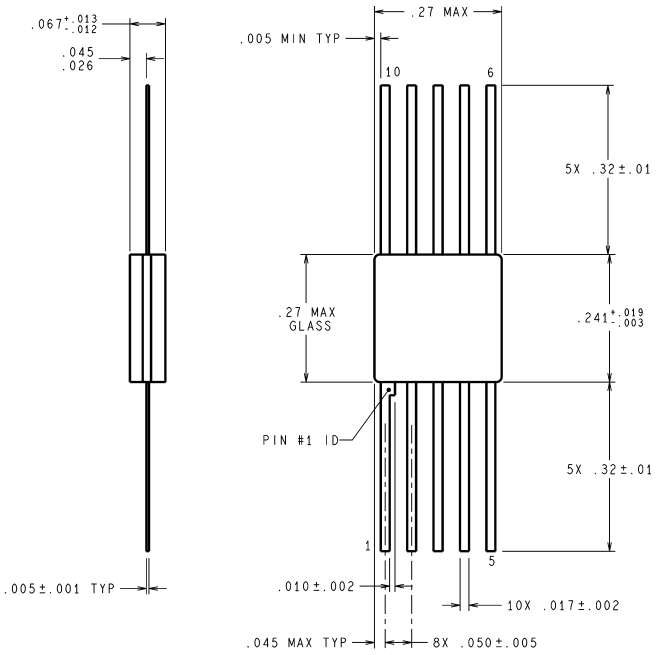


CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS



Ceramic Dual-In-Line Package (J)
NS Package Number J08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN INCHES

W10A (Rev H)

Ceramic Flatpack Package (W)
NS Package Number W10A

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