

1M x 9-Bit Dynamic RAM Module

HYM 91000S/L-60/-70/-80
HYM 91000SL/LL-60/-70

Advanced Information

- 1 048 576 words by 9-bit organization
- Fast access and cycle time
 - 60 ns access time
 - 110 ns cycle time (-60 version)
 - 70 ns access time
 - 130 ns cycle time (-70 version)
 - 80 ns access time
 - 150 ns cycle time (-80 version)
- Fast page mode capability with
 - 40 ns cycle time (-60/-70 version)
 - 45 ns cycle time (-80 version)
- Single + 5 V ($\pm 10\%$) supply
- Low power dissipation
 - max. 4455 mW active (-60 version)
 - max. 4000 mW active (-70 version)
 - max. 3500 mW active (-80 version)
 - CMOS – 50 mW standby
 - TTL – 100 mW standby
 - 15 mW under battery back up condition (HYM 91000SL/LL)
- Common $\overline{\text{CAS}}$ control for eight common data-in and data-out lines
- Separate $\overline{\text{CAS}}$ control for ninth bit
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, $\overline{\text{RAS}}$ -only refresh, Hidden-Refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs and clocks fully TTL compatible
- Single In-Line Memory Module socket (HYM 91000S/SL) and lead (HYM 91000L/LL) version
- Pin configuration and outline dimensions according to JEDEC standards
- Utilizes nine 1M-DRAMs in SOJ package
- 512 refresh cycles/8 ms (HYM 91000S/L)
- 512 refresh cycles/64 ms (HYM 91000SL/LL)

The HYM 91000S/L-60/-70/-80 is a 1 Mbyte RAM module organized as 1 048 576 words by 9-bit in a 30-pin single-in-line package comprising in HYB 511000J 1M × 1 DRAMs in SOJ-packages mounted together with nine 0.2 µF multilayer ceramic decoupling capacitors on a PC board.

The HYM 91000SL/LL-60/-70/-80 is the low power version comprising nine HYB 511000JL 1M × 1 low power DRAMs specially selected for battery backup applications.

Each HYB 511000J/JL is described in the data sheet and is fully electrically tested and processed according to Siemens standard quality procedure prior to module assembly. After assembly onto the board, a further set of electrical tests is performed.

A common $\overline{\text{CAS}}$ controls for eight common data-in and data-out lines. Bit nine (D8, Q8) which is generally used for parity is controlled by $\overline{\text{CAS}}$. The common I/O feature on the HYM 91500S/SL/L/LL-60/-70/-80 dictates the use of early write cycles to prevent contention on D and Q.

Ordering Information

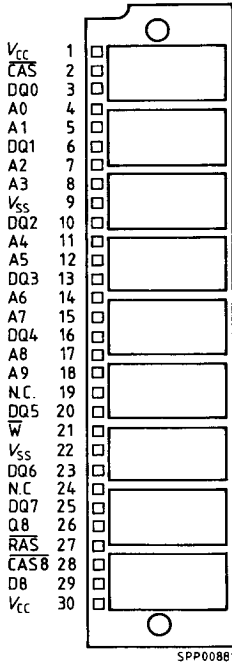
Type	Ordering Code	Package	Description
HYM 91000S-60	Q67100-Q470	L-SIM-30-800 JEDEC MO-064-AC	DRAM Module (access time 60 ns) ¹⁾
HYM 91000S-70	Q67100-Q445	L-SIM-30-800 JEDEC MO-064-AC	DRAM Module (access time 70 ns) ¹⁾
HYM 91000S-80	Q67100-Q396	L-SIM-30-800 JEDEC MO-064-AC	DRAM Module (access time 80 ns) ¹⁾
HYM 91000L-60	Q67100-Q564	L-SIM-30-800 JEDEC MO-068-AC	DRAM Module (access time 60 ns) ²⁾
HYM 91000L-70	Q67100-Q497	L-SIM-30-800 JEDEC MO-068-AC	DRAM Module (access time 70 ns) ²⁾
HYM 91000L-80	Q67100-Q448	L-SIM-30-800 JEDEC MO-068-AC	DRAM Module (access time 80 ns) ²⁾
HYM 91000SL-60	Q67100-Q569	L-SIM-30-800 JEDEC MO-064-AC	DRAM Module (access time 60 ns) Low Power ¹⁾
HYM 91000SL-70	Q67100-Q571	L-SIM-30-800 JEDEC MO-064-AC	DRAM Module (access time 70 ns) Low Power ¹⁾
HYM 91000LL-60	Q67100-Q570	L-SIM-30-800 JEDEC MO-068-AC	DRAM Module (access time 60 ns) Low Power ²⁾
HYM 91000LL-70	Q67100-Q572	L-SIM-30-800 JEDEC MO-068-AC	DRAM Modules (access time 70 ns) Low Power ²⁾

¹⁾ socket type

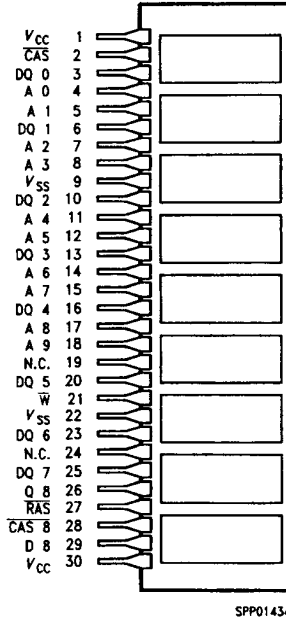
²⁾ pin type

Pin Configuration

HYM 91000S/SL
 (Socket type)



HYM 91000L/LL
 (Pin type)

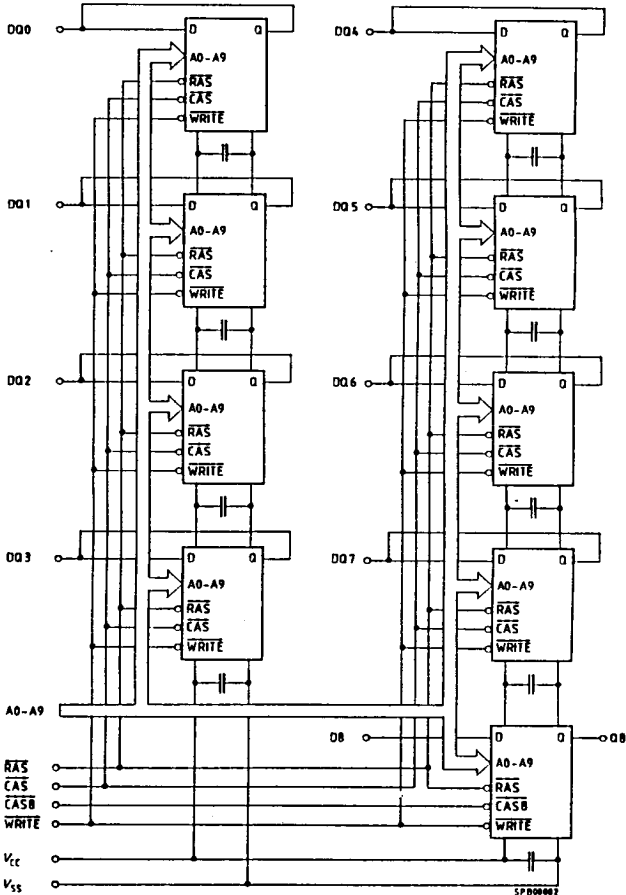


Pin Names

A0-A9	Address Inputs
DQ0-DQ7	Data Input Output
D8	Data Input
Q8	Data Output
CAS	Column Address Strobe

RAS	Row Address Strobe
WRITE	Read/Write Input
CAS	Column Address Strobe
V _{cc}	Power Supply (+ 5 V)
V _{ss}	Ground (0 V)
N.C.	No Connection

Block Diagram



Absolute Maximum Ratings

Operating temperature range	0 to + 70 °C
Storage temperature range	- 55 to + 125 °C
Soldering temperature	260 °C
Soldering time	10 s
Input/output voltage	- 1 to + 7 V
Power supply voltage	- 1 to + 7 V
Power dissipation	5.4 W
Data out current (short circuit)	50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0$ to 70 °C; $V_{CC} = 5$ V ± 10 %

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
Input high voltage	V_{IH}	2.4	6.5	V	—
Input low voltage	V_{IL}	- 1.0	0.8	V	—
Output high voltage ($I_{OUT} = - 5$ mA)	V_{OH}	2.4	—	V	—
Output low voltage ($I_{OUT} = 4.2$ mA)	V_{OL}	—	0.4	V	—
Input leakage current (0 V ≤ V_{IN} ≤ 6.5 V, all other pins = 0 V)	$I_{I(L)}$	- 20	20	μA	—
Output leakage current (DO is disabled, 0 V ≤ V_{OUT} ≤ 5.5 V)	$I_{O(L)}$	- 20	20	μA	—
Average V_{CC} supply current: HYM 91000**-60 HYM 91000**-70 HYM 91000**-80 (RAS, CAS, address cycling: $t_{RC} = t_{RC}$ min.)	I_{CC1}	—	810 720 630	mA mA mA	1) 2) 3) 1) 2) 3) 1) 2) 3)
Standby V_{CC} supply current (RAS = CAS = V_{IH})	I_{CC2}	—	18	mA	1)
Average V_{CC} supply current, during RAS-only refresh cycles: HYM 91000**-60 HYM 91000**-70 HYM 91000**-80 (RAS cycling, CAS = $V_{IH} = t_{RC} = t_{RC}$ min.)	I_{CC3}	—	810 720 630	mA mA mA	1) 2) 3) 1) 2) 3) 1) 2) 3)

Notes see page 9.

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Test condition
		min.	max.		
Average V_{CC} supply current, during fast page mode: HYM 91000**-60 HYM 91000**-70 HYM 91000**-80 ($\overline{RAS} = V_{IL}$, \overline{CAS} address cycling: $t_{PC} = t_{RC}$ min.)	I_{CC4}	—	630 540 450	mA mA mA	1) 2) 3) 1) 2) 3) 1) 2) 3)
Standby V_{CC} supply current: ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2$ V)	I_{CC5}	—	9	mA	—
Average V_{CC} supply current, during \overline{CAS} -before- \overline{RAS} -mode: HYM 91000**-60 HYM 91000**-70 HYM 91000**-80 (\overline{RAS} , \overline{CAS} cycling: $t_{RC} = t_{RC}$ min.)	I_{CC6}	—	810 720 630	mA mA mA	1) 1) 1)

for HYM 91000SL/LL only:

Standby V_{CC} supply current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC2}	—	1.8	mA	1)
Battery backup current average power supply current battery backup mode: ($\overline{CAS} = \overline{CAS}$ before \overline{RAS} cycling or 0.2 V, $\overline{WRITE} = V_{CC} - 0.2$ V or 0.2 V, $A0$ to $A9 = V_{CC} - 0.2$ V or 0.2 V, $DI = V_{CC} - 0.2$ V or 0.2 V or open, $t_{RC} = 125$ μ S, $t_{RAS} = t_{RAS}$ min. - 1 μ S)	I_{CC7}	—	2.7	mA	2) 13)

Notes see page 9.

AC Characteristics ^{4) 5)}

$T_A = 0$ to 70 °C; $V_{CC} = 5$ V \pm 10 %; $t_T = 5$ ns

Parameter	Symbol	Limit Values						Unit
		HYM 91000***-60		HYM 91000***-70		HYM 91000***-80		
		min.	max.	min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	–	130	–	150	–	ns
Fast page mode cycle time	t_{PC}	40	–	40	–	45	–	ns
Access time from \overline{RAS}	^{6) 11)} t_{RAC}	–	60	–	70	–	80	ns
Access time from \overline{CAS}	^{6) 11)} t_{CAC}	–	20	–	20	–	20	ns
Access time from column address	^{6) 12)} t_{AA}	–	30	–	35	–	40	ns
Access time from \overline{CAS} precharge	⁶⁾ t_{CPA}	–	30	–	35	–	40	ns
\overline{CAS} to output in low-Z	⁶⁾ t_{CLZ}	0	–	0	–	0	–	ns
Output buffer turn-off delay	⁷⁾ t_{OFF}	0	20	0	20	0	20	ns
Transition time (rise and fall)	⁷⁾ t_T	3	50	3	50	3	50	ns
\overline{RAS} precharge time	t_{RP}	40	–	50	–	60	–	ns
\overline{RAS} pulse width	t_{RAS}	60	10000	70	10000	80	10000	ns
\overline{RAS} pulse width (fast page mode)	t_{RASP}	60	100000	70	100000	80	100000	ns
\overline{RAS} hold time	t_{RSH}	20	–	20	–	20	–	ns
\overline{CAS} hold time	t_{CSH}	60	–	70	–	80	–	ns
\overline{CAS} pulse width	t_{CAS}	20	10000	20	10000	20	10000	ns
\overline{RAS} to \overline{CAS} delay time	¹¹⁾ t_{RCD}	20	40	20	50	20	60	ns
\overline{RAS} to column address delay time	¹²⁾ t_{RAD}	15	30	15	35	15	40	ns
\overline{CAS} to \overline{RAS} precharge time	t_{CRP}	5	–	5	–	5	–	ns
\overline{CAS} precharge time (fast page mode)	t_{CP}	10	–	10	–	10	–	ns
Row address setup time	t_{ASR}	0	–	0	–	0	–	ns
Row address hold time	t_{RAH}	10	–	10	–	10	–	ns
Column address setup time	t_{ASC}	0	–	0	–	0	–	ns
Column address hold time	t_{CAH}	15	–	15	–	15	–	ns
Column address hold time referenced to \overline{RAS}	t_{AR}	50	–	55	–	60	–	ns
Column address to \overline{RAS} lead time	t_{RAL}	30	–	35	–	40	–	ns
Read command setup time	t_{RSC}	0	–	0	–	0	–	ns
Read command hold time	⁸⁾ t_{RCH}	0	–	0	–	0	–	ns
Read command hold time referenced to \overline{RAS}	⁸⁾ t_{RRH}	0	–	0	–	0	–	ns
Write command hold time	t_{WCH}	15	–	15	–	15	–	ns
Write command hold time referenced to \overline{RAS}	t_{WCR}	50	–	55	–	60	–	ns

Notes see page 9.

AC Characteristics (cont'd) ^{4) 5)}

Parameter	Symbol	Limit Values						Unit
		HYM 91000**60		HYM 91000**70		HYM 91000**80		
		min.	max.	min.	max.	min.	max.	
Write command pulse width	t_{WP}	15	–	15	–	15	–	ns
Write command to \overline{RAS} lead time	t_{RWL}	20	–	20	–	20	–	ns
Write command to \overline{CAS} lead time	t_{CWL}	20	–	20	–	20	–	ns
Data setup time	⁹⁾ t_{DS}	0	–	0	–	0	–	ns
Data hold time	⁹⁾ t_{DH}	15	–	15	–	15	–	ns
Data hold time referenced to \overline{RAS}	t_{DHR}	50	–	55	–	60	–	ns
Refresh period HYM 91000 S/L	t_{REF}	–	8	–	8	–	8	ms
Refresh period HYM 91000 SL/LL	t_{REF}	–	64	–	64	–	64	ms
Write command setup time	¹⁰⁾ t_{WCS}	0	–	0	–	0	–	ns
\overline{CAS} setup time (\overline{CAS} -before- \overline{RAS} cycle)	t_{CSR}	10	–	10	–	10	–	ns
\overline{CAS} hold time (\overline{CAS} -before- \overline{RAS} cycle)	t_{CHR}	30	–	30	–	30	–	ns
\overline{RAS} to \overline{CAS} precharge time	t_{RPC}	0	–	0	–	0	–	ns
\overline{CAS} precharge time (\overline{CAS} -before- \overline{RAS} counter test cycle)	t_{CPT}	40	–	40	–	40	–	ns
\overline{CAS} precharge time	t_{CPN}	10	–	10	–	10	–	ns

Notes see page 9.

Capacitance

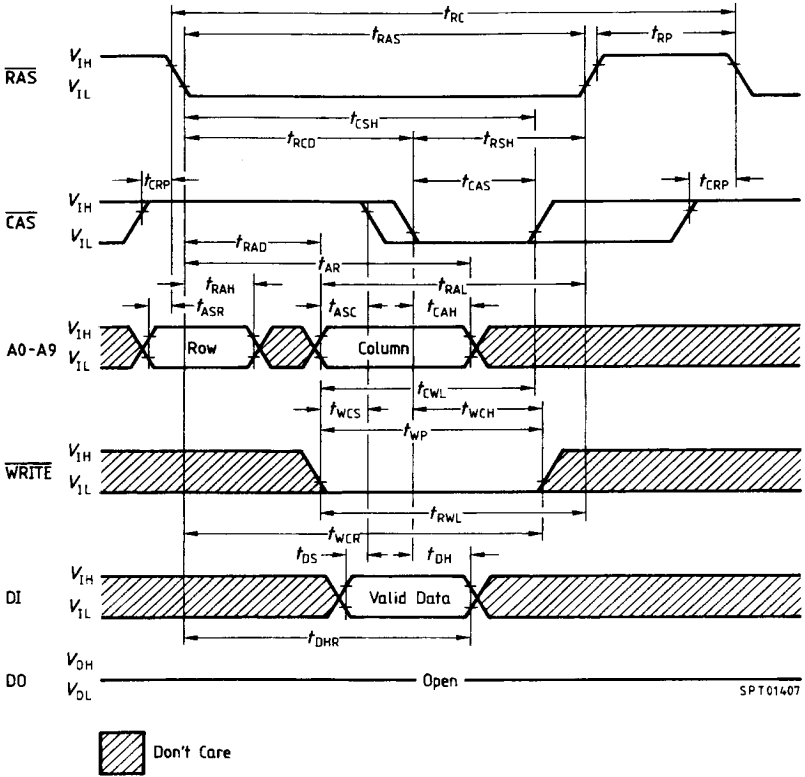
$T_A = 0$ to 70 °C; $V_{CC} = 5$ V ± 10 %; $f = 1$ MHz

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance (A0 to A9, \overline{RAS} , \overline{WE} , \overline{CAS})	C_{I1}	–	60	pF
Input capacitance (D8, $\overline{CAS8}$)	C_{I2}	–	10	pF
I/O capacitance (D0 to D8)	C_{I0}	–	15	pF
Output capacitance (Q8)	C_O	–	10	pF

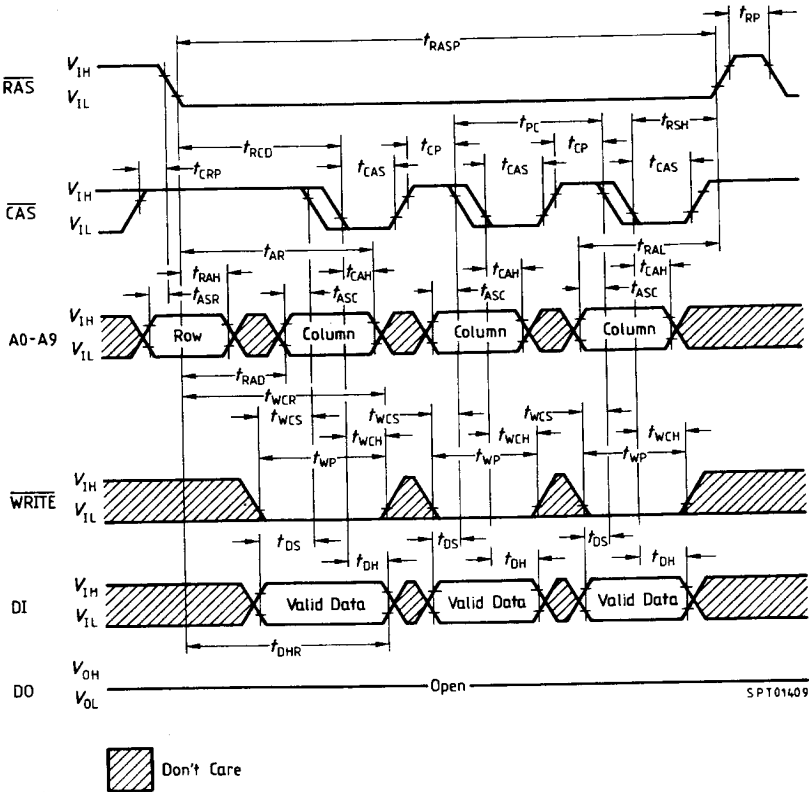
Notes for pages 5 to 8

- 1) All voltages are referenced to V_{SS} .
- 2) t_{CC1} , t_{CC3} , t_{CC4} and t_{CC6} depend on cycle rate.
- 3) t_{CC1} and t_{CC4} depend on output loading. Specified values are measured with the output open.
- 4) An initial pause of 200 μ s is required after power-up followed by 8 \overline{RAS} cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 \overline{CAS} -before- \overline{RAS} initialization cycles instead of 8 \overline{RAS} cycles is required.
- 5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL} .
- 6) Measured with a load equivalent of 2 TTL loads and 100 pF.
- 7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit conditions and is not referenced to output voltage levels.
- 8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- 9) These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{WRITE} leading edge in read-write cycles.
- 10) t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance).
- 11) Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC} .
- 12) Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA} .
- 13) t_{RAS} (max.) = 1 μ s is only applied to refresh of battery-backup.
 t_{RAS} (max.) = 10 μ s is applied to functional operating.

Write Cycle (early write)

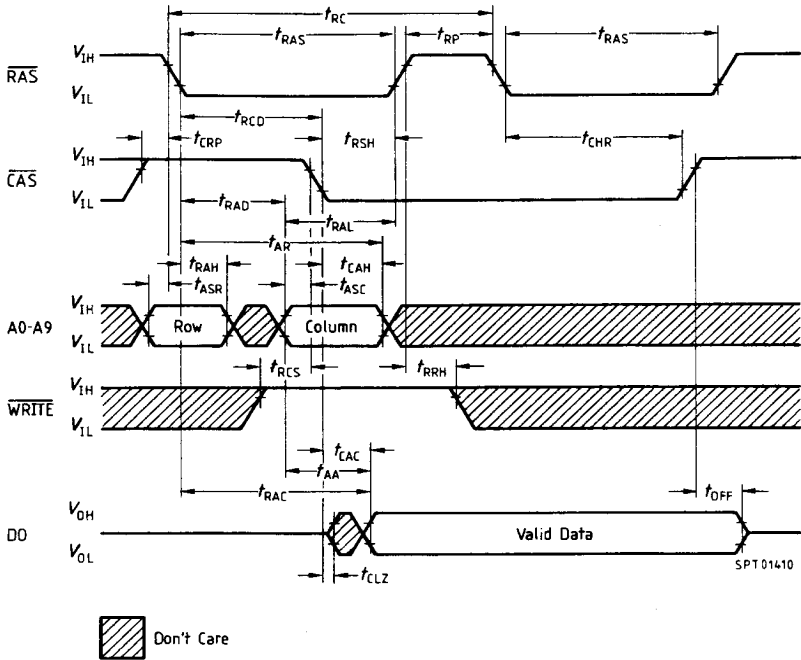


Fast Page Mode Write Cycle (early write)

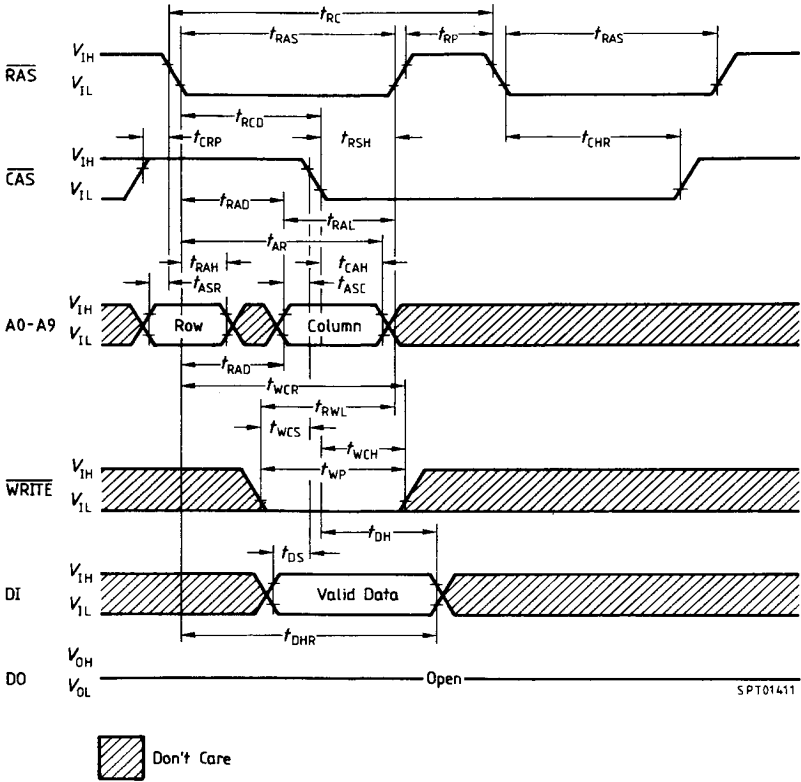


SPT01409

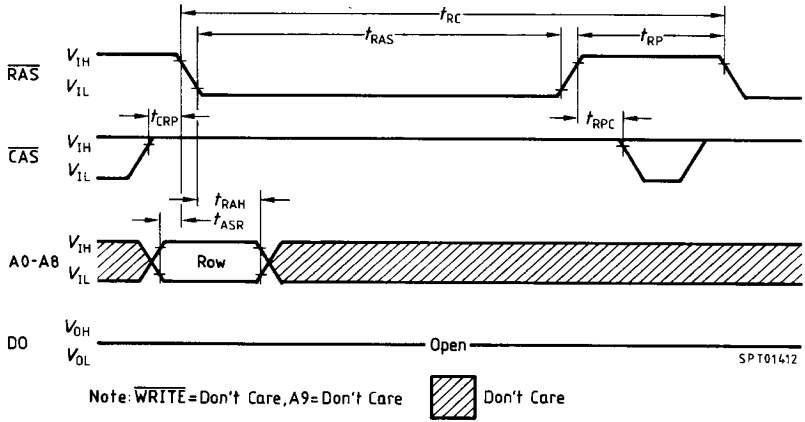
Hidden Refresh Cycle (read)



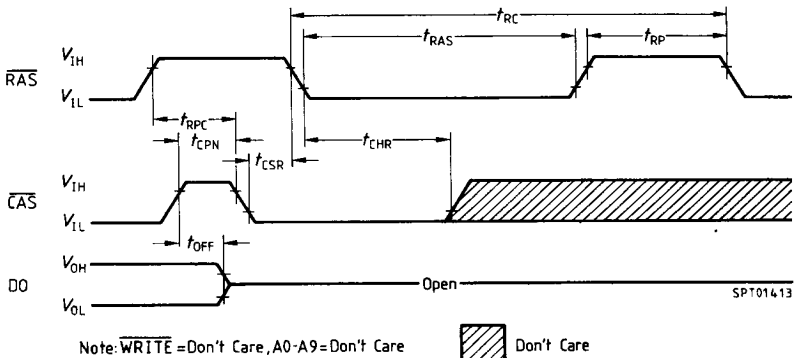
Hidden Refresh Cycle (write)



RAS-Only Refresh Cycle



CAS-Before-RAS Refresh Cycle

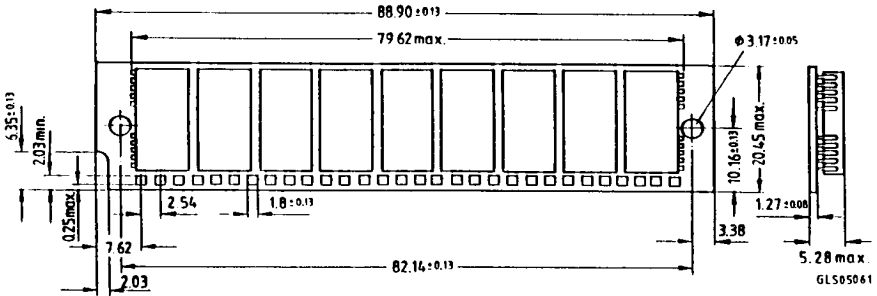


Package Outlines

Module Package, L-SIM-30-800, socket type

(Single in-Line Memory Module)

JEDEC MO-064-AC

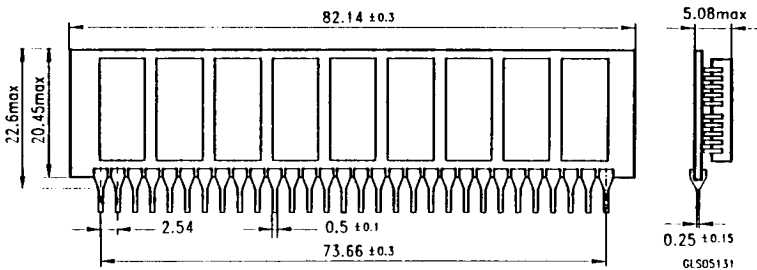


Dimensions in mm

Module Package, L-SIM-30-800, pin type

(Single in-Line Memory Module)

JEDEC MO-068-AC



Dimensions in mm