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Part Numbers
G2216-208-041PF B2 (SDSL 2B1Q)
G2214-208-041DF B2 (SDSL CAP)
G2237-208-041PT B2 (SHDSL/HDSL2)
G2237-208-041PT C1 (SHDSL/HDSL2)

XDSL2™ SDSL, HDSL2, or SHDSL - ILD2

Dual-Channel, Low Power, Programmable Transceiver with Integrated Framer and Line Drivers

Data Sheet

Overview

The GlobespanVirata® XDSL2™ Digital Subscriber Line (DSL) chip sets provide low power, high density solutions for 2-wire DSL equipment. These chip sets are fully programmable and field upgradeable eliminating the risk of product obsolescence and accelerating the time-to-market for new network services. The GlobespanVirata® XDSL2™ DSL chip sets are fully interoperable with multi-vendor DSL chip set solutions. This interoperability enables dynamic interworking of multiple vendor DSL solutions with the capability to interoperate with products that conform to ANSI and ETSI DSL standards.

GlobespanVirata's unique hardware platform supports multiple dual-channel applications including SDSL, HDSL2, and SHDSL, using population options for optimization.

The XDSL2 DSL chip sets incorporate two DSL bit pumps plus framing into a three-chip solution comprised of a dual-channel digital signal processor (DSP) with built-in framer and two Analog Front Ends each with an Integrated Line Driver (ILD2).

The XDSL2 chip sets interface directly with off-the-shelf T1/E1 transceivers and Nx64 multiplexing, eliminating the need for a separate DSL framer to combine and format the two DSL channels into a standard interface. GlobespanVirata's DSL XDSL2 chip sets deliver two channels of full duplex transmission up to 2320 kb/s, depending on the application.

The high density XDSL2 dual-channel DSL chip sets are ideal for CO applications, while single-channel versions with integrated framer are also available for CPE applications.

Features

- Dual-channel DSP with framer that fully integrates 2 separate DSL chips into a single device
- Two AFEs, each with an integrated differential line driver
- 2B1Q, CAP, or PAM line codes
- Supports dual-channel symmetric data rates of 144 kb/s to 2320 kb/s (depending on the application)
- Supports IDSL with optional data interface rates of 64 kb/s, 128 kb/s, and 144 kb/s
- Offers physical layer interoperability with competitive solutions
- Glueless interface to popular microprocessors
- Transmission compliant with ETSI TS 101 135, ITU-T G.991.1, and ANSI TR-28 for single pair 2B1Q and CAP, ANSI T1.418 for HDSL2 and ITU-T G.991.2 for SHDSL
- Reference design compatible with Bellcore GR-1089, IEC 60950, UL 1950, ITU-T K.20 and K.21
- Built-in framer provides easy access to EOC and indicator bits (framing can be bypassed completely for 2-channel independent operation)
- Interfaces directly with off-the-shelf single-channel T1/E1 transceivers
- ATM UTOPIA Level 1 and 2 interface
- A single oscillator and hybrid topology supports all speeds
- +3.3V and +5V power supplies

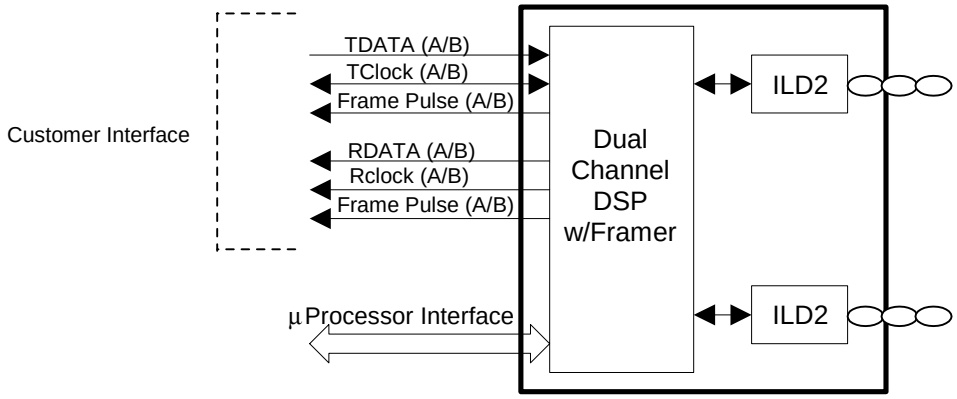


Figure 1. Block Diagram of XDSL2™ DSP with Two Single-Channel ILD2s

Introduction

The GlobespanVirata DSL chip sets support applications ranging from remote network access, digital pair gain, video conferencing, and cellular base station land-line connectivity, for T1/E1 services. Up to 36 voice circuits may be provisioned over a single copper pair.

Example Applications

- Compatibility with voice/data pair gain systems
- Cellular and microcellular systems
- T1/E1 and fractional T1/E1 DSL transceiver
- Wireless base station connectivity

Related Materials

To accelerate time-to-market, GlobespanVirata offers our customers a comprehensive Design Guide which includes details on planning, layout, testing, debugging, and expert tips and recommendations for building a successful DSL product. The Design Guide is distributed as part of a Design Package which includes firmware, transceiver schematics, sample code, transceiver layout Gerber files, and Bill of Materials.

For rapid prototyping, Quick Kits are available. These Quick Kits contain all transceiver design BOM components in kit form so there's no component lead time delay.

The Super GlobespanVirata Development System (SGDS™), an easy-to-use evaluation and development platform designed to support all GlobespanVirata xDSL transceiver solutions, is also available for early product development.

The SGDS also provides an interface to the GlobespanVirata Microsoft® Windows® - based Host Interface Program (WHIP). When the SGDS is teamed with WHIP, product evaluation, testing and debugging is achieved with the click of a mouse.

GlobespanVirata Transceiver System Overview

- The GlobespanVirata XDSL2™ DSL chip sets consist of a dual-channel DSP with an on-chip framer, and two single-channel AFEs (with ILD2).

- The single-channel ILD2s filter and digitize the signal received on the telephone line and for the transmit side, generate analog signals from the digital data and filter the analog signals to create the 2B1Q, CAP or PAM transmit signal (depending on the line code).

- The GlobespanVirata Windows-based Host Interface Program (WHIP) is offered as part of the GlobespanVirata transceiver system development package for SDSL 2B1Q, HDSL2, and SHDSL applications. WHIP allows you to test and debug your product design with the click of a mouse. This graphical interface allows you to send commands, perform trace and debug procedures, and initiate a startup on both the CO and CP units. WHIP offers complete flexibility and modularity - you can rearrange windows and toolbars to suit your preferences and design requirements.

- SDSL CAP applications are offered the GlobespanVirata Host Interface Program (HIP) software as part of the GlobespanVirata transceiver system development package. The PC-based HIP software provides a PC interface to the host. HIP allows the host to run scripts to obtain and manipulate data, test performance, and debug the software. No additional software or special PC hardware or tools are required. Customers who use HIP with their host processor receive the benefits of faster diagnosis and specialized assistance from the GlobespanVirata staff.

Architecture

The interface between the Host and the transceiver consists of the following:

- Transmission Interface (data, clock and synchronization signals)
- Control Interface (microprocessor compatible)
- Diagnostic Interface
- Power Interface
- Loop Interface

System timing is derived from a free running oscillator in the transceiver of the central office (CO). At the customer premises end (CPE), the CPE derives a clock from the received line signal and provides this clock to the CPE transmitter.

The dual-channel chip set also supports Network Timing Recovery (NTR) at the CO end. With this feature enabled, the CO unit will accept a clock at 8 kHz (± 100 ppm) as an input and the STU-R will output a clock that is phase locked to the CO clock. The NTR clock should have a duty cycle of 45-55%. Note that this feature is only available with an UTOPIA interface.

The DSL transceiver supports both T1 and E1 rates, and fractional rates.

Transceiver States

The following is a list of the possible states that the DSL transceiver can be in:

- IDLE mode, where the transceiver is not attempting to start up, pass data, or perform tests
- TEST mode, where the transceiver is either in local analog loopback or local digital loopback and is not passing user data
- STARTUP mode (SDSL only), where the transceiver is attempting a startup of the DSL connection, prior to entering DATA mode
- HANDSHAKE mode (HDSL2 and SHDSL), where a link is established between the CO unit and the CPE unit
- TRAINING mode (HDSL2 and SHDSL), where the transceiver is attempting a startup, prior to entering DATA mode
- DATA mode, where the transceiver has started up and trained and is capable of passing user data

Software Interface

A microprocessor interface that uses simple read/write drivers provides direct access to the GlobespanVirata chip set—eliminating the need for complicated register maps and advanced programming. These drivers allow the Host to select rates, adjust transmit power, read signal quality, and perform a variety of other tasks which include reporting the current operational status of the transceiver.

To configure and control the transceiver, GlobespanVirata provides hardware-dependent driver examples and GlobespanVirata supplied transceiver software modules (TSMs). The TSMs have the ability to allow a single CPU in the Host to control multiple transceivers. This could be a potential cost savings for arrangements where it might be advantageous to put multiple transceivers on one card, such as at the CO.

NOTE:
You will not need a register map of the DSP, as this information is not required to successfully design and implement an STU. As discussed previously, access to the DSP is provided through hardware-dependent I/O routines and GlobespanVirata provided TSMs.

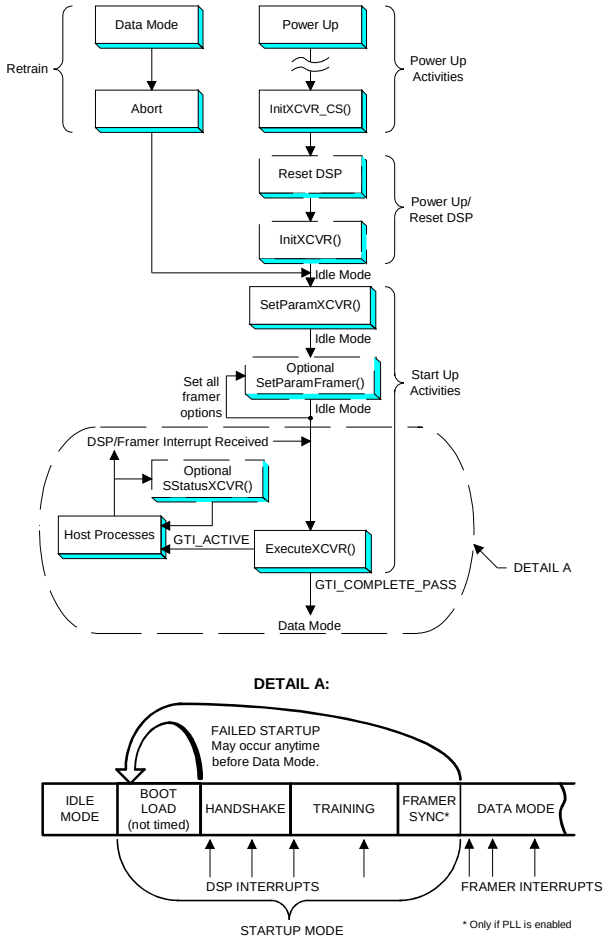


Figure 2. Typical Transceiver Power Up/Start Up Sequence

Transceiver Power Up Sequence

Figure 2 describes a typical sequence from power up to DATA mode for a transceiver. After power is applied to both the Host and the transceiver, the Host calls the `InitXCVR_CS()` and `InitXCVR()` routines to initialize transceiver variables and to initialize the DSP/Framer.

Next, the Host calls the `SetParamXCVR()` routine to set up the parameters that are appropriate for start up of the transceiver.

The `SetParamFramer()` routine is called by the Host to initialize framer options.

After setting up the transceiver parameters, the Host calls the `ExecuteXCVR()` routine to execute the command that was set up using the `SetParamXCVR()` routine. With a successful completion of the `ExecuteXCVR()` routine, the transceiver will now be in DATA mode.

The `SStatusXCVR()` routine is used to track performance and to obtain information from the transceiver about what state the transceiver is in (i.e., monitor start-up, check signal quality, etc.).

Setting Up the Command Parameters [SetParamXCVR()]

The routine `SetParamXCVR()` processes the parameter array structure that will be executed when the `ExecuteXCVR()` routine is called.

The parameter structure will be similar to the following start-up *example*:

```
struct PARAM_XCVR_ARRAY Items;
Items.length = GTI_NUM_OF_CMD_PARAMETERS
Items.item[GTI_ACTION_ITEM]=GTI_STARTUP_REQ;
Items.item[GTI_MODE_ITEM]=GTI_CO;
Items.item[GTI_POWER_SCALE_ITEM]=GTI_DEFAULT_SCALE;
Items.item[GTI_FRAMER_TYPE_ITEM]= GTI_UTOPIA_L2;
                                .
                                .
                                .
```

Table 1 describes the example arguments to the `SetParamXCVR()` routine when performing start-up. This is only a sample subset of possible parameters, provided to illustrate how easy it is to work with the GlobespanVirata chip sets.

Table 1. Example SetParamXCVR() Structure

Parameter	Function
GTI_ACTION_ITEM	The action GTI_STARTUP_REQ begins start-up, which, upon successful completion, results in the transceiver changing into DATA mode.
GTI_MODE_ITEM	Mode describes which transceiver the Host is talking to, the CO or CP.
GTI_POWER_SCALE_ITEM	Allows the transmit power to be set in small increments.
GTI_FRAMER_TYPE_ITEM	The framing modes are interface specific. Possible arguments for framing modes, depending on the customer interface, include: No Framing, UTOPIA Level 1, UTOPIA Level 2, T1, E1, and nxDS0 (with the ability to choose continuous DS0 blocks).

Checking the Transceiver Status [SStatusXCVR()]

The `SStatusXCVR()` routine can be executed when in DATA mode, utilizing minimal processing power. To further illustrate the ease of programming GlobespanVirata chip sets, Table 2 supplies a few examples of `SStatusXCVR()`.

Table 2. Example SStatusXCVR() Parameters

Parameter	Function
GTI_XMIT_POWER	This action returns the transmitted power.
GTI_START_PROGRESS	The current detailed start-up state of the transceiver is returned.
GTI_BERT_ERROR	The number of bit errors detected during the 511 BERT test is returned.
GTI_RECEIVER_GAIN	Total receiver gain setting can be calculated using the return values from this action.

System Power Requirements

The 144-pin Dual-channel DSP/Framer chip requires +3.3V (see Table 14 on page 16 for tolerance), and the two ILD2 chips require +3.3V (±5%) as well as +5V (±5%). Power requirements, including transceiver power consumption, have a tolerance of ±5%. The maximum peak-to-peak ripple and noise voltage is 50 mV for all supplies.

The transceiver obtains its power from the power feed in the Host through the power interface. Table 3, Table 4, Table 5, and Table 7 provide power requirements for the 144-pin Dual-channel DSP.

Table 3. Typical SDSL 2B1Q System Power Consumption Per Channel (DSP/Framer in a 144 LPQ2)

Line Rate (Kb/s)	Drain Current (mA)		Power/Port (mW)
	3.3VD DSP & ILD2	5VA ILD2	
144	75	85	673
272	105	85	772
400	110	90	813
528	115	90	830
784	160	90	978
1040	170	90	1011
1168	210	90	1143
1552	235	95	1251
2064	250	95	1300
2320	280	95	1400

NOTE:

1. Power per channel based on dual-channel operation

2. Based on customer schematic:
G-02-2302-1006C-02 using 1:2 transformer

Add 30 mA at 5VA for unified designs based on SHDSL population option G-02-2302-1006C-03 using 1:4 transformer or HDSL2 population option G-02-2302-1006C-03 using 1:5.4 transformer

3. Transmit power: 13.5 dbm (nominal at all rates)

4. Measured during activation and data mode

Table 4. Typical SDSL CAP System Power Consumption Per Channel (DSP/Framer in a 144 TQFP)

Line Rate (Kb/s)	Drain Current (mA)		Power/Port (mW)
	3.3VD DSP & ILD2	5VA ILD2	
144	75	90	698
272	80	90	714
400	115	105	905
528	145	115	1055
784	145	115	1055
1040	145	115	1055
1552	155	115	1087
2064	165	120	1145
2320	185	120	1210

NOTE:

1. Power per channel based on dual-channel operation

2. Based on customer schematic:
G-02-2302-1006C-03 using 1:4 transformer

3. Transmit power: 13.5 dbm (nominal at 2320kb/s)

4. Measured during activation and data mode

Table 5. Typical HDSL2 System Power Consumption Per Port (DSP/Framer in a 144 LPQ2)

Line Rate (Kb/s)	Drain Current (mA)		Power/Port (mW)
	3.3VD DSP & ILD2	5VA ILD2	
T1 (1.552)	270	150	1681

NOTE:

1. Power per channel based on dual-channel operation

2. Based on customer schematic: G-02-2302-1006C-01 using 1:5.4 transformer

3. Transmit power: 16.8 dbm (nominal)

Table 6. Maximum Junction Temperature

T_J Maximum
125 °C

Table 7. Typical SHDSL System Power Consumption Per Channel (DSP/Framer in a 144 LPQ2)

Line Rate (Kb/s)	Drain Current (mA)		Power/Port (mW)
	3.3VD DSP & ILD2	5VA ILD2	
144	100.0	125.0	955.0
200	105.0	125.0	971.5
208	105.0	125.0	971.5
272	120.0	125.0	1021.0
392	130.0	125.0	1054.0
400	130.0	125.0	1054.0
528	135.0	125.0	1070.5
776	160.0	125.0	1153.0
784	160.0	125.0	1153.0
1040	180.0	125.0	1219.0
1168	185.0	125.0	1235.5
1552	225.0	130.0	1392.5
2056	245.0	130.0	1458.5
2064	245.0	130.0	1458.5
2312	270.0	130.0	1541.0
2320	270.0	130.0	1541.0

NOTE:

1. Power per channel based on dual-channel operation

2. Based on customer schematic: G-02-2302-1006C-03 using 1:4 transformer

3. Transmit power: 13.5 dbm (nominal at all rates)

4. Measured during activation and data mode

5. All Nx64 payload rates are supported (where N = 3 through 36). The line rates listed in Table 7 are a few typical data points

Electrical Interface Specification

All processor interfaces, customer clock and data, and diagnostic interface inputs and outputs associated with the 144-pin DSP Core are compatible with 5V CMOS and TTL logic, as well as 3.3V CMOS logic. While the DSP is a 3.3V device, all the above inputs are designed to be 5V tolerant. The Control Interface supports multiplexed, non-multiplexed, and Motorola processor interface modes.

Performance

GlobespanVirata has rigorously tested the performance of the DSL chip sets, with the results detailed in Table 8, Table 9, Table 10 and Table 11.

Table 8. SDSL 2B1Q Performance Specifications (Reach in kft and km)

Line Rate (kb/s)	No Noise			
	24 AWG		26 AWG	
	kft	km	kft	km
144	25.4	7.7	21.0	6.4
272	23.6	7.2	19.5	5.9
400	22.4	6.8	17.3	5.2
528	21.3	6.5	16.1	4.9
784	19.1	5.8	15.2	4.6
1040	17.6	5.4	14.4	4.4
1168	15.9	4.8	13.8	4.2
1552	13.3	4.1	12.7	3.9
2064	11.8	3.6	11.1	3.4
2320	11.3	3.4	10.9	3.3

Table 9. SDSL CAP Performance Specifications (Reach in kft and km)

Line Rate (kb/s)	No Noise			
	24 AWG		26 AWG	
	kft	km	kft	km
144	30.4	9.2	21.4	6.5
272	30.3	9.2	20.3	6.1
400	28.7	8.7	18.8	5.7
528	26.2	7.9	17.0	5.3
784	23.1	7.0	15.8	4.8
1040	22.4	6.8	15.5	4.7
1552	19.4	5.9	13.9	4.2
2064	17.2	5.2	12.2	3.7
2320	15.8	4.8	11.7	3.5

Table 10. HDSL2 Performance Specifications (Reach in kft and km)

Line Rate (kb/s)	No Noise			
	24 AWG		26 AWG	
	kft	km	kft	km
T1 (1.552 kb/s)	18.0	5.5	13.5	4.1

Table 11. SHDSL Performance Specifications (Reach in kft and km)

Line Rate (kb/s)	No Noise	
	26 AWG	
	kft	km
144	26.0	7.9
200	21.4	6.5
392	19.9	6.0
520	18.7	5.7
776	17.5	5.3
1032	16.6	5.1
1168	15.8	4.8
1544	14.0	4.2
2056	13.0	3.9
2312	12.5	3.8

NOTE:
All Nx64 payload rates are supported (where N= 3 through 36). The line rates listed in Table 11 are a few typical data points.

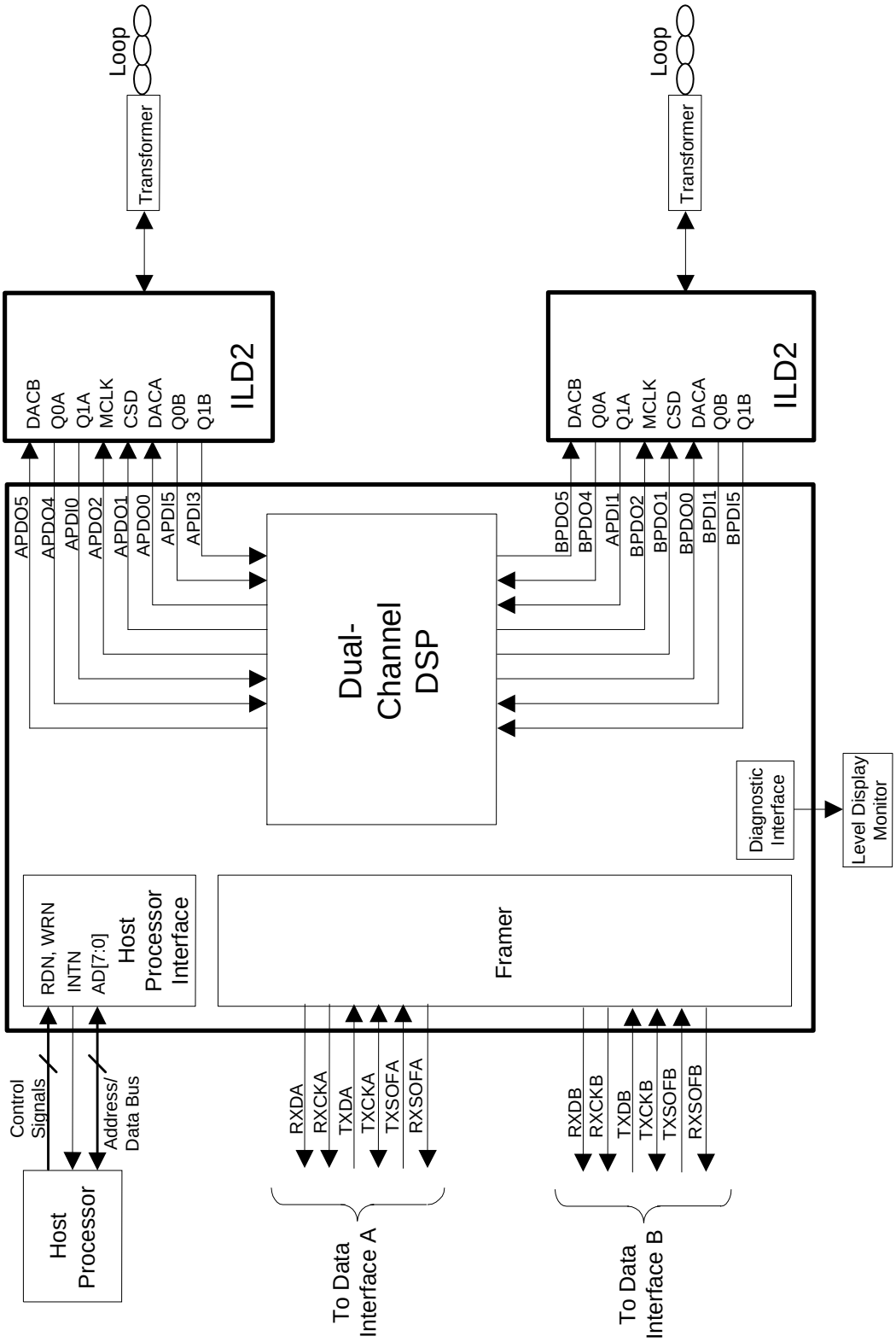


Figure 3. XDSL2™ Dual-Channel DSP with Integrated Line Driver Functional Diagram

Dual-Channel DSP/Framer Specifications

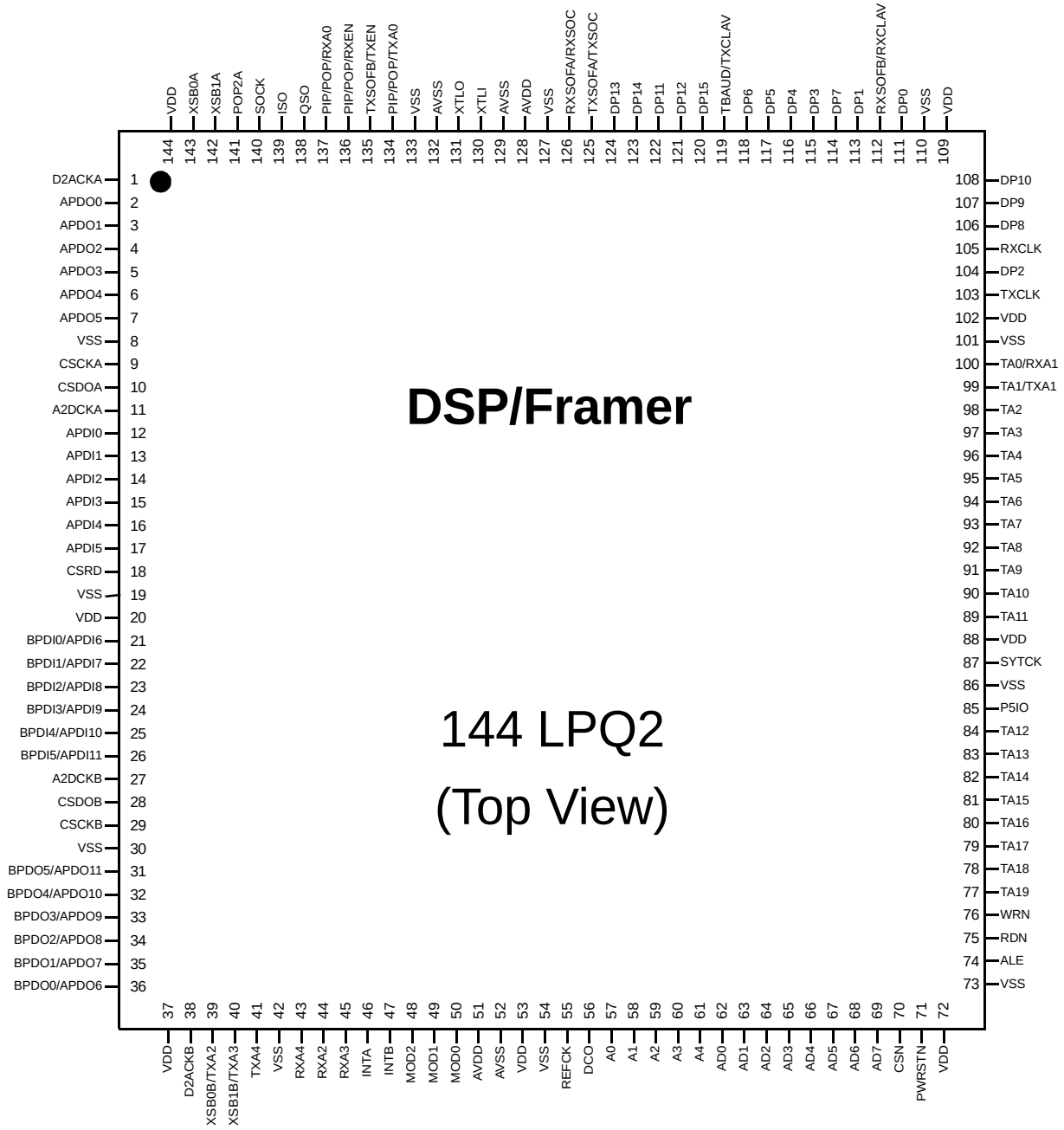


Figure 4. 144-Pin Dual-Channel DSP/Framer Pin Diagram

Table 12. 144-Pin Dual-Channel DSP/Framer Signal Descriptions

Pin	Name(s)	Mode(s)	Functional Description
1	D2ACKA	I/O	**Not used for this application.** Per application schematic, do not connect.
2	APDO0	O	**Data Out, Channel A.** Data transmitted to ILD2 from DSP/Framer. Connected to ILD2 pin DACA for channel A.
3	APDO1	O	**Control Output, Channel A.** Control signal transmitted to ILD2 from DSP/Framer. Connected to ILD2 pin CSD for channel A.
4	APDO2	O	**Master Clock to ILD2, Channel A.** Input to AFE PLL which generates oversampling clocks. Connected to ILD2 pin MCLK for channel A.
5	APDO3	O	**Not used for this application.** Per application schematic, do not connect.
6	APDO4	I	**Data In, Channel A.** Data transmitted to DSP/Framer from ILD2. Connected to ILD2 pin Q0A for channel A.
7	APDO5	O	**Data Out, Channel A.** Data transmitted to ILD2 from DSP/Framer. Connected to ILD2 pin DACB for channel A.
8	VSS	—	**Ground.**
9	CSCKA	O	**Not used for Revision "B2" DSP/Framer applications.** Per application schematic, do not connect.
		I	**TMS.** Boundary-scan mode select. Applicable to Revision "C1" DSP/Framer applications only, for JTAG support.
10	CSDOA	O	**Not used for this application.** Per application schematic, do not connect.
11	A2DCKA	I/O	**Not used for this application.** Per application schematic, do not connect.
12	APDI0	I	**Data In, Channel A.** Data transmitted to DSP/Framer from ILD2. Connected to ILD2 pin Q1A for channel A.
13	APDI1	I	**Data In, Channel B.** Data transmitted to DSP/Framer from ILD2. Connected to ILD2 pin Q1A for channel B.
14	APDI2	I	**Not used for this application.** Per application schematic, pulled low through a 1kΩ resistor to ground.
15	APDI3	I	**Data In, Channel A.** Data transmitted to DSP/Framer from ILD2. Connected to ILD2 pin Q1B for channel A.
16	APDI4	I	**Not used for this application.** Per application schematic, pulled low through a 1kΩ resistor to ground.
17	APDI5	I	**Data In, Channel A.** Data transmitted to DSP/Framer from ILD2. Connected to ILD2 pin Q0B for channel A.
18	CSRD	I	**Not used for Revision "B2" DSP/Framer applications.** Per application schematic, pulled low through a 1kΩ resistor to ground. **TDI.** Boundary-scan data in. Applicable to Revision "C1" DSP/Framer applications only, for JTAG support.
19	VSS	—	**Ground.**
20	VDD	P	**+3.3V supply.**
21	BPDI0/APDI6	I	**Not used for this application.** Per application schematic, pulled low through a 1kΩ resistor to ground.
22	BPDI1/APDI7	I	**Data In, Channel B.** Data transmitted to DSP/Framer from ILD2. Connected to ILD2 pin Q0B for channel B.
23 **24** **25**	BPDI2/APDI8 BPDI3/APDI9 BPDI4/APDI10	I	**Not used for this application.** Per application schematic, pulled low through a 1kΩ resistor to ground.
26	BPDI5/APDI11	I	**Data In, Channel B.** Data transmitted to DSP/Framer from ILD2. Connected to ILD2 pin Q1B for channel B.
27	A2DCKB	I/O	**Not used for this application.** Per application schematic, do not connect.
28	CSDOB	O	**Not used for this application.** Per application schematic, do not connect.
29	CSCKB	O	**Not used for Revision "B2" DSP/Framer applications.** Per application schematic, do not connect. **TDO.** Boundary-scan data out. Applicable to Revision "C1" DSP/Framer applications only, for JTAG support.
30	VSS	—	**Ground.**
31	BPDO5/APDO11	O	**Data Out, Channel B.** Data transmitted to ILD2 from DSP/Framer. Connected to ILD2 pin DACB for channel B.
32	BPDO4/APDO10	I	**Data In, Channel B.** Data transmitted to DSP/Framer from ILD2. Connected to ILD2 pin Q0A for channel B.
33	BPDO3/APDO9	O	**Not used for this application.** Per application schematic, do not connect.

Table 12. 144-Pin Dual-Channel DSP/Framer Signal Descriptions

Pin	Name(s)	Mode(s)		Functional Description
34	BPDO2/APDO8	O		**Master Clock to ILD2, Channel B.** Input to AFE PLL which generates oversampling clocks. Connected to ILD2 pin MCLK for channel B.
35	BPDO1/APDO7	O		**Control Output, Channel B.** Control signal transmitted to ILD2 from DSP/Framer. Connected to ILD2 pin CSD for channel B.
36	BPDO0/APDO6	O		**Data Out, Channel B.** Data transmitted to ILD2 from DSP/Framer. Connected to ILD2 pin DACA for channel B.
37	VDD	P		**+3.3V supply.**
38	D2ACKB	O		**Not used for this application.** Per application schematic, do not connect.
39	XSB0B/TXA2	SERIAL	I/O	**No Connect.** For serial interface applications, this pin is used for debug purposes only.
		UTOPIA	I/O	**TXA2- ATM UTOPIA Level 2 Transmit Address.** (I) Driven by the ATM to PHY layer to select the appropriate PHY device and port. Not used for ATM UTOPIA Level 1 applications, internally configured as output.
40	XSB1B/TXA3	SERIAL	I/O	**No Connect.** For serial interface applications, this pin is used for debug purposes only.
		UTOPIA	I/O	**TXA3- ATM UTOPIA Level 2 Transmit Address.** (I) Driven by the ATM to PHY layer to select the appropriate PHY device and port. Not used for ATM UTOPIA Level 1 applications, internally configured as output.
41	TXA4	SERIAL	I/O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	I/O	**TXA4- ATM UTOPIA Level 2 Transmit Address.** (I) Driven by the ATM to PHY layer to select the appropriate PHY device and port. Not used for ATM UTOPIA Level 1 applications, internally configured as output.
42	VSS	—		**Ground**.
43 **44** **45**	RXA4 RXA2 RXA3	SERIAL	I/O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	I/O	**ATM UTOPIA Level 2 Receive Address.** (I) Driven by the ATM to PHY layer to select the appropriate PHY device and port. Not used for ATM UTOPIA Level 1 applications, internally configured as output.
46	INTA	O		**Interrupt of DSP A.** Carries interrupts from internal DSP core A. The polarity of the interrupt level is programmable with default to inactive open-drain. Internally generated status can be enabled to activate the interrupt pin. Used during start-up for code downloads. INTA and INTB are both required. Both can be declared open-drain and tied together, if desired.
47	INTB	O		**Interrupt of DSP B.** Carries interrupts from internal DSP core B and framer. The polarity of the interrupt level is programmable with default to inactive open-drain. Internally generated status can be enabled to activate the interrupt pin. Used during start-up for code downloads and EOC interrupts in data mode. INTA and INTB are both required. Both can be declared open-drain and tied together, if desired.
48 **49** **50**	MOD2 MOD1 MOD0	I		**Host Bus Mode.** Bits 2 through 0. These input pins define the host bus control modes: 000 = Non-multiplexed processor mode 001 = Motorola mode where RDN is R/W and WRN is DSN 01X = reserved for testing 100 = Multiplexed processor mode 101 = reserved for testing.
51	AVDD	P		**AVDD.** Digital +3.3V supply for VCO.
52	AVSS	—		**AVSS.** Ground pin for VCO. Connect to digital ground as per schematic.
53	VDD	P		**+3.3V supply.**
54	VSS	—		**Ground.**
55	REFCK	I/O		**Reference Clock.** Used to pass network timing reference.
56	DCO	I/O		**DCO.** Pull up as per application schematic.
57 **58** **59** **60** **61**	A0 A1 A2 A3 A4	I		**Address Bus**. Bits 4 through 0. Host Address bus in the non-multiplexed mode. A[4:3] are used to select between the two internal 8 byte address spaces.
62 **63** **64** **65** **66** **67** **68** **69**	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I/O		**Multiplexed Address and Data Bus.** AD[4:0] = Address inputs in multiplexed mode. See A[4:0] for usage.

Table 12. 144-Pin Dual-Channel DSP/Framer Signal Descriptions

Pin	Name(s)	Mode(s)		Functional Description
70	CSN	I		**Chip Select.** Active low in µP mode.
71	PWRSTN	I		**Power Reset Not.** Low active. DSP hardware reset that after deactivation still leaves the internal circuits in the software reset mode. In addition, all outputs are forced into high impedance mode when active. Also functions as **RSTN** for **JTAG** control for Revision "C1" DSP/Framer applications.
72	VDD	P		**+3.3V supply.**
73	VSS	—		**Ground.**
74	ALE	I		**Address Latch Enable.** In the processor mode, this pin is an input that indicates an active address cycle on the multiplexed bus.
75	RDN	I		**Read Not.** Active low read pulse. This signal enables data bus output buffers during read operations.
76	WRN	I		**Write Not.** Active low write pulse. This signal is used as a standard processor data write control signal.
77 **78** **79** **80** **81** **82** **83** **84**	TA19 TA18 TA17 TA16 TA15 TA14 TA13 TA12	I/O		**External TDM.** Not used for this application. Per application schematic, do not connect.
85	P5IO	I		**Programmable Input Pin for Revision "B2" DSP/Framer applications.** **TCK.** Boundary-scan clock. Applicable to Revision "C1" DSP/Framer applications only, for JTAG support.
86	VSS	—		**Ground.**
87	SYTCK	O		**Not used for this application.** Per application schematic, do not connect.
88	VDD	P		**3.3V supply.**
89 **90** **91** **92** **93** **94** **95** **96** **97** **98**	TA11 TA10 TA9 TA8 TA7 TA6 TA5 TA4 TA3 TA2	I/O		**External TDM.** Not used for this application. Per application schematic, do not connect.
99	TA1/TXA1	SERIAL	I/O	**Not used for this application.** Internally configured as output.
		UTOPIA	I/O	**TXA1 - ATM UTOPIA Level 2 Transmit Address.** (I) Driven by the ATM to PHY layer to select the appropriate PHY device and port. Not used for ATM UTOPIA Level 1 applications, internally configured as output.
100	TA0/RXA1	SERIAL	I/O	**Not used for this application.** Internally configured as output.
		UTOPIA	I/O	**RXA1 - ATM UTOPIA Level 2 Receive Address.** (I) Driven by the ATM to PHY layer to select the appropriate PHY device and port. Not used for ATM UTOPIA Level 1 applications, internally configured as output.
101	VSS	—		**Ground.**
102	VDD	P		**+3.3V supply.**
103	TXCLK	SERIAL	I/O	**TXCKA - Transmit clock for channel A.** Framed = I; unframed = O.
		UTOPIA	I	**TXCLK - ATM UTOPIA Level 1 and 2 Transmit Clock.** Synchronizes all signal transfers from the ATM to the PHY device.
104	DP2	SERIAL	I/O	**TXCKB - Transmit clock for channel B.** Framed = I; unframed = O.
		UTOPIA	I	**TXDT2 - ATM UTOPIA Level 1 and 2 Transmit Data.** Byte-Wide True Data from the ATM to the PHY device.
105	RXCLK	SERIAL	O	**RXCKA - Receive clock for channel A.**
		UTOPIA	I	**RXCLK - ATM UTOPIA Level 1 and 2 Receive Clock.** Synchronizes all signal transfers from the ATM to the PHY device.
106	DP8	SERIAL	O	**RXDA - Receive serial data for channel A.**
		UTOPIA	O	**RXDT0 - ATM UTOPIA Level 1 and 2 Receive Data.** Byte-Wide True Data from the PHY to the ATM device.

Table 12. 144-Pin Dual-Channel DSP/Framer Signal Descriptions

Pin	Name(s)	Mode(s)		Functional Description
107	DP9	SERIAL	O	**RXDB - Receive serial data for channel B.**
		UTOPIA	O	**RXDT1 - ATM UTOPIA Level 1 and 2 Receive Data.** Byte-Wide True Data from the PHY to the ATM device.
108	DP10	SERIAL	O	**RXCKB - Receive clock for channel B.** This pin is the same as BRXCK for applications bypassing the on-chip framer.
		UTOPIA	O	**RXDT2 - ATM UTOPIA Level 1 and 2 Receive Data.** Byte-Wide True Data from the PHY to the ATM device.
109	VDD	P		**+3.3V supply.**
110	VSS	—		**Ground.**
111	DP0	SERIAL	I	**TXDA - Serial transmit data for channel A.**
		UTOPIA	I	**TXDT0 - ATM UTOPIA Level 1 and 2 Transmit Data.** Byte-Wide True Data from the ATM to the PHY device.
112	RXSOFB/RXCLAV	SERIAL	O	**RXSOFB - Receive start of frame for channel B.**
		UTOPIA	O	**RXCLAV - ATM UTOPIA Level 1 and 2 Receive Cell Available Signal.** Used by the PHY layer device to indicate that the receive buffer has a new cell.
113	DP1	SERIAL	I	**TXDB - Serial transmit data for channel B.**
		UTOPIA	I	**TXDT1 - ATM UTOPIA Level 1 and 2 Transmit Data.** Byte-Wide True Data from the ATM to the PHY device.
114	DP7	SERIAL	I/O	**Not used for this application.** Internally configured as output.
		UTOPIA	I	**TXDT7 - ATM UTOPIA Level 1 and 2 Transmit Data.** Byte-Wide True Data from the ATM to the PHY device.
115	DP3	SERIAL	I/O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	I	**TXDT3 - ATM UTOPIA Level 1 and 2 Transmit Data.** Byte-Wide True Data from the ATM to the PHY device.
116	DP4	SERIAL	I/O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	I	**TXDT4 - ATM UTOPIA Level 1 and 2 Transmit Data.** Byte-Wide True Data from the ATM to the PHY device.
117	DP5	SERIAL	I/O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	I	**TXDT5 - ATM UTOPIA Level 1 and 2 Transmit Data.** Byte-Wide True Data from the ATM to the PHY device.
118	DP6	SERIAL	I/O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	I	**TXDT6 - ATM UTOPIA Level 1 and 2 Transmit Data.** Byte-Wide True Data from the ATM to the PHY device.
119	TBAUD/TXCLAV	SERIAL	I/O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	O	**TXCLAV - ATM UTOPIA Level 1 and 2 Transmit Cell Available Signal.** Used by the PHY layer device to indicate that there is space available for a new cell.
120	DP15	SERIAL	I/O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	O	**RXDT7 - ATM UTOPIA Level 1 and 2 Receive Data.** Byte-Wide True Data from the PHY to the ATM device.
121	DP12	SERIAL	I/O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	O	**RXDT4 - ATM UTOPIA Level 1 and 2 Receive Data.** Byte-Wide True Data from the PHY to the ATM device.
122	DP11	SERIAL	I/O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	O	**RXDT3 - ATM UTOPIA Level 1 and 2 Receive Data.** Byte-Wide True Data from the PHY to the ATM device.
123	DP14	SERIAL	I/O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	O	**RXDT6 - ATM UTOPIA Level 1 and 2 Receive Data.** Byte-Wide True Data from the PHY to the ATM device.
124	DP13	SERIAL	O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	O	**RXDT5 - ATM UTOPIA Level 1 and 2 Receive Data.** Byte-Wide True Data from the PHY to the ATM device.
125	TXSOFA/TXSOC	SERIAL	I	**TXSOFA - Transmit Start of frame for channel A.**
		UTOPIA	I	**TXSOC - ATM UTOPIA Level 1 and 2 Transmit Start of Cell** (active high). This bit is true on the first byte of the transmitted cell from the ATM to the PHY.

Table 12. 144-Pin Dual-Channel DSP/Framer Signal Descriptions

Pin	Name(s)	Mode(s)		Functional Description
126	RXSOFA/RXSOC	SERIAL	O	**RXSOFA - Receive Start of frame for channel A**.
		UTOPIA	O	**RXSOC - ATM UTOPIA Level 1 and 2 Receive Start of Cell** (active high). This bit is true on the first byte of the transmitted cell from the PHY to the ATM.
127	VSS	—		**Ground.**
128	AVDD	P		**AVDD.** Digital +3.3V supply for VCO.
129	AVSS	—		**AVSS.** Ground pin for VCO. Connect to digital ground as per schematic.
130	XTLI	I		**Crystal Oscillator Input.** Oscillator input. It accepts a free running external clock at subrate of the internal VCO/PLL (see board recommendations).
131	XTLO	O		**Crystal Oscillator Output.** Connects to one crystal terminal and capacitor.
132	AVSS	—		**AVSS.** Ground pin for VCO. Connect to digital ground as per schematic.
133	VSS	—		**Ground.**
134	PIP/POP/TXA0	SERIAL	I/O	**Not used for this application.** Per application schematic, do not connect.
		UTOPIA	I/O	**TXA0 - ATM UTOPIA Level 2 Transmit Address.** (I) Driven by the ATM to PHY layer to select the appropriate PHY device and port. Not used for ATM UTOPIA Level 1 applications, internally configured as output.
135	TXSOFB/TXEN	SERIAL	I	**TXSOFB - Transmit Start of Frame for channel B.**
		UTOPIA	I	**TXEN - ATM UTOPIA Level 1 and 2 Transmit Enable** (active low). The ATM layer device uses this pin to throttle the rate at the octet boundary.
136	PIP/POP/RXEN	SERIAL	I	**Not used for this application.** Terminate with a pull-up resistor.
		UTOPIA	I	**RXEN - Receive Enable** (active low). The ATM layer device uses this pin to throttle the rate at the octet boundary.
137	PIP/POP/RXA0	SERIAL	I/O	**Not used for this application.** Internally configured as output.
		UTOPIA	I/O	**RXA0 - ATM UTOPIA Level 2 Receive Address.** (I) Driven by the ATM to PHY layer to select the appropriate PHY device and port. Not used for ATM UTOPIA Level 1 applications, internally configured as output.
138	QSO	O		**2B1Q and PAM: QSOA, QSOB - Level Display 2 Serial Data Output.** Serial data for level display 2. Data format the same as ISO.
				CAP: QSOA, QSOB - Quadrature Serial Output. Quadrature constellation display serial output. Data format the same as ISO.
139	ISO	O		**2B1Q and PAM: ISOA, ISOB - Level Display 1 Serial Data Output.** Serial data for level display 1. Data format is asynchronous with 12 bits of data and start and stop bits.
				CAP: ISOA, ISOB - In-phase Serial Output. In-phase constellation display serial output. Data format is asynchronous with 12 bits of data and start and stop bits.
140	SOCK	O		**2B1Q and PAM: Serial Data Clock.** For ISO and QSO data outputs.
				CAP: Serial Data Clock. For ISO and QSO constellation data outputs.
141	POP2A	O		**POP2A** - Configured as a programmable output after power-up for Channel A.
142	XSB1A	O		**External Strobe1 of DSP A.** One of two strobes from the DSP that are synchronized with the internal signal processing clock.
143	XSB0A	O		**External Strobe0 of DSP A.** One of two strobes from the DSP that are synchronized with the internal signal processing clock.
144	VDD	P		**+3.3V supply.**

Boundary-Scan Testing

Four pins are provided for compliance to IEEE Standard 1149.1 (JTAG) for boundary scan testing. These DSP pins are used to control and communicate with the boundary-scan logic. JTAG support is available only in Revision “C1” of the DSP/Framer. Table 13 provides a list of the four JTAG pins:

Table 13. Boundary-Scan Pins

144-Pin DSP/Framer Revision “C1” Pin #	JTAG Description
9	TMS - Test Mode Select
18	TDI - Test Data Input
29	TDO - Test Data Output
85	TCK - Test Clock

Table 14. Dual-Channel DSP/Framer Electrical Characteristics

Parameters	Min	Nom	Max	Unit	Test Conditions/Comments
Absolute Maximum Ratings					
Power Supply Voltage, V_{DD}	—	—	3.6	V	
Power Supply Voltage, AV_{DD}	—	—	3.6	V	
Input Voltage	GND – 0.3	—	5.5	V	
Storage Temperature	–40	—	125	℃	
Junction Temperature	—	—	125	℃	
Recommended Operating Conditions					
Power Supply Voltage, V_{DD}	3.13	3.3	3.47	V	
Power Supply Voltage, AV_{DD}	2.75	3.3	3.47	V	
Input Voltage	GND – 0.3	3.3	5.5	V	
Operating Temperature	–40	25	85	℃	
Digital Specifications					
I/O Levels	TTL and/or CMOS compatible				
Digital Inputs					
Input Low Voltage, V_{IL}	–0.3	0	0.8	V	For all inputs except XTLI. For XTLI, the maximum V_{IL} is VDD/2.
Input High Voltage, V_{IH}	2.0	3.3	5.25	V	
Digital Outputs					
Output Low Voltage, V_{OL}	—	0	0.4	V	Current sink, I_{OL}, ≤ 3.5 mA
Output High Voltage, V_{OH} for Rev. B2 of the DSP	2.4	3.3	—	V	Current load, I_{OH}, ≤ 6 mA for all pins
Output High Voltage, V_{OH} for Rev. C1 of the DSP	2.4	3.3	—	V	Current load, I_{OH}, ≤ 6 mA for all non-UTOPIA pins Current load, I_{OH}, ≤ 10 mA for all UTOPIA pins
DC Specifications					
Input Leakage Current, I_{LI}	10	—	—	µA	Input voltage, V_I, between 0 volts and V_{DD}
High-Z Leakage Current, I_{LO}	10	—	—	µA	Output voltage, V_O, between 0 volts and V_{DD}
Input Capacitance, C_{IN} (f_c = 1 MHz)	—	6	—	pF	
I/O Capacitance, C_{IO} (f_c = 1 MHz)	—	10	—	pF	

Note: All of the following pins are 5V tolerant:

All Input (I) signal pins except XTLI

All Input/Output (I/O) signal pins

No Output (O) signal pins except INTA, INTB, and POP2A

Table 15. Clock Specifications for XTLI Pin

Timing Parameters			Voltage	
Duty Cycle	**Rise Time Maximum (nsec)**	**Fall Time Maximum (nsec)**	**Overshoot Maximum**	**Undershoot Maximum**
40 - 60%	4	4	3.3V + 5%	100 mV below ground

Note the following layout guidelines:

1. We recommend not more than 4 DSPs per clock source.
2. The clock source distribution network should be routed in a star pattern ensuring equal distances to all DSPs.
3. Place a series termination resistor as close to the clock source as possible.
4. Refer to the “Critical Clock and Signal Layout Guidelines” section in Chapter 3 of the Design Guide for further information.

Customer Data Interface

The customer data interface includes data signals, control signals, and address signals. The GlobespanVirata 144-pin DSP has an on-chip programmable framer for handling multiple TC layer framing formats. The supported, software selectable, framing formats include Serial Mode and Asynchronous Transfer Mode (ATM) UTOPIA Level 1 and Level 2. Please note only one UTOPIA Level 1 interface is supported per dual channel DSP/Framer. Table 16 lists corresponding pins for both Serial and UTOPIA Modes.

Table 16. 144-Pin DSP Data Interface Pin Usage

Pin Name	Pin Number	UTOPIA Mode		Serial Mode	
DP0	111	I	TXDT0	I	TXDA
DP1	113	I	TXDT1	I	TXDB
DP2	104	I	TXDT2	I/O	TXCKB
DP3	115	I	TXDT3	I/O	Not used
DP4	116	I	TXDT4	I/O	Not used
DP5	117	I	TXDT5	I/O	Not used
DP6	118	I	TXDT6	I/O	Not used
DP7	114	I	TXDT7	I/O	Not used
DP8	106	O	RXDT0	O	RXDA
DP9	107	O	RXDT1	O	RXDB
DP10	108	O	RXDT2	O	RXCKB
DP11	122	O	RXDT3	I/O	Not used
DP12	121	O	RXDT4	I/O	Not used
DP13	124	O	RXDT5	O	Not used
DP14	123	O	RXDT6	I/O	Not used
DP15	120	O	RXDT7	I/O	Not used
TXCLK	103	I	TXCLK	I/O	TXCKA
TXSOFA/TXSOC	125	I	TXSOC	I	TXSOFA
TBAUD/TXCLAV	119	O	TXCLAV	I/O	Not used
RXCLK	105	I	RXCLK	O	RXCKA
RXSOFA/RXSOC	126	O	RXSOC	O	RXSOFA
RXSOFB/RXCLAV	112	O	RXCLAV	O	RXSOFB
PIP/POP/TXA0	134	I	TXA0*	I/O	Not used
TA1/TXA1	99	I	TXA1*	I/O	Not used
XSB0B/TXA2	39	I	TXA2*	I/O	Not used
XSB1B/TXA3	40	I	TXA3*	I/O	Not used
TXA4	41	I	TXA4*	I/O	Not used
PIP/POP/RXA0	137	I	RXA0*	I/O	Not used
TA0/RXA1	100	I	RXA1*	I/O	Not used
RXA2	44	I	RXA2*	I/O	Not used
RXA3	45	I	RXA3*	I/O	Not used
RXA4	43	I	RXA4*	I/O	Not used
TXSOFB/TXEN	135	I	TXEN	I	TXSOFB
PIP/POP/RXEN	136	I	RXEN	I	Not used

* Not used for UTOPIA Level 1 applications.

ATM UTOPIA Level 1 and Level 2

Figure 5 and Figure 6 detail the interface for standard ATM UTOPIA Level 1 and Level 2. Dual-channel ATM over UTOPIA Level 2 or single-channel ATM over UTOPIA Level 1 is supported for SHDSL, SDSL 2B1Q, and HDSL2.

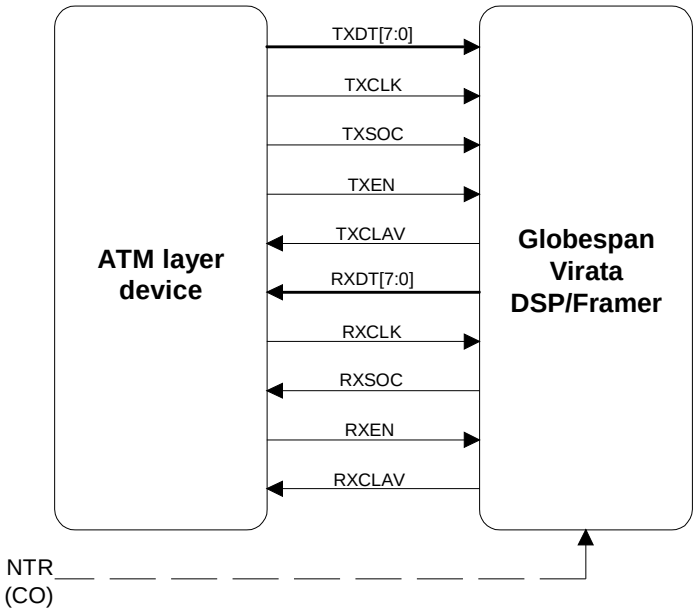
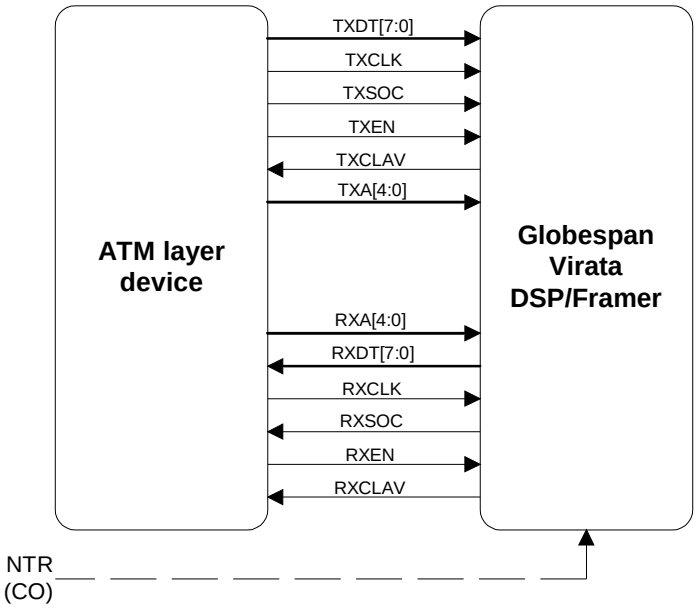


Figure 5. UTOPIA Level 1 Signals



NOTE: RXSOC, RXCLAV, and TXCLAV are tri-state active high signals and need appropriate pull-down terminations.

Figure 6. UTOPIA Level 2 Signals

Transmit, receive, and tri-state timing is shown in Figure 7, Figure 8, and Figure 9. Timing parameters are shown in Table 17.

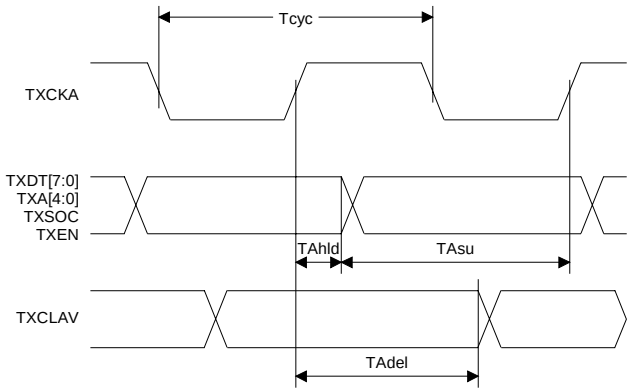


Figure 7. Transmit ATM Timing

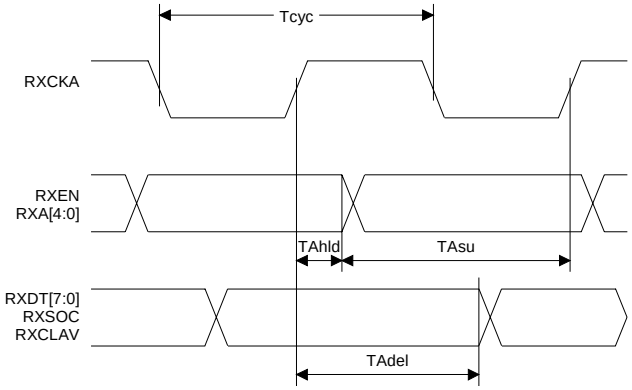


Figure 8. Receive ATM Timing

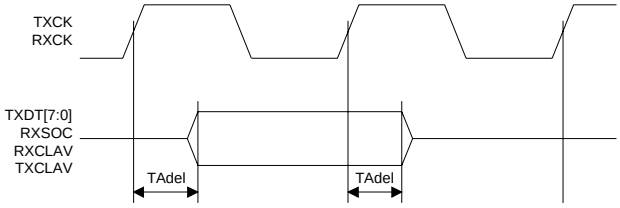


Figure 9. Tri-State ATM Timing

Table 17. ATM Timing Parameters

Specifi-cation	Description	Min	Max
Tcyc	Clock Period	40 ns	
TAsu	Input Setup to Clock Rising Edge	4 ns	
TAhld	Input Hold from Clock Rising Edge	1 ns	
TAdel	Output Delay from Clock Rising Edge		15 ns

Supported Serial Interfaces

The following serial interfaces are supported per application:

SHDSL: Dual or single-channel Slotted E1, Slotted T1, and Nx64 Interfaces (refer to the SHDSL Design Guide, GSDG-0014, for a detailed description).

HDSL2: Single-channel Fixed T1 Interface (refer to the HDSL2 Design Guide, GSDG-0013, for a detailed description).

SDSL CAP: Single-channel Slotted E1, Slotted T1, and Nx64 Interfaces (refer to the SDSL CAP Design Guide, GSDG-0012 for a detailed description). Dual-channel supported in unframed mode only (no physical layer framing).

Table 18. Summary of Transceiver Serial Interface Leads

Name	Type CO/Framer	Type CO/Framer Bypass	Type CP/Framer	Type CP/Framer Bypass	Description
Transmission Interface					
TXD[A,B]	I	I	I	I	Transmit Data for channels A and B
TXCK[A,B]	I	O	I	O	Transmit Bit Clock for channels A and B (see **NOTE**)
RXD[A,B]	O	O	O	O	Receive Data for channels A and B
RXCK[A,B]	O	O	O	O	Receive Bit Clock for channels A and B (see **NOTE**)
TXSOF[A,B]	I	N/C	I	N/C	Transmit start of Frame for channels A and B
RXSOF[A,B]	O	N/C	O	N/C	Receive start of Frame for channels A and B

NOTE:

Each **Type** field shows the directional flow for the CO/CP with Framer, or CO/CP without the integrated Framer (Bypass mode) from the view of the DSP/Framer.
Figure 10 and Figure 11 depict the directions of the framed and unframed serial data/clock interfaces.

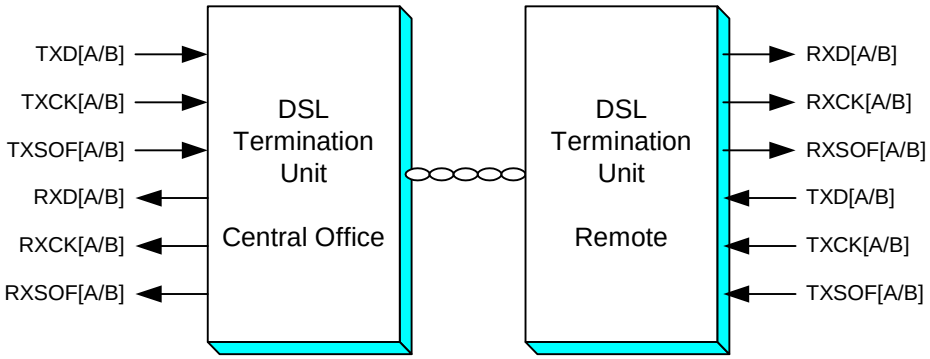


Figure 10. *Framed Serial Data/Clock Interface

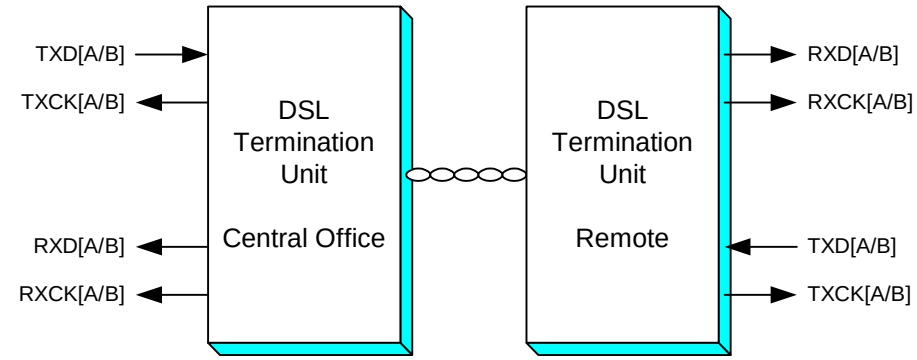
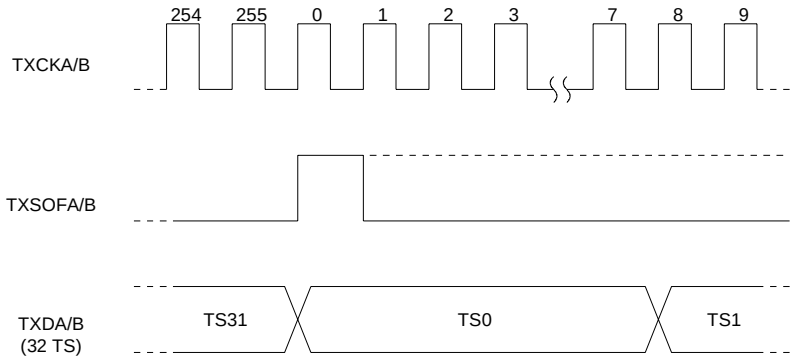


Figure 11. *Unframed (Framer Bypass Mode) Serial Data/Clock Interface.

* Note that TX and RX clocks must have the same frequency at both the CO and CPE.

The relationship between the data and the Start Of Frame signal (SOF) to the clock pulse is illustrated below. Figure 12 and Figure 13 depict E1, which has sync byte in time slot 0. Figure 14 and Figure 15 depict T1, which has an F-bit signifying the start of time slot 0. For unframed mode, the SOF is not applicable. Figure 16 and Figure 17 depict Nx64 operation.



NOTE: The transmit start of frame pulse (TXSOFA/B) must be low for at least 8 clock cycles.

Figure 12. Transmit Slotted E1 Interface Timing

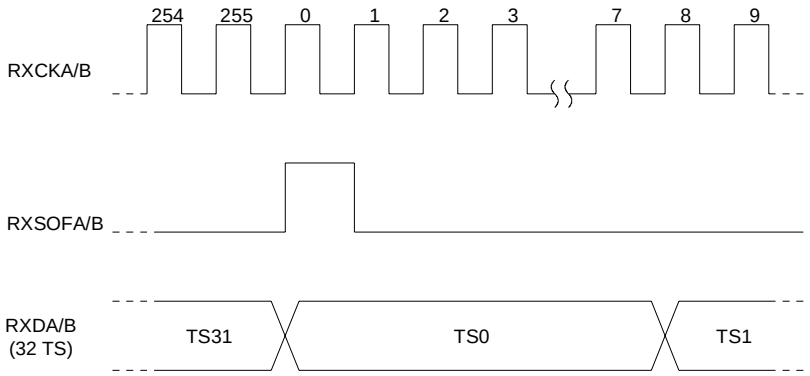


Figure 13. Receive Slotted E1 Interface Timing

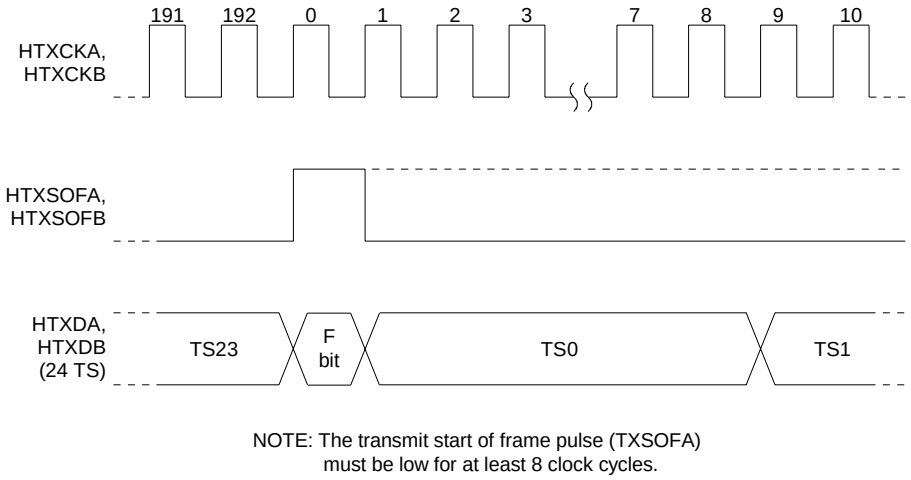


Figure 14. T1 Interface Transmit Timing for HDSL2

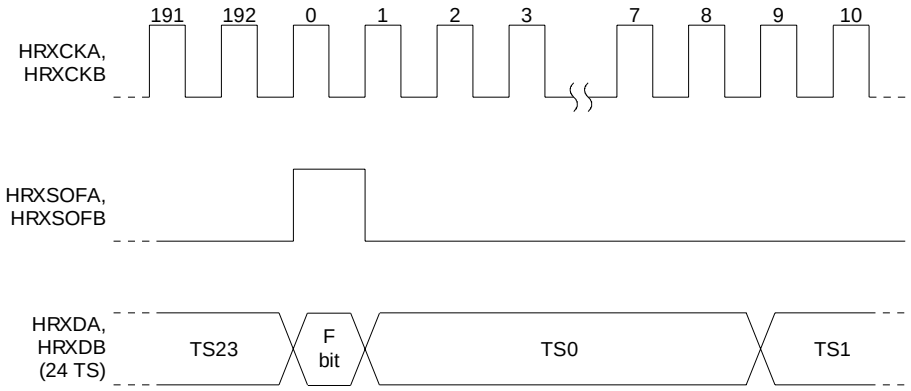


Figure 15. T1 Interface Receive Timing for HDSL2

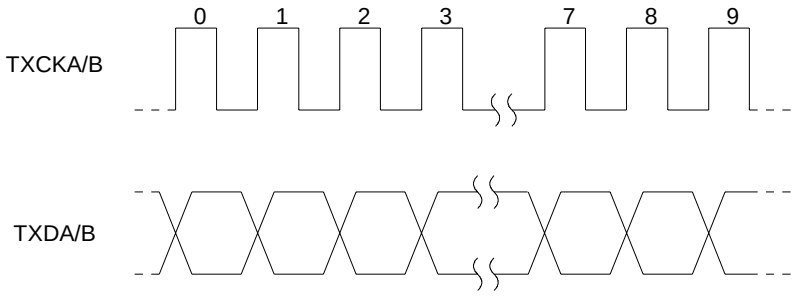


Figure 16. Transmit Nx64 Interface Timing

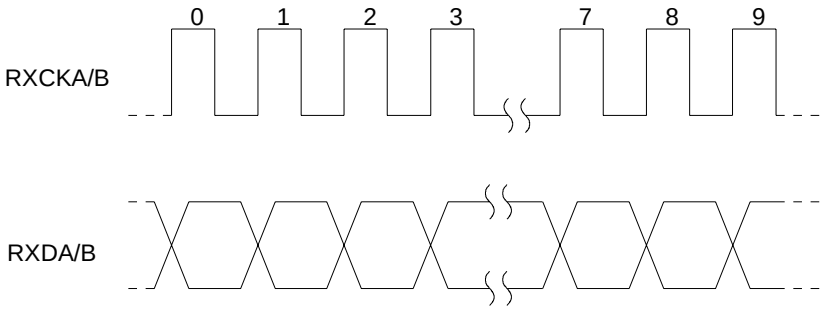


Figure 17. Receive Nx64 Interface Timing

Figure 18 and Figure 19 show serial transmit and receive timing. This timing applies to all products (SDSL, HDSL2, and SHDSL - ILD2).

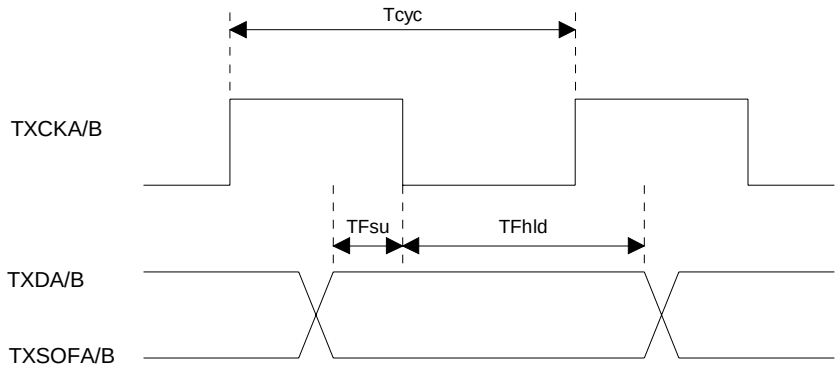


Figure 18. Serial Transmit Timing

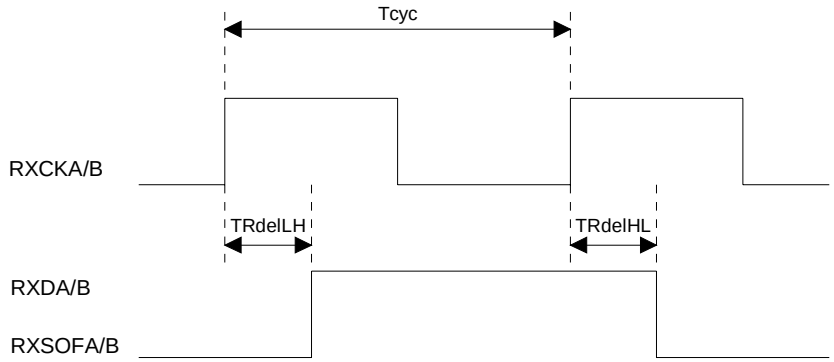


Figure 19. Serial Receive Timing

Table 19. Serial Timing Parameters

Specification	Description	Min	Max
Tcyc	Clock Period	50 ns	
TFsu	Input Setup to Clock Falling Edge	10 ns	
TFhld	Input Hold from Clock Falling Edge	5 ns	
TRdelLH	Output Delay From Low to High		20 ns
TRdelHL	Output Delay From High to Low		20 ns

Input Timing Parameters

Specifications are defined in terms of setup and hold times of the data inputs relative to a reference clock.

Table 20. Input Timing Parameters

Input Signal	Pin	Edge	Setup (nsec)	Hold (nsec)
TxDA TxDB	TXCKA (103) TXCKB (104)	+/-	10	5

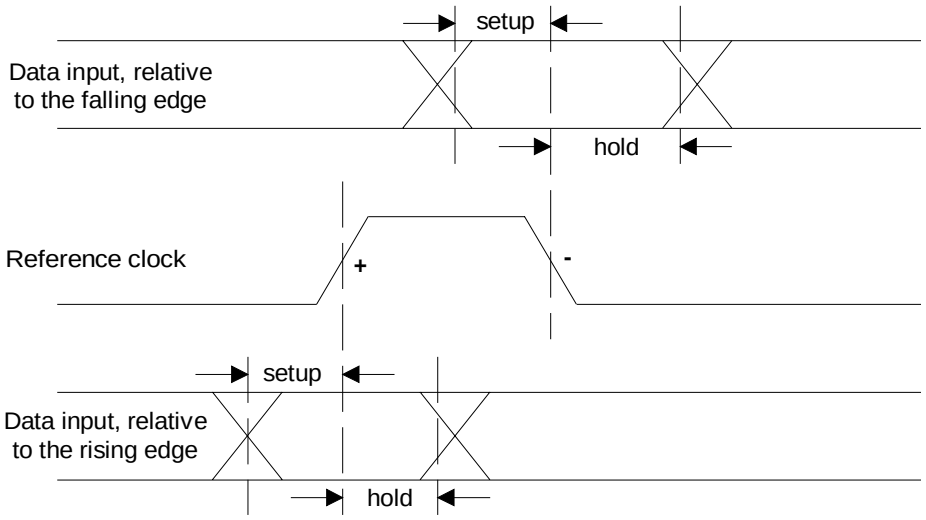


Figure 20. Input Timing Diagram

Output Timing Parameters

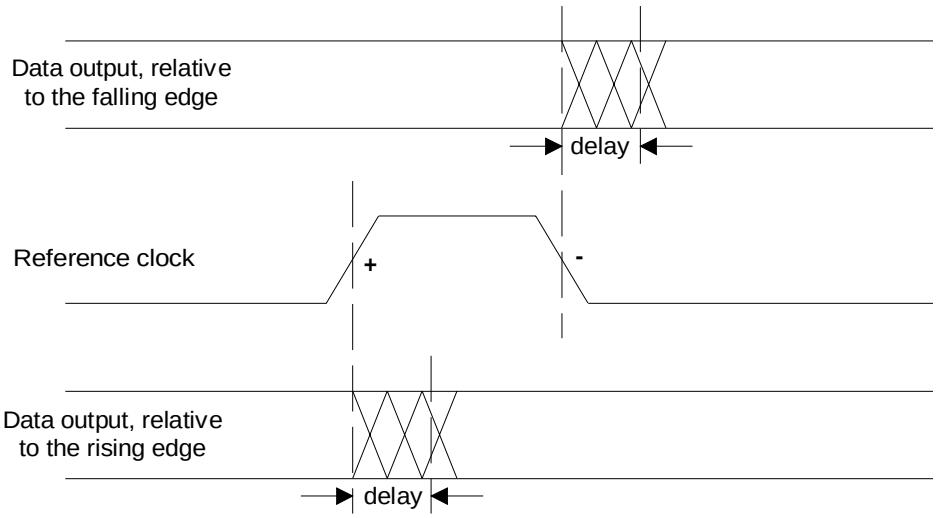
Specifications are defined in terms of propagation delay from a reference clock edge to the data output stable condition.

NOTE:

All loads are 35 pF, unless noted otherwise.
Add 1.5 nsec per 10 pF of additional loading.
Rise and fall times are 5 nsec.

Table 21. Output Timing Parameters

Output	Pin	Edge	Min (nsec)	Max (nsec)
All outputs to high-Z	PWRSTN (71)	+		50
RxDA RxDB	RXCKA (105) RXCKB (108)	+/-		20
ISO/QSO	SOCK (140)	+		10



This timing applies to ALL data outputs and their respective clocks

Figure 21. Output Timing Diagram

Host Processor Interfaces

GlobespanVirata chip sets easily interface with multiplexed (Intel style), generic non-multiplexed, and non-multiplexed Motorola style host processors. The MOD pins on the DSP must be set according to Table 22 for the type of processor interface required. These pins should be set (pulled high or low) using the resistor values shown in the Customer Schematics.

Table 22. MOD Settings

Processor	MOD2	MOD1	MOD0	RDN Function	WRN Function	ALE Use
Multiplexed	1	0	0	RDN	WRN	ALE
Motorola	0	0	1	RD/WRN	DSN	n/a (pulled low)
Other non-multiplexed	0	0	0	RDN	WRN	n/a (pulled low)

NOTE:

A value of 1 refers to pulled high and 0 refers to pulled low.

Table 23. Summary of Transceiver Host Interface Leads

Name	Type CO/Framer	Description
AD[0-7]	I/O	8 Bit Multiplexed Address/Data Bus
CSN	I	DSP Chip Select
ALE	I	Multiplexed Processor Address Latch Enable
WRN	I	Write Strobe
RDN	I	Read Strobe
PWRSTN	I	Power Reset Not
INTNA, INTNB	O	DSP/Framer Interrupts
MOD[2,1,0]	I	Host Bus Control Modes
A[0-4]	I	Non-multiplexed Address Bus

NOTE:

Each **Type** field shows the directional flow for the CO/CP with Framer, or CO/CP without the integrated Framer (Bypass mode) from the view of the DSP/Framer.
Figure 10 and Figure 11 depict the directions of the framed and unframed serial data/clock interfaces.

Multiplexed Bus Mode Timing Requirements and Characteristics

Table 24. Read Cycle Timing Characteristics

Parameter	Symbol	Max (ns)	Test Conditions/Comments
Address valid to data valid	tHAVDV	35	Capacitive load on HAD[7:0] is 100 pF Active HCSNA overlap with active HRDN defines the effective HRDN pulse
Read strobe active to data valid	tHRDNLDV	25	Capacitive load on HAD[7:0] is 100 pF Active HCSNA overlap with active HRDN defines the effective HRDN pulse
Bus active after read	tHRDNHDX	10	

Table 25. Read Cycle Timing Requirements

Parameter	Symbol	Min (ns)	Test Conditions/Comments
Chip select setup time before read strobe	tHCSNLHRDNL	0	Active HCSNA overlap with active HRDN defines the effective HRDN pulse
Chip select hold time after read strobe	tHRDNHHCSNH	0	Active HCSNA overlap with active HRDN defines the effective HRDN pulse
Address setup time before latch strobe low	tHAVHALEL	10	
Address hold time after latch strobe low	tHALELHAX	5	
Address latch strobe width	tHALEHHALEL	10	
Address setup time before read strobe	tHAVHRDNL	10	
Read strobe inactive before next cycle	tHRDNLHHALEH	10	
Inter-access cycle time (not shown)	tHALEHHALEH	200	The minimum time between successive reads

Table 26. Write Cycle Timing Requirements

Parameter	Symbol	Min (ns)	Test Conditions/Comments
Inter-access cycle time (not shown)	tHALELHALEL	200	The minimum time between successive writes
Chip select setup time before write strobe low	tHCSNLHWRNL	10	Active HCSNA overlap with active HWRN defines the effective HWRN pulse
Write strobe width	tHWRNLHWRNH	20	
Chip select hold time after write strobe high	tHWRNHHCSNH	0	Active HCSNA overlap with active HWRN defines the effective HWRN pulse
Address setup time before latch strobe low	tHAVHALEL	10	
Address hold time after latch strobe low	tHALELHAX	5	
Data setup time before write strobe	tHDVHWRNH	10	
Data hold time after write strobe	tHWRNHHDX	2	
Address latch strobe width	tHALEHHALEL	10	
Address setup time before write strobe	tHAVHWRNL	0	
Write strobe inactive before next cycle	tHWRNHHALEH	10	

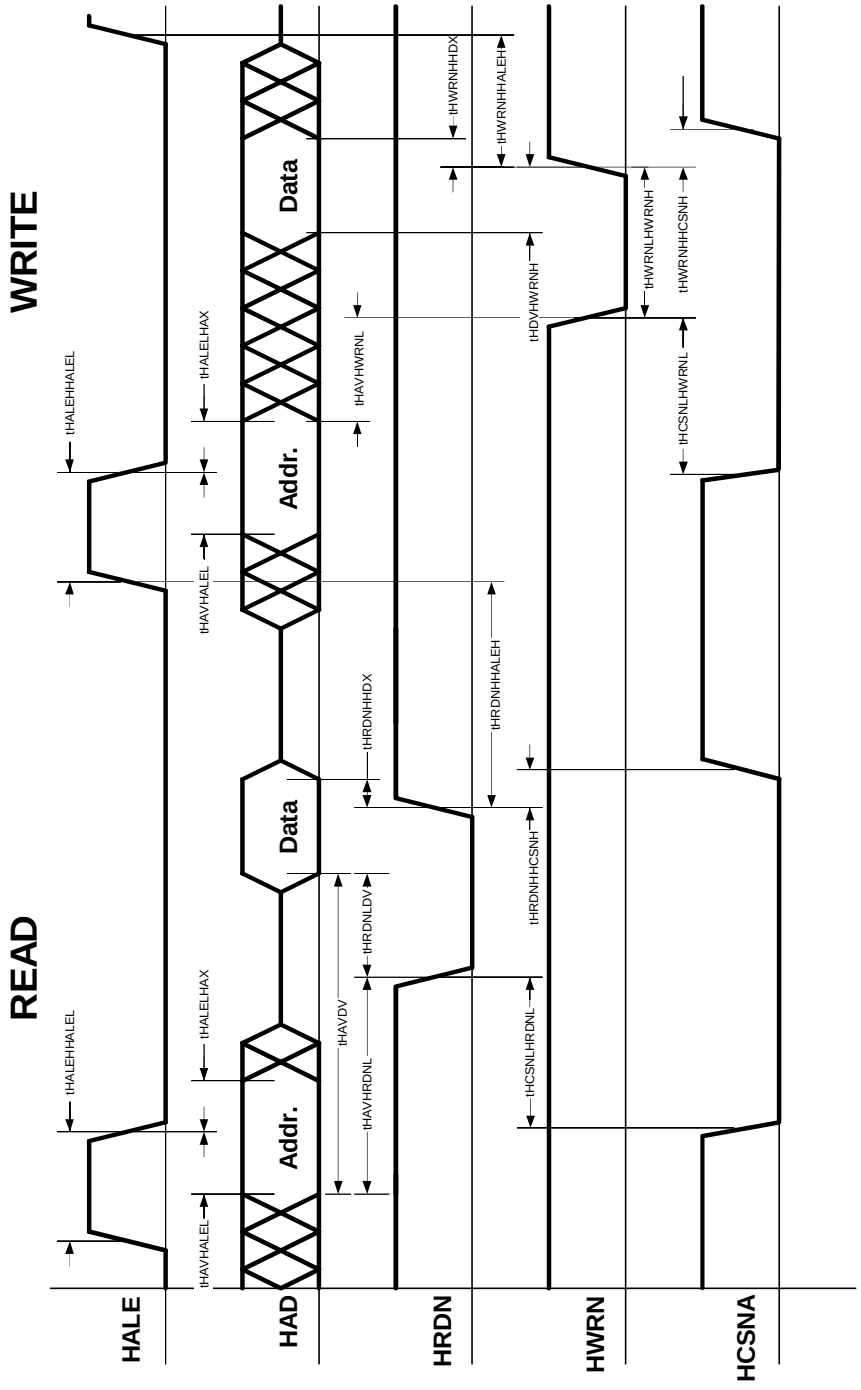


Figure 22. Multiplexed Bus Mode Timing Diagram

Non-multiplexed Bus Mode Timing Requirements and Characteristics

Table 27. Read Cycle Timing Characteristics

Parameter	Symbol	Max (ns)	Test Conditions/Comments
Address valid to data valid	tHAVHDV	35	Capacitive load on HD[7:0] is 100 pF Active HCSNA overlap with active HRDN defines the effective HRDN pulse
Read strobe active to data valid	tHRDNLHDV	25	Capacitive load on HD[7:0] is 100 pF Active HCSNA overlap with active HRDN defines the effective HRDN pulse
Bus active after read	tHRDNHHDZ	10	

Table 28. Read Cycle Timing Requirements

Parameter	Symbol	Min (ns)	Test Conditions/Comments
Chip select active before read	tHCSNLHRDNL	0	Active HCSNA overlap with active HRDN defines the effective HRDN pulse
Chip select hold time after read	tHRDNHHCSNH	0	Active HCSNA overlap with active HRDN defines the effective HRDN pulse
Address setup time before read	tHAVHRDNL	5	
Address hold time after read	tHRDNHHAX	5	
Inter-access cycle time (not shown)	tHRDNLHRDNL	200	The minimum time between successive reads

Table 29. Write Cycle Timing Requirements

Parameter	Symbol	Min (ns)	Test Conditions/Comments
Inter-access cycle time (not shown)	tHWRNLHWRNL	200	The minimum time between successive writes
Chip select setup time before write strobe low	tHCSNLHWRNL	10	Active HCSNA overlap with active HWRN defines the effective HWRN pulse
Write strobe width	tHWRNLHWRNH	20	
Chip select hold time after write	tHWRNHHCSNH	0	Active HCSNA overlap with active HWRN defines the effective HWRN pulse
Address setup time before write	tHAVHWRNL	10	
Address hold time after write	tHWRNHHAX	5	
Data setup time before write	tHDVHWRNH	10	
Data hold time after write	tHWRNHHDX	2	

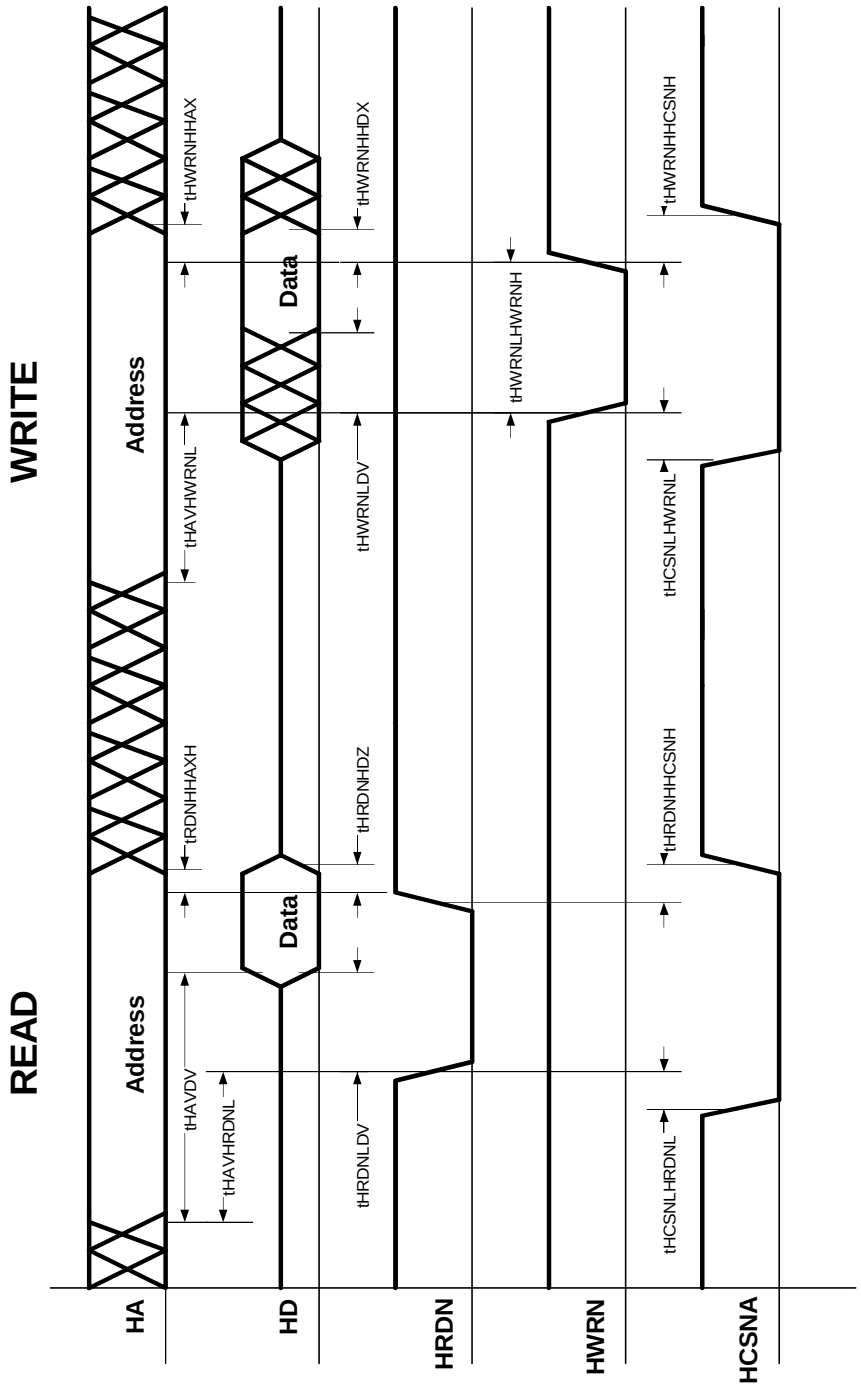


Figure 23. Non-multiplexed Bus Mode Timing Diagram

Motorola Bus Mode Timing Requirements and Characteristics

Table 30. Read Cycle Timing Characteristics

Parameter	Symbol	Min (ns)	Max (ns)	Test Conditions/Comments
Address valid to data valid	tHAVDV		20	
Data set (DSN) strobe active to data valid	tDSNLDV		10	
Bus active after data set strobe inactive	tDSNHHDX		6	

Table 31. Read Cycle Timing Requirements

Parameter	Symbol	Min (ns)	Max (ns)	Test Conditions/Comments
Inter-access cycle time (not shown)	-	200		The minimum time between successive reads
Address setup time before chip select low	tHAVHCSNL	5		
R/Wn setup before chip select low	tHRWNHHCSNL	5		
R/Wn hold time after chip select inactive	tHCSNHHRWNL	0		
Address hold time after chip select inactive	tDSNHHAX	5		
Chip select setup time before data set strobe	tHCSNLDSNL	5		
Chip select hold time after data set strobe	tDSNHHCSNH	0		

Table 32. Write Cycle Timing Requirements

Parameter	Symbol	Min (ns)	Max (ns)	Test Conditions/Comments
Inter-access cycle time (not shown)	-	200		The minimum time between successive writes
Address setup time before chip select low	tHAVHCSNL	5		
R/Wn setup before chip select low	tHRWNHHCSNL	5		
R/Wn hold time after chip select inactive	tHCSNHHRWNH	0		
Data setup time before data set strobe active	tDVDSNL	5		
Data set strobe width for write operation	tDSNLDSNH	5		
Address hold time after chip select inactive	tDSNHHAX	5		
Chip select setup time before data set strobe	tHCSNLDSNL	5		
Chip select hold time after data set strobe	tDSNHHCSNH	0		

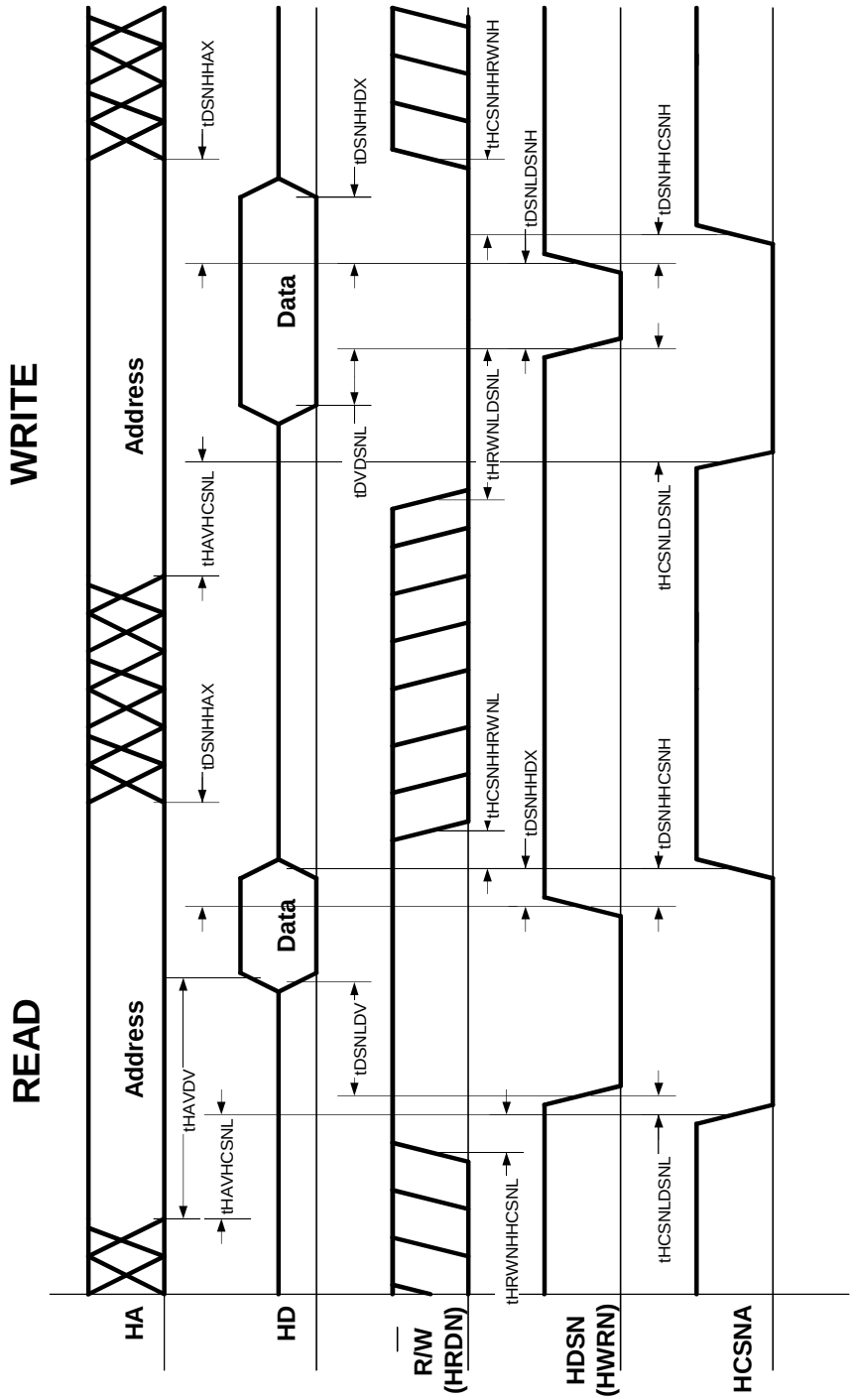


Figure 24. Motorola Bus Mode Timing Diagram

GS3137 ILD2 Specifications

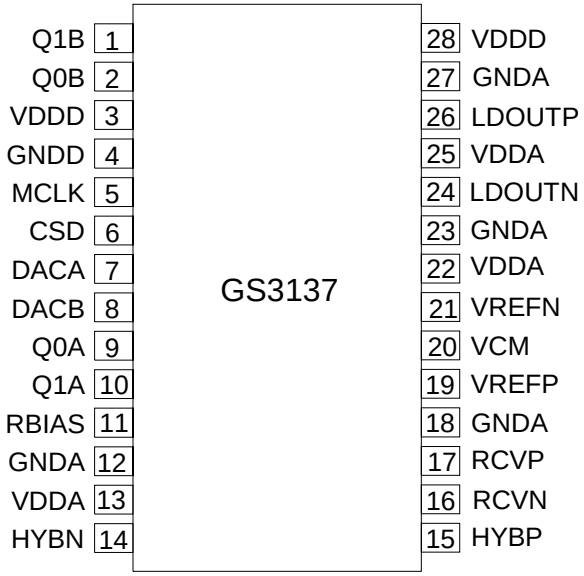


Figure 25. GS3137 28-pin ILD2 Pin Diagram

NOTE:

The EPTSSOP is required to support a transmit power of higher than 15 dbm (HDSL2 and asymmetric PSD options for SHDSL).

Table 33. GS3137 ILD2 Signal Descriptions

Pin	Symbol	Type	Name / Function
1	Q1B	O	**Data Output to DSP.**
2	Q0B	O	
3	VDDD	P	**Digital Supply.** +3.3V.
4	GNDD	P	**Digital Ground.**
5	MCLK	I	**Master Clock from DSP.** Input to PLL which generates oversampling clocks.
6	CSD	I	**Control Input from DSP.** Configures the device.
7	DACA	I	**Data Input from DSP.**
8	DACB	I	
9	Q0A	O	**Data Output to DSP.**
10	Q1A	O	
11	RBIAS	I	**External Bias Resistor Connection.**
12	GNDA	P	**Analog Ground**.
13	VDDA	P	**Analog Supply**. +5V.
14	HYBN	I	**Negative Input from Hybrid Network.** See **NOTE**.
15	HYBP	I	**Positive Input from Hybrid Network.** See **NOTE**.
16	RCVN	I	**Negative Input from Line Transformer.** See **NOTE**.
17	RCVP	I	**Positive Input from Line Transformer.** See **NOTE**.

Table 33. GS3137 ILD2 Signal Descriptions

Pin	Symbol	Type	Name / Function
18	GNDA	P	**Analog Ground**.
19	VREFP	I	**Positive Reference Voltage.**
20	VCM	I	**Common-mode Reference Voltage.**
21	VREFN	I	**Negative Reference Voltage.**
22	VDDA	P	**Analog Supply**. +5V.
23	GNDA	P	**Analog Ground**.
24	LDOUTN	O	**Negative Line Driver Output**. See **NOTE**.
25	VDDA	P	**Analog Supply**. +5V.
26	LDOUTP	O	**Positive Line Driver Output**. See **NOTE**.
27	GNDA	P	**Analog Ground**.
28	VDDD	P	**PLL Supply 3.3V.** See **NOTE**.

NOTE:

Refer to your application schematics for all application-specific pin assignments.

Table 34. GS3137 ILD2 Electrical Characteristics

Parameter	Conditions	Min	Nom	Max	Unit
Absolute Maximum Ratings					
Power Supply Voltages	5V supply			7.0	V
	3.3V supply			3.6	V
Recommended Operating Conditions					
Power Supply Voltages	5V supply	4.75	5	5.25	V
	3.3V supply	3.135	3.3	3.465	V
Operating Temperature	–	-40	–	85	℃
Digital Inputs					
Input Logic High V_{IH}	$\lvert I_{IH} \rvert$ <10µA	DV_{DD}-1	–	–	V
Input Logic Low V_{IL}	$\lvert I_{IH} \rvert$ <10µA	- 0.3	–	0.8	V
Digital Outputs					
Output Logic High, V_{OH}	I_{OH}=-20µA	DV_{DD}-0.5	–	–	V
Output Logic Low, V_{OL}	I_{OL}=20µA	–	–	0.4	V

Manufacturing Information

Table 35. Device Manufacturing Characteristics

Parameter	Chip(s)	Conditions
Maximum Temperature Gradient	DSP and AFE	**JEDEC Moisture Sensitivity Class 3** • Unsealed parts may be exposed to 30℃ 60% relative humidity for up to one week • If exposed more than one week, parts must be baked at 125℃ for 7 hours
Solder Profile	DSP and AFE	• 6℃/second maximum temperature ramp rate • 10-40 seconds at 220℃-225℃ (do not exceed 225℃) • 120-180 seconds above solder liquidus (approximately 183℃)

Thermal Performance

Table 36. Thermal Resistance

Product	Θ_{jA} at 0 LPM Air Velocity (^{o}C/W)	Θ_{jA} at 200 LPM Air Velocity (^{o}C/W)
144 LPQ2 DSP	16.0	13.6
28 SSOP AFE	49.8	43.9
28 EPTSSOP AFE	37.9	32.5

NOTE:
^{o}C/W = ^{o}C/Watts
LPM = Linear Feet Per Minute (LPM/196.8 = Meter/Second)
Θ_{JA}= Thermal Resistance - Junction to Ambient

Thermal data is obtained by mounting the chip set to a JEDEC standard board. The thermal performance in a custom board may vary. The following describes JEDEC standards:

In August (1996), the Electronics Industries Association released Standard EIA/JESD51-3 titled, “Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages.” This Standard provides guidelines for design of the test board used in taking thermal resistance measurements of integrated circuit packages. Prior to release of this Standard, thermal resistance data for similar packages varied greatly across the industry because of the use of different test board designs. In particular, the characteristics of the test board were found to have a dramatic impact on the measured Theta JA (Θ_{JA}). As the industry converts to using this standard test board design, the variation in thermal resistance data caused by the board should be minimized.

Key features of the standard test board design are:

- Board thickness: 0.062”
- Board dimension: 3.0" x 4.5" for packages < 27.0 mm
- Board dimension: 4.0" x 4.5" for packages > 27.0 mm

The JEDEC method for specifying the thermal performance of ICs does not reflect thermal performance at the line card or system level. Equipment OEMs must take thermal management into account in the design of systems featuring high-density line cards.

DSL Chip Set Outline Diagrams

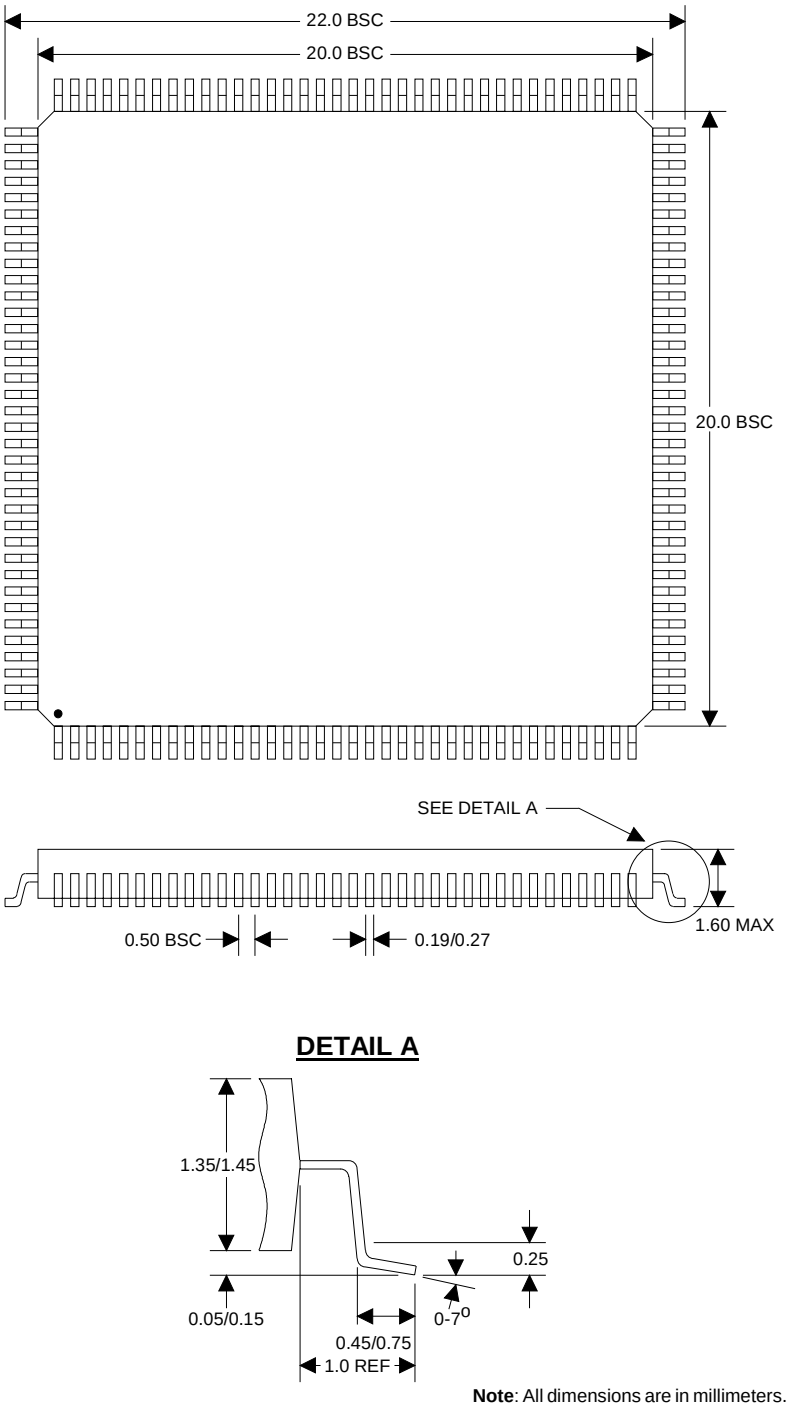
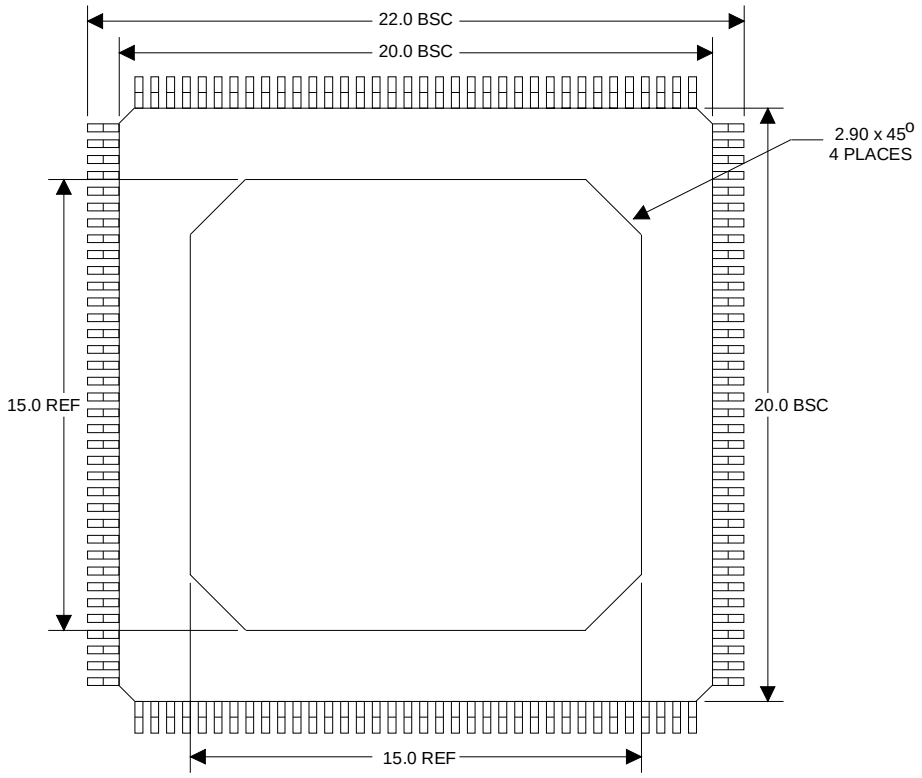


Figure 26. 144 LPQ2 and TQFP Dual-Channel DSP/Framer Outline Diagram

NOTE:

144 TQFP DSP/Framer is for dual-channel SDSL CAP unframed applications only.

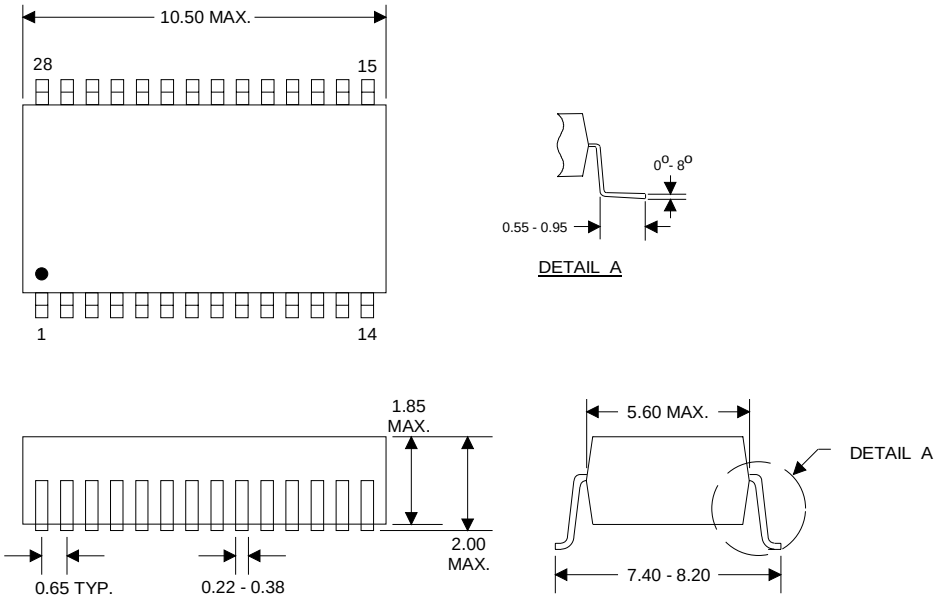


Note: All Dimensions are in millimeters (mm).

Figure 27. Bottom View of an LPQ2 Package

NOTE:

Refer to Application Note AN-026, “Differences Between TQFP and LPQ2 Packages for GlobeSpan G22xx-series DSP/Framers,” for details on the use of the LPQ2 package.



NOTE: All dimensions are in millimeters.

Figure 28. GS3137-08F ILD2 in 28 SSOP package

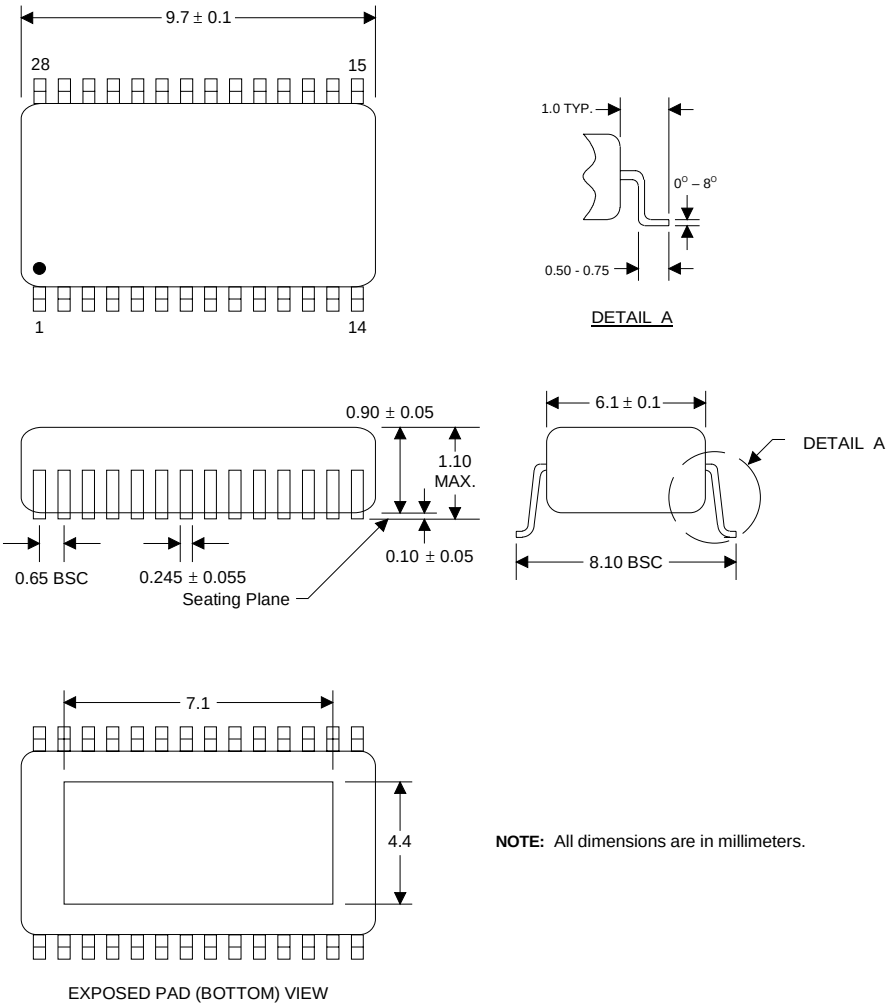


Figure 29. GS3137-08T ILD2 in 28 EPTSSOP package (Required to support HDSL2 and asymmetric PSD options for SHDSL).

NOTE:

Please make sure your PCB design takes into consideration the exposed PAD at the bottom of this package, which will need to be connected to the analog ground plane. The dimensions for this exposed pad are 7.1 mm x 4.4 mm located at the center of the device, as shown in the Bottom View above. Refer to Application Note AN-022, “Mounting Guidelines for GlobeSpan GS3137-08T in a 28-pin EPTSSOP Package,” for detailed mounting guidelines for this package.

XDSL2™ SDSL, HDSL2 and SHDSL - ILD2 Chip Set Order Information

Table 37. DSL Chip Set Part Number

Product	Supports	Chip Set	DSP/Framer	ILD2
SDSL 2B1Q ***Only***	Up to 2320 kb/s	G2216-208-041PF B2	144 LPQ2 GS2216-208-001P B2	28 SSOP GS3137-08F* (QTY 2)
SDSL CAP ***Only***	Up to 2320 kb/s	G2214-208-041DF B2	144 TQFP GS2214-208-001D B2	28 SSOP GS3137-08F* (QTY 2)
SHDSL/HDSL2	Up to 2320 kb/s	G2237-208-041PT B2	144 LPQ2 GS2237-208-001P B2	28 EPTSSOP GS3137-08T (QTY 2)
		G2237-208-041PT C1	144 LPQ2 GS2237-208-001P C1	

* The exposed PAD TSSOP (EPTSSOP) is required for designs that are upgradeable to SHDSL or HDSL2.

Table 38. Device Packaging

Device	Part Number	Package	Preproduction Orders		Production Orders	
			Minimum Order Quantity	Quantity Multiples	Minimum Order Quantity	Quantity Multiples
DSP	GS2216-208-001P B2	144 LPQ2	60	60	240	240
DSP	GS2214-208-001D B2	144 TQFP	60	60	240	240
DSP	GS2237-208-001P B2	144 LPQ2	60	60	240	240
DSP	GS2237-208-001P C1	144 LPQ2	60	60	240	240
AFE	GS3137-08F	28 SSOP	50	50	500	500
AFE	GS3137-08T	28 EPTSSOP	50	50	500	500

For additional information, contact GlobespanVirata, Inc. at **1-888-855-4562** (toll-free within the U.S. and Canada) or **1-732-345-7500**.

Visit the GlobeSpan Internet site at **www.globespan.net**.