21555AA/BA and 21555AB/BB Differences

Application Note

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1.0 Introduction

This document defines the differences between the 21555AA/BA bridge when compared with the 21555AB/BB bridge. The 21555 bridge is a second generation Non-Transparent PCI-to-PCI bridge.

1.1 Changes to the 21555 Bridge

After the introduction of the 21555AA/BA bridge, two errata were discovered

- The I_2O circuitry would not work in asynchronous mode.
- The BSDL circuitry was driving data one cycle late.

Additionally, the PCI standards committee ratified the new PCI 2.3 Specification, which required an additional bit to be added to the control register and status register.

The new 21555AB/BB bridge version addresses all three of these issues.

Note: This Differences document is not a stand-alone document and does not provide complete 21555 bridge details. The intent here is only to highlight the feature differences between the 21555AA/BA and the 21555BA/BB steppings. Please be sure to review the data sheet and spec updates for more complete information on the device.

2.0 Stepping Differences

Table 1. Stepping Differences

Package Markings	REV_ID Register Value[a]	Speed (MHz)	Stepping
Intel FW21555AA	02h	33	A2
Intel FW21555BA	02h	66	A2
Intel FW21555AB	03h	33	A3
Intel FW21555BB	03h	66	A3

a. Identified in a PCI system by reading the value in the REV_ID register.

3.0 I2O Asynchronous Operation

The 21555AA/BA devices would not operate asynchronously. This behavior has been corrected in the 21555AB/BB device. Please refer to the device data sheet for information on I_2O operation.

4.0 BSDL Data Being Driven Late

The 21555AA/BA BSDL (Boundary-Scan Description Language) data was being driven one clock cycle late causing a potential device contention issue if BSDL was single stepped during testing. This behavior has been corrected in the 21555AB/BB device. The BSDL file does not change.

5.0 New Feature - PCI 2.3 Compliance

The PCI Special Interest Group ratified the PCI 2.3 specification requiring an additional bit in the control register and an additional bit in the status register. The new register bits are as follows:

Table 1. Primary and Secondary Command Registers

Offsets	Primary Command	Secondary Command
Primary byte	05:04h	45:44h
Secondary byte	45:44h	05:04h

Bit	Name	R/W	Description
10	Interrupt Disable Bit	R/W	This bit disables the 21555 from asserting p_inta_l / s_inta_l. • When 0, enables the 21555 to assert its p_inta_l / s_inta_l signal. • When 1, disables the 21555 ability to assert the p_inta_l / s_inta_l signal. This bit's state after RST# is 0.

Note: Please refer to the following documentation for more information:

- *21555 Non-transparent PCI-to-PCI Bridge Datasheet*
- *21555 Non-transparent PCI-to-PCI Bridge User's Manual*
- *21555 Non-transparent PCI-to-PCI Bridge Hardware Implementation manual*
- *21555 Specification Update*

Table 2. Primary and Secondary Status Registers

Offsets	Primary Status	Secondary Status
Primary byte	07:06h	47:46h
Secondary byte	47:46h	07:06h

Bit	Name	R/W	Description
3	Interrupt Status Bit	R	This bit reflects the state of the interrupt in the 21555 bridge. • Only when the Interrupt Disable Bit in the command register is set to 0 and the appropriate interrupt status bit set to 1 will the p_inta_l/s_inta_l signals be asserted. • Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.