REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R006-98	98-01-22	Monica L. Poelking
B	Changes in accordance with NOR 5962-R111-98	98-05-22	Monica L. Poelking
C	Add device 02. Editorial changes throughout.	98-07-01	Monica L. Poelking
D	Update boilerplate to MIL-PRF-38535 requirements. - CFS	05-10-04	Thomas M. Hess

REV	D	D	D	D																
SHEET	35	36	37	38																
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Thomas M. Hess

DEFENSE SUPPLY CENTER COLUMBUS

COLUMBUS, OHIO 43218-3990
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Thomas M. Hess

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
94-10-17

REVISION LEVEL
D

MICROCIRCUIT, DIGITAL, CMOS, 32-BIT INTEGRATED MICROCONTROLLER, MONOLITHIC SILICON

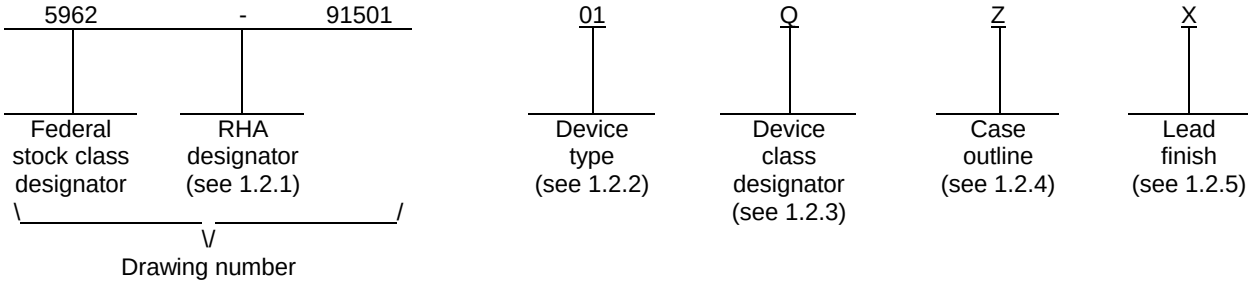
SIZE	CAGE CODE	
A	**67268**	**5962-91501**

SHEET 1 OF 38

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	68332 1/	32-bit integrated microcontroller
02	68332-20 1/	32-bit integrated microcontroller

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
Z	CMGA5-P132	132	Pin grid array
X	See figure 1	132	Gull wing leaded chip carrier
Y	See figure 1	132	Gull wing leaded chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ This part does not include the Quadrature Decoder (QDEC) function.

1.3 Absolute maximum ratings. 1/

Storage temperature range (T_{STG})	-55°C to +150°C
Supply voltage range	-0.3 V dc to +6.5 V dc 1/ 2/ 3/
Input voltage range (V_{IN})	-0.3 V dc to +6.5 V dc 1/ 2/ 3/ 4/
Instantaneous maximum current single pin limit (applies to all pins)	25 mA 1/ 2/ 3/ 5/
Power dissipation (P_D)	690 mW
Operating maximum current digital input disruptive current range	
$V_{SS} - 0.3 \le V_{IN} \le V_{DD} + 0.3$	-500 μA to +500 μA 5/ 6/ 7/
Thermal resistance, junction-to-case (θ_{JC}):	
Case Z	10°C/W
Case X and Y	10°C/W
Lead temperature range (soldering, 5 seconds)	270°C

1.4 Recommended operating conditions.

Case operating temperature range	-55°C to +125°C
Supply voltage range	4.50 V dc ≤ V_{DD} ≤ 5.50 V dc
PLL reference frequency range (f_{REF})	25 kHz to 50 kHz
System frequency: 8/	
Device 01	16.78 MHz
Device 02	20.97 MHz
On-chip PLL system frequency (f_{SYS}):	
Device 01	0.131 ≤ f_{SYS} ≤ 16.78 MHz
Device 02	0.131 ≤ f_{SYS} ≤ 20.97 MHz
External clock operation:	
Device 01	16.78 MHz
Device 02	20.97 MHz
PLL lock time (t_{LPLL})	20 ms 9/
Limp mode clock frequency (f_{LIMP}): 10/	
SYNCR X bit = 0	f_{SYS} max/2 MHz
SYNCR X bit = 1	f_{SYS} max MHz
CLKOUT stability (C_{STAB}): 11/ 12/	
Short term	-1.0% to +1.0%
Long term	-0.5% to +0.5%

1/ Permanent damage can occur if maximum ratings are exceeded. Exposure to voltages or currents in excess of recommended values affects device reliability. Device modules may not operate normally while being exposed to electrical extremes.
2/ Although sections of the device contain circuitry to protect against damage from high static voltages or electrical fields, take normal precautions to avoid exposure to voltages higher than maximum-rated voltages.
3/ This parameter is periodically sampled rather than 100% tested.
4/ All pins except TSTME/TSC.
5/ All functional non-supply pins are internally clamped to V_{SS}. All functional pins except EXTAL, $\overline{\text{TSTME}}$/TSC, and XFC are internally clamped to V_{DD}.
6/ Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions.
7/ Total input current for all digital input-only and all digital input/output pins must not exceed 10 mA. Exceeding this limit can cause disruption of normal operation.
8/ All internal registers retain data at 0 Hz.
9/ Assumes that stable V_{DDSYN} is applied, that an external filter capacitor with a value of 0.1 FF is attached to the XFC pin. and that the crystal oscillator is stable. Lock time is measured from power-up to reset release. This specification also applies to the period required for PLL lock after changing the W and Y frequency control bits in the synthesizer control register (SYNCR) while the PLL is running, and to the period required for the clock to lock after LPSTOP.
10/ Determine by the internal reference voltage applied to the on-chip VCO. The X-bit in SYNCR controls a divide by two prescaler on the system clock output.
11/ Short-term CLKOUT stability is the average deviation from programmed frequency measured over a 2 Fs interval at maximum f_{SYS}. Long-term CLKOUT stability is the average deviation from programmed frequency measured over a 1 ms interval at maximum f_{SYS}. Stability is measured with a stable external clock input applied variation in crystal oscillator frequency is additive to this figure.
12/ This parameter is periodically sampled rather than 100% tested.
13/ Values will be added when they become available.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and on figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Timing waveforms. The timing waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{DD} \le 5.5\ V$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input high voltage	V_{IH}		1, 2, 3	All	$0.7(V_{DD})$	V_{DD} + 0.3	V
Input low voltage	V_{IL}				V_{SS} – 0.3	$0.2(V_{DD})$	V
Input hysteresis 2/	V_{HYS}				0.5		V
Input leakage current, input-only pins 3/	I_{IN}	$V_{IN} = V_{DD}$ or V_{SS} Input-only pins.			-2.5	+2.5	µA
High impedance (off-state) leakage current, all input/output and output pins 3/	I_{OZ}	$V_{IN} = V_{DD}$ or V_{SS} All input/output and output pins.			-2.5	+2.5	µA
CMOS outputs high voltage 3/ 4/	V_{OH}	I_{OH} = -10.0 µA Group 1, 2, 4 I/O pins and all output pins.			V_{DD} – 0.2		V
CMOS outputs low voltage 3/	V_{OL}	I_{OL} = 10.0 µA Group 1, 2, 4 I/O pins and all output pins.				0.2	V
Output high voltage 3/ 4/	V_{OH}	I_{OH} = -0.8 mA Group 1, 2, 4 I/O pins and all output pins.			V_{DD} – 0.8		V
Output low voltage 3/	V_{OL}	I_{OL} = 1.6mA, Group 1 CLKOUT, FREEZE/QOUT, $\overline{\text{IPIPE}}$				0.4	V
		I_{OL} = 5.3 mA, Group 2, 4 I/O pins, $\overline{\text{CSBOOT}}$, $\overline{\text{BG}}$/$\overline{\text{CS}}$				0.4	
		I_{OL} = 12 mA, Group 3				0.4	
Three-state control input high voltage	V_{IHTSC}				$1.6(V_{DD})$	9.1	V
Data bus mode select pull-current 5/	I_{MSP}	$V_{IN} = V_{IL}$ Data(15:0)				-120	µA
		$V_{IN} = V_{IH}$ Data(15:0)			-15		
VDD supply current, RUN 6/ 7/	I_{DD}			01		124	mA
				02		160	
LPSTOP = 32.768 kHz crystal VCO off (STSIM = 0)	S_{IDD}			All		350	µA
LPSTOP (external clock input freq. = max. f_{SYS})	S_{IDD}					5	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{DD} \le 5.5\ V$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Clock synthesizer operating voltage	V_{DDSYN}		1, 2, 3	01	4.5	5.5	V
				02	4.75	5.25	
V_{DDSYN} supply current, 32.768 kHz crystal, VCO on, max. f_{SYS} 6/	I_{DDSYN}			01		1	mA
				02		2	
External clock, max. f_{SYS}	I_{DDSYN}			01		5	mA
				02		6	
LPSTOP, 32.768 kHz crystal, VCO off (STSIM = 0)	S_{IDDSYN}			All		150	µA
32.768 kHz crystal, V_{DD} powered down	I_{DDSYN}					100	µA
RAM standby voltage specified V_{DD} applied standby mode, $V_{DD} = V_{SS}$	V_{SB}			01	0.0	5.5	V
				02	0.0	5.25	
				01	3.0	5.5	
				02	3.0	5.25	
RAM standby current specified V_{DD} applied	I_{SB}			All		10	µA
RAM standby current standby mode $V_{DD} = V_{SS}$	I_{SB}					50	µA
Input capacitance	C_{IN}	See 4.4.1c	4			20	pF
Output capacitance	C_{OUT}					20	pF
Functional test		See 4.4.1b	7, 8				
Frequency of operation (32.768 kHz crystal) 9/	f		9, 10, 11	01	0.13	16.78	MHz
				02	0.13	20.97	
Clock period	1	See figure 4.	9, 10, 11	01	59.6		ns
				02	47.7		
ECLK period	1A			01	476		ns
				02	381		
External clock input period 10/	1B			01	59.6		ns
				02	47.7		
Clock pulse width	2, 3			01	24		ns
				02	18.8		
ECLK pulse width	2A, 3A			01	236		ns
				02	183		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{DD} \le 5.5\ V$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
External clock input high/low time 10/	2B, 3B	See figure 4.	9, 10, 11	01	29.8		ns
				02	23.8		
Clock rise and fall time	4, 5			All		5	ns
Rise and fall time - all outputs except CLKOUT	4A, 5A					8	ns
External clock rise and fall time	4B, 5B					5	ns
Clock high to address, FC, SIZE, $\overline{RMC}$, valid	6			01	0	29	ns
				02	0	23	
Clock high to address, data, FC, SIZE, $\overline{RMC}$, high impedance	7			01	0	59	ns
				02	0	47	
Clock high to address, FC, SIZE, $\overline{RMC}$, invalid	8			All	0		ns
Clock low to $\overline{AS}$, $\overline{DC}$, $\overline{CS}$, asserted	9			01	2	25	ns
				02	2	23	
$\overline{AS}$ or $\overline{DC}$ or $\overline{CS}$ asserted (read) 11/	9A			01	-15	15	ns
				02	-10	10	
Clock low to $\overline{IFETCH}$, $\overline{IPIPE}$ asserted	9C			All	2	22	ns
Address, FC, SIZE, $\overline{RMC}$, valid to $\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ read) asserted	11			01	15		ns
				02	10		
Clock low to $\overline{AS}$, $\overline{DC}$, $\overline{CS}$, negated	12			01	2	29	ns
				02	2	23	
Clock low to $\overline{IFETCH}$, $\overline{IPIPE}$ negated	12A			All	2	22	ns
$\overline{AS}$, $\overline{DC}$, $\overline{CS}$ negated to address, FC, SIZE invalid (address hold)	13			01	15		ns
				02	10		
$\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ read) width asserted	14			01	100		ns
				02	80		
$\overline{DS}$, $\overline{CS}$ width asserted (write)	14A			01	45		ns
				02	36		
$\overline{AS}$, $\overline{CS}$ (and $\overline{DS}$ read) width asserted (fast write cycle)	14B			01	40		ns
				02	32		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{DD} \le 5.5\ V$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{AS}$, $\overline{DC}$, $\overline{CS}$ width negated 12/	15	See figure 4.	9, 10, 11	01	40		ns
				02	32		
Clock high to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ high impedance	16			01		59	ns
				02		47	
$\overline{AS}$, $\overline{DC}$, $\overline{CS}$ negated to R/$\overline{W}$ high	17			01	15		ns
				02	10		
Clock high to R/$\overline{W}$ high	18			01	0	29	ns
				02	0	23	
Clock high to R/$\overline{W}$ low	20			01	0	29	ns
				02	0	23	
R/$\overline{W}$ high to $\overline{AS}$, $\overline{CS}$ asserted	21			01	15		ns
				02	10		
R/$\overline{W}$ low to $\overline{DS}$, $\overline{CS}$ asserted (write)	22			01	70		ns
				02	54		
Clock high to data out valid	23			01		29	ns
				02		23	
Data out valid to negating edge of $\overline{AS}$, $\overline{CS}$ (fast write cycle)	24			01	15		ns
				02	10		
$\overline{DC}$, $\overline{CS}$ negated to data out invalid (data out hold)	25			01	15		ns
				02	10		
Data out valid to $\overline{DS}$, $\overline{CS}$ asserted (write)	26			01	15		ns
				02	10		
Data in valid to clock low (data set-up)	27			All	5		ns
Late $\overline{BERR}$, $\overline{HALT}$ asserted to clock low (set-up time)	27A			01	20		ns
				02	15		
$\overline{AS}$, $\overline{DS}$ negated to $\overline{DSACK(1:0)}$, $\overline{BERR}$, $\overline{HALT}$, $\overline{AVEC}$ negated	28			01	0	80	ns
				02	0	60	
$\overline{DC}$, $\overline{CS}$ negated to data in invalid (data in hold) 13/	29			All	0		ns
$\overline{DC}$, $\overline{CS}$ negated to data in high impedance 13/ 14/	29A			01		55	ns
				02		48	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{DD} \le 5.5\ V$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CLKOUT low to data in invalid (fast cycle hold) 13/	30	See figure 4.	9, 10, 11	01	15		ns
				02	10		
CLKOUT low to data in high impedance 13/	30A			01		90	ns
				02		72	
$\overline{DSACK(1:0)}$ asserted to data in valid	31	See figure 4. 15/		01		50	ns
				02		46	
Clock low to $\overline{BG}$ asserted/ negated	33	See figure 4.		01		29	ns
				02		23	
$\overline{BR}$ asserted $\overline{BG}$ asserted (RMC not asserted) 16/	35			All	1		t_{cyc}
$\overline{BGACK}$ asserted to $\overline{BG}$ negated	37				1	1	t_{cyc}
$\overline{BG}$ width negated	39				2		t_{cyc}
$\overline{BG}$ width asserted	39A				1		t_{cyc}
R/$\overline{W}$ width asserted (write or read)	46			01	150		ns
				02	115		
R/$\overline{W}$ width asserted (fast write or read cycle)	46A			01	90		ns
				02	70		
Asynchronous input set-up time $\overline{BR}$, $\overline{BGACK}$, $\overline{DSACK(1:0)}$, $\overline{BERR}$, $\overline{AVEC}$, $\overline{HALT}$	47A			All	5		ns
Asynchronous input hold time	47B			01	15		ns
				02	12		
$\overline{DSACK(1:0)}$ asserted to $\overline{BERR}$, $\overline{HALT}$ asserted 17/	48			All		30	ns
Data out hold from clock high	53				0		ns
Clock high to data out high impedance	54			01		28	ns
				02		23	
R/$\overline{W}$ asserted to data bus impedance change	55			01	40		ns
				02	32		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{DD} \le 5.5\ V$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{\text{RESET}}$ pulse width (reset instruction)	56	See figure 4.	9, 10, 11	All	512		t_{cyc}
$\overline{\text{BERR}}$ negated to $\overline{\text{HALT}}$ negated (rerun)	57				0		ns
Clock low to data bus driven (show)	70			01	0	29	ns
				02	0	23	
Data set-up time clock low (show)	71			01	15		ns
				02	10		
Data hold from clock low (show)	72			All	10		ns
$\overline{\text{BKPT}}$ input set-up time	73			01	15		ns
				02	10		
$\overline{\text{BKPT}}$ input hold time	74			All	10		ns
Mode select set-up time	75				20		t_{cyc}
Mode select hold time	76				0		ns
$\overline{\text{RESET}}$ assertion time 18/	77				4		t_{cyc}
$\overline{\text{RESET}}$ rise time 19/ 20/	78					10	t_{cyc}
Background debugging mode timing							
DSI input set-up time	B0	See figure 4.	9, 10, 11	All	15		ns
DSI input hold time	B1				10		ns
DSCLK set-up time	B2				15		ns
DSCLK hold time	B3				10		ns
S0 delay time	B4					25	ns
SCLK cycle time	B5				2		t_{cyc}

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{DD} \le 5.5\ V$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Background debugging mode timing - Continued.							
CLKOUT high to $\overline{\text{FREEZE}}$ asserted negated	B6	See figure 4.	9, 10, 11	All		50	ns
CLKOUT high to $\overline{\text{IFETCH}}$ high impedance	B7					50	ns
CLKOUT high to $\overline{\text{IFETCH}}$ valid	B8					50	ns
DSCLK low time	B9				1		t_{cyc}
ECLK bus timing							
ECLK low to address valid 21/	E1	See figure 4.	9, 10, 11	01		60	ns
				02		48	
ECLK low to address hold	E2			All	10		ns
ECLK low to $\overline{\text{CS}}$ valid ($\overline{\text{CS}}$ delay)	E3			01		150	ns
				02		120	
ECLK low to $\overline{\text{CS}}$ hold	E4			01	15		ns
				02	10		
$\overline{\text{CS}}$ negated width	E5			01	30		ns
				02	25		
Read data set-up time	E6			01	30		ns
				02	25		
Read data hold time	E7			01	15		ns
				02	5		
ECLK low to data high impedance	E8			01		60	ns
				02		48	
$\overline{\text{CS}}$ negated to data hold (read)	E9			All	0		ns
$\overline{\text{CS}}$ negated to data high impedance	E10					1	t_{cyc}
ECLK low to data valid (write)	E11					2	t_{cyc}
ECLK low to data hold (write)	E12			01	5		ns
				02	10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{DD} \le 5.5\ V$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ECLK bus timing - Continued.							
$\overline{CS}$ negate to data hold (write)	E13	See figure 4.	9, 10, 11	All	0		ns
Address access time (read) 22/	E14			01	386		ns
				02	308		
Chip select access time (read) 23/	E15			01	296		ns
				02	236		
Address set-up time	E16			All	0.5		t_{cyc}
QSPI timing							
Operating frequency master	f_{OP}	See figure 4.	9, 10, 11	All		0.25	sys clk freq
Operating frequency slave	f_{OP}					0.25	sys clk freq
Cycle time master	1				4	510	t_{cyc}
Cycle time slave	1				4		t_{cyc}
Enable lead time master	2				2	128	t_{cyc}
Enable lead time slave	2				2		t_{cyc}
Enable lag time master	3					0.5	SCK
Enable lag time slave	3				2		t_{cyc}
Clock (SCK) high or low time master	4				$2t_{cyc}$ - 60	$255t_{cyc}$	ns
Clock (SCK) high or low time slave 24/	4				$2t_{cyc}$ - n		ns
Sequential transfer delay master	5				17	8192	t_{cyc}
Sequential transfer delay slave (does not require deselect)	5				13		t_{cyc}

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{DD} \le 5.5\ V$	Group A subgroups	Device type	Limits		Unit
					Min	Max	
QSPI timing - Continued.							
Data set-up time (inputs) master	6	See figure 4.	9, 10, 11	All	30		ns
Data set-up time (inputs) slave	6				20		ns
Data hold time (inputs) master	7				0		ns
Data hold time (inputs) slave	7				20		ns
Slave access time	8					1	t_{cyc}
Slave MISO disable time	9					2	t_{cyc}
Data valid (after SCK edge) master	10					50	ns
Data hold time (after SCK edge) slave	10					50	ns
Data hold time (outputs) master	11				0		ns
Data hold time (outputs) slave	11				0		ns
Rise time input	12					2	µs
Rise time output	12					30	ns
Fall time input	13					2	µs
Fall time output	13					30	ns

See footnotes on next sheet.

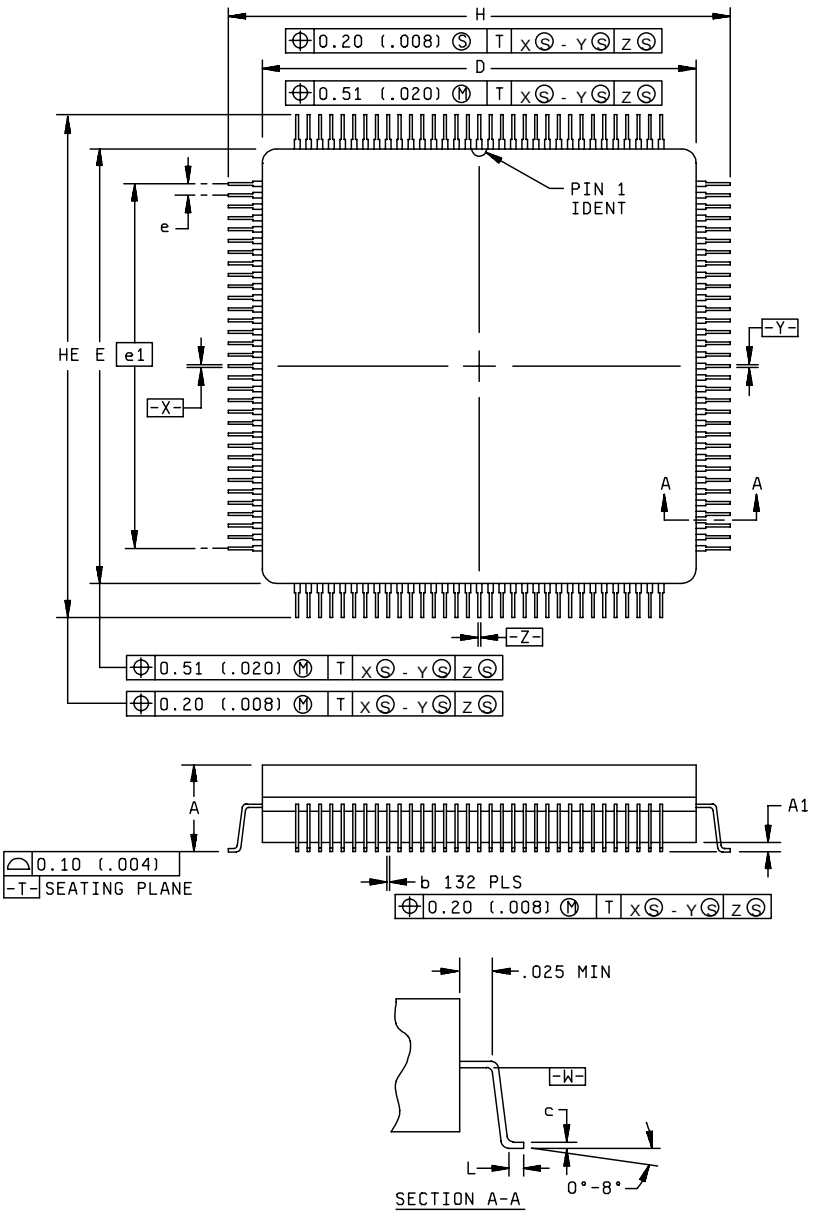
TABLE I. Electrical performance characteristics - Continued.

1/ All testing to be performed using worst-case test conditions unless otherwise specified.
2/ Applies to: TP[15:0], Port D [7:0], Port E [7:3], Port F [7:0], TSTME/TSC, BKPT, RESET, IFETCH, T2CLK, RXD
3/ Input-only pins: TSTME/TSC, BKPT, T2CLK, RXD
Output only pins: CSBOOT, BG/CS, CLKOUT, FREEZE/QUOT, IPIPE
Input/Output pins:
Group 1: DATA[15:0], IFECH, TP[15:0]
Group 2: Port C (ADDR23/ECLK, ADDR[22:19]/CS[9:6], FC[2:0]/CS[5:3])
Port D (PCS[3:1], TXD, PCS0/SS)
Port E (DSACK[1:0], AVEC, RMC, DS, AS, SIZ[1:0])
Port F (IRQ[7:1], MODCLK)
ADDR[18:0], R/W, BERR, BR/CS0, BGACK/CS2
Group 3: HALT, RESET
Group 4: MISO, MOSI, SCK
4/ Does not apply to HALT and RESET because they are open drain pins. Does not apply to Port D (MISO, MOSI, SCK, PCS/SS, PCS[3:1], TXS) in wired-OR mode.
5/ Use of an active pulldown device is recommended.
6/ Total operating current is the sum of the appropriate V_{DD} supply and V_{DDSYN} supply current.
7/ Current measured with system clock frequency of 16.78 MHz, all modules active.
8/ The SRAM module will not switch into standby mode as long as V_{SB} does not exceed V_{DD} by more than 0.5 V. The SRAM array cannot be accessed while the module is in standby mode.
9/ Minimum system clock frequency is four times the crystal frequency, subject to specified limits.
10/ Minimum external clock high and low times are based on 50% duty cycle. The minimum allowable t_{XCYC} period will be reduced when the duty cycle of the external clock signal varies. The relationship between external clock input duty cycle and minimum t_{XCYC} is expressed:

Minimum t_{XCYC} period = Minimum / (50% - external clock input duty cycle tolerance).

To achieve maximum operating (f_{SYS}) while using an external clock input, adjust clock input duty cycle to obtain a 50 percent duty cycle on CLKOUT.
11/ Specification t_{STSA} is the worst-case skew between AS and DS or CS. The amount of skew depends on the relative loading of these signals. When loads are kept within specified limits, skew will not cause AS an DS to fall outside the limits shown in specification t_{CLSA}.
12/ If multiple chip selects are used, CS width negated (specification t_{SN}) applies to the time from the negation of a heavily loaded chip select to the assertion of a lightly loaded chip select. The CS width negated specification between multiple chip selects does not apply to chip selects being used for synchronous ECLK cycles.
13/ These hold times are specified with respect to DS or CS on asynchronous reads and with respect to CLKOUT on fast cycle reads. The user is free to use either hold time.
14/ Maximum value is equal to (t_{CYC}/2) + 25 ns.
15/ If the asynchronous set-up time (specification t_{AIST}) requirements are satisfied, the DSACK(1:0) low to data set-up time (specification t_{DADI}) and DSACK(1:0) low to BERR low set-up time (specification t_{DABA}) can be ignored. The data must satisfy only the late BERR low to clock low set-up time (specification t_{BELCL}) for the following clock cycle
16/ To ensure coherency during every operand transfer, BG will not be asserted in response to BR until after all cycles of the current operand transfer are complete and RMC is negated.
17/ In the absence of DSACK(1:0), BERR is an asynchronous input using the asynchronous set-up time (specification t_{AIST}).
18/ After external RESET negation is detected, a short transition period (approximately 2 t_{cyc}). elapses, then the SIM drives RESET low for 512 t_{cyc}.
19/ External assertion of the RESET input can overlap internally-generated resets. To insure that an external reset is recognized in all cases, RESET must be asserted for at least 590 CLKOUT cycles.
20/ External logic must pull RESET high during this period in order for normal MCU operation to begin.
Address access time = (2.5 + WS) t_{cyc} - t_{CHAV} - t_{DICL}
Chip select access time = (2 + WS) t_{cyc} - t_{CLSA} - t_{DICL}
Where: WS = number of wait states. When fast termination is used (2 clock bus) WS = -1.
21/ When the previous bus cycle is not ECLK cycle, the address may be valid before ECLK goes low.
22/ Address access time = t_{Ecyc} - t_{EAD} - t_{EDSR}.
23/ Chip select access time = t_{Ecyc} - t_{ECSD} - t_{EDSR}.
24/ In formula, n = External SCK rise + External SCK fall time.

Case X



NOTES: (For case outline X only)

1. The preferred unit of measurement is millimeters. However, this item was designed using inch-pound units of measurement. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
2. Dimensions D and E define maximum ceramic body dimensions including glass protrusion and mismatch of ceramic body top and bottom.
3. Datum plane -W- is located at the underside of leads where leads exit package body.
4. Datum X-Y and Z to be determined where center leads exit package body at datum -W-.
5. Dimensions HD and HE to be determined at seating plane, datum -T-.
6. Dimensions D and E to be determined at datum plane -W-.

FIGURE 1. Case outlines.

Case X

Case X				
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.155	.178	3.940	4.520
A1	.019	.039	0.500	1.000
b	.008	.012	0.204	0.292
c	.005	.010	0.127	0.254
D/E	.860	.900	21.85	22.86
e	.025 BSC		---	
e1	.800 BSC		20.32 BSC	
HD/HE	1.072	1.088	27.230	27.630
L	.020	.030	0.510	0.760
N	132		132	
R	.0110	.0340	2.790	0.864
R1	.009	---	0.229	---

NOTES:
1. A terminal 1 identification mark shall be located at the index corner in the shaded area shown. Terminal 1 is located immediately adjacent to and counterclockwise from the index corner. Terminal numbers increase in a counterclockwise direction when viewed as shown.
2. Generic lead attach dogleg depiction.
3. Dimension N: Number of terminals.
4. Corner shapes (square, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
5. Metric equivalents are given for general information only.
6. Controlling dimension: Inch.
7. Datums X and Y to be determined where center leads exit the body.
8. Dimensions b and c include lead finish.

FIGURE 1. Case outlines - Continued.

Case Y

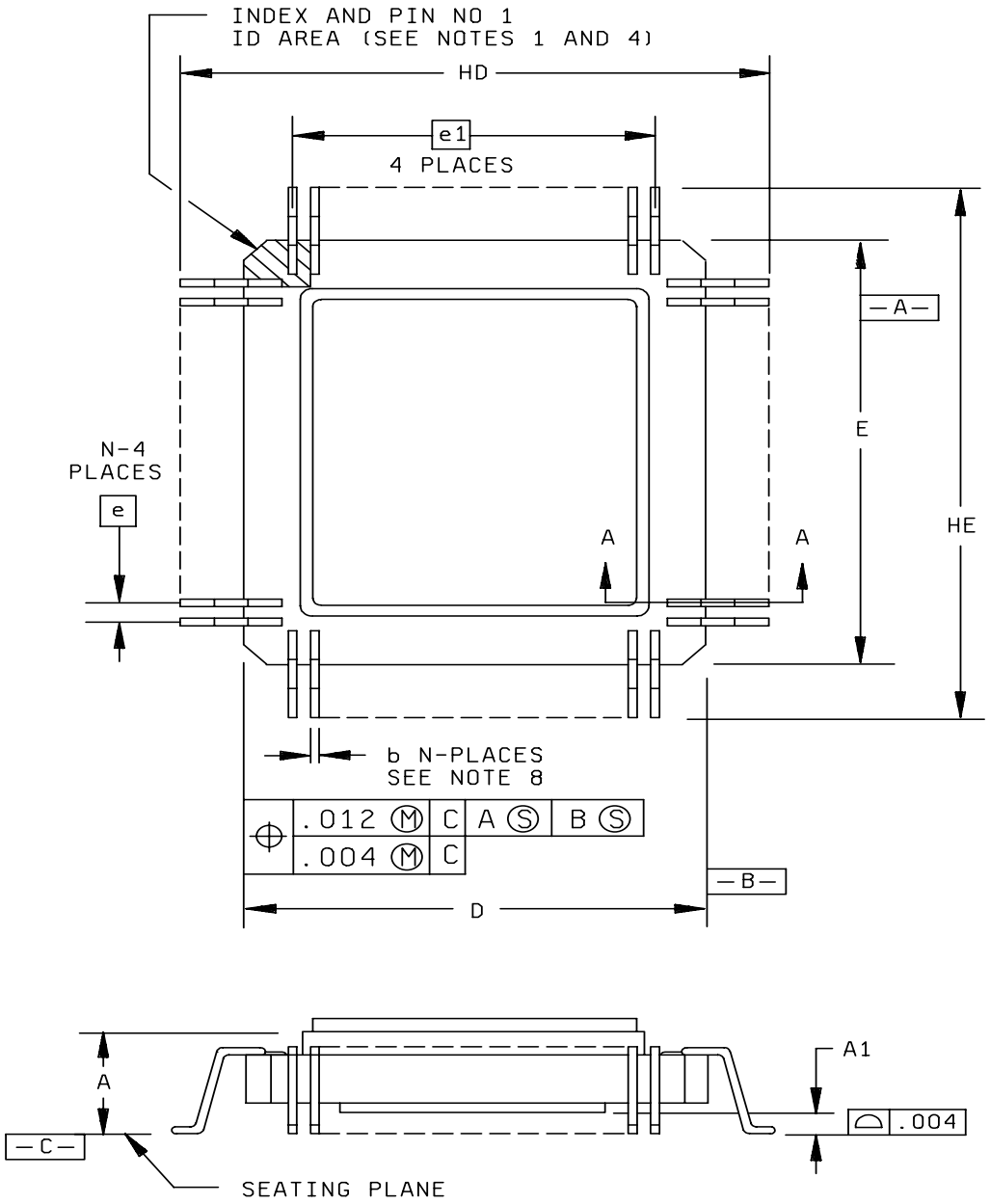
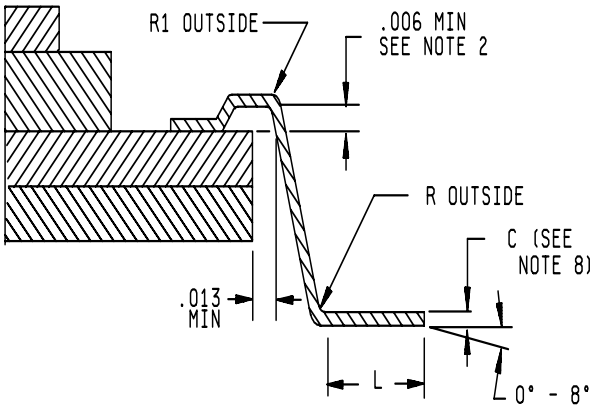


FIGURE 1. Case outlines - Continued.

Case Y



SECTION A-A

Case Y				
Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A		.125		3.175
A1	.018	.035	0.457	0.889
b	.018	.030	0.457	0.762
c	.005	.010	0.127	0.254
D/E	.940	.960	23.88	24.38
e	.025 BSC		---	
e1	.600 BSC		---	
HD/HE	1.133	1.147	28.78	29.13
L	.024	.040	0.610	1.016
N	132		132	
R	.011	.034	0.279	0.864
R1	.009	---	0.229	---

NOTES:
1. A terminal 1 identification mark shall be located at the index corner in the shaded area shown. Terminal 1 is located immediately adjacent to and counterclockwise from the index corner. Terminal numbers increase in a counterclockwise direction when viewed as shown.
2. Generic lead attach dogleg depiction.
3. Dimension N: Number of terminals.
4. Corner shapes (square, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
5. Metric equivalents are given for general information only.
6. Controlling dimension: Inch.
7. Datums X and Y to be determined where center leads exit the body.
8. Dimensions b and c include lead finish.

FIGURE 1. Case outlines - Continued.

Case X

Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
1	V_{DD}	28	V_{DD}	55	IFETCH/DS1	82	AS	109	D2
2	V_{SS}	29	V_{SS}	56	BKPT/DSCLK	83	V_{SS}	110	D1
3	TP11	30	A9	57	TSTME/TSC	84	V_{DD}	111	D0
4	TP10	31	A10	58	FREEZE/QUOT	85	DS	112	CSBOOT
5	TP9	32	A11	59	V_{SS}	86	RMC	113	BR/CS0
6	TP8	33	A12	60	XTAL	87	AVEC	114	BG/CS1
7	V_{DD}	34	V_{SS}	61	VDDSYN	88	DSACK1	115	BGACK/CS2
8	V_{SS}	35	A13	62	EXTAL	89	DSACK0	116	V_{CC}
9	TP7	36	A14	63	V_{DD}	90	A0	117	V_{SS}
10	TP6	37	A15	64	XPC	91	D15	118	FC0/CS3
11	TP5	38	A16	65	V_{DD}	92	D14	119	FC1/CS4
12	TP4	39	V_{DD}	66	CLKOUT	93	D13	120	FC2/CS5
13	TP3	40	V_{SS}	67	V_{SS}	94	D12	121	A19/CS6
14	TP2	41	A17	68	RESET	95	V_{SS}	122	A20/CS7
15	TP1	42	A18	69	HALT	96	V_{DD}	123	A21/CS8
16	TP0	43	MISO	70	BERR	97	D11	124	A22/CS9
17	V_{SS}	44	MOSI	71	IRQ7	98	D10	125	A23/CS10
18	V_{DD}	45	SCK	72	IRQ6	99	D9	126	V_{DD}
19	VSTBY	46	PCS0/SS	73	IRQ5	100	D8	127	V_{SS}
20	A1	47	PCS1	74	IRQ4	101	V_{SS}	128	T2CLK
21	A2	48	PCS2	75	IRQ3	102	D7	129	TP15
22	A3	49	PCS3	76	IRQ2	103	D6	130	TP14
23	A4	50	V_{DD}	77	IRQ1	104	D5	131	TP13
24	A5	51	V_{SS}	78	MODCK	105	D4	132	TP12
25	A6	52	TXD	79	R/W	106	V_{SS}		
26	A7	53	RXD	80	SIZ1	107	V_{DD}		
27	A8	54	IPIPE/DS0	81	SIZ0	108	D3		

FIGURE 2. Terminal connections.

Case Y

Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
1	VDD	34	VSS	67	VDD	100	VSS
2	VSTBY	35	TXD	68	DS	101	FCO/CS3
3	A1	36	RXD	69	RMC	102	FC1/CS4
4	A2	37	IPIPE/DSO	70	AVEC	103	FC2/CS5
5	A3	38	IFETCH/DS1	71	DSACK1	104	A19/CS6
6	A4	39	BKPT/DSCLK	72	DSACK0	105	A20/CS7
7	A5	40	TSTME/TSC	73	A0	106	A21/CS8
8	A6	41	FREEZE/QUOT	74	D15	107	A22/CS9
9	A7	42	VSS	75	D14	108	A23/CS10
10	A8	43	XTAL	76	D13	109	VDD
11	VDD	44	VDDSYN	77	D12	110	VSS
12	VSS	45	EXTAL	78	VSS	111	T2CLK
13	A9	46	VDD	79	VDD	112	TP15
14	A10	47	XPC	80	D11	113	TP14
15	A11	48	VDD	81	D10	114	TP13
16	A12	49	CLKOUT	82	D9	115	TP12
17	VSS	50	VSS	83	D8	116	VDD
18	A13	51	RESET	84	VSS	117	VSS
19	A14	52	HALT	85	D7	118	TP11
20	A15	53	BERR	86	D6	119	TP10
21	A16	54	IRQ7	87	D5	120	TP9
22	VDD	55	IRQ6	88	D4	121	TP8
23	VSS	56	IRQ5	89	VSS	122	VDD
24	A17	57	IRQ4	90	VDD	123	VSS
25	A18	58	IRQ3	91	D3	124	TP7
26	MISO	59	IRQ2	92	D2	125	TP6
27	MOSI	60	IRQ1	93	D1	126	TP5
28	SCK	61	MODCK	94	D0	127	TP4
29	PCS0/SS	62	R/W	95	CSBOOT	128	TP3
30	PCS1	63	SIZ1	96	BR/CS0	129	TP2
31	PCS2	64	SIZ0	97	BG/CS1	130	TP1
32	PCS3	65	AS	98	BGACK/CS2	131	TP0
33	VDD	66	VSS	99	VCC	132	VSS

FIGURE 2. Terminal connections - Continued.

Case Z

Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name	Pin number	Pin name
A1	A2	C1	A6	E4	VSS	J4	VSS	L12	DSACK1
A2	TP4	C2	A4	E10	VSS	J10	VSS	L13	A0
A3	TP5	C3	A1	E11	VSS	J11	VSS	M1	PCS2
A4	TP7	C4	TP3	E12	D4	J12	D13	M2	RXD
A5	TP9	C5	VDD	E13	D5	J13	D12	M3	IFETCH/DSI
A6	TP11	C6	VDD	F1	A12	K1	MISO	M4	FREEZE/QUOT
A7	TP13	C7	VDD	F2	A11	K2	MOSI	M5	EXTAL
A8	TP14	C8	VDD	F3	VSTBY	K3	PCSO/SS	M6	CLKOUT
A9	T2CLK	C9	VDD	F11	VDD	K4	VDD	M7	BERR
A10	A22/CS9	C10	A19/CS6	F12	D6	K5	VSS	M8	IRQ6
A11	A20/CS7	C11	BGACK/CS2	F13	D7	K9	VSS	M9	IRQ4
A12	FC1/CS4	C12	CSBOOT	G1	A14	K10	DS	M10	IRQ1
A13	BG/CS1	C13	D2	G2	A13	K11	DSACK0	M11	SIZ1
B1	A5	D1	A8	G3	VSS	K12	D15	M12	RMC
B2	TP1	D2	A7	G11	VSS	K13	D14	M13	AVEC
B3	TP2	D3	A3	G12	D8	L1	SCK	N1	PCS3
B4	TP6	D4	TP0	G13	D9	L2	PCS1	N2	IPIPE/DS0
B5	TP8	D5	VSS	H1	A15	L3	TXD	N3	TSTME/TSC
B6	TP10	D9	VSS	H2	A16	L4	BKPT/DSCLK	N4	XTAL
B7	TP12	D10	VSS	H3	VDD	L5	VDD	N5	XFC
B8	TP15	D11	BR/CS0	H11	VDD	L6	VDDSYN	N6	RESET
B9	A23/CS10	D12	D1	H12	D11	L7	VDD	N7	HALT
B10	A21/CS8	D13	D3	H13	D10	L8	VDD	N8	IRQ7
B11	FC2/CS5	E1	A10	J1	A17	L9	VDD	N9	IRQ5
B12	FC0/CS3	E2	A9	J2	A18	L10	R/W	N10	IRQ3
B13	D0	E3	VSS	J3	VSS	L11	AS	N11	IRQ2
								N12	MODCK
								N13	SIZO

Note: The following signals are active low: PCS0/SS, PCS1, PCS2, PCS3, IPIPE, IFETCH, BKPT, TSTME, RESET, HALT, ERR, IRQ1-7, W, AS, DS, RMC, AVEC, DSACK1, DSACK0, CSBOOT, BR, BG, BGACK, CS0-10 for all packages.

FIGURE 2. Terminal connections - Continued.

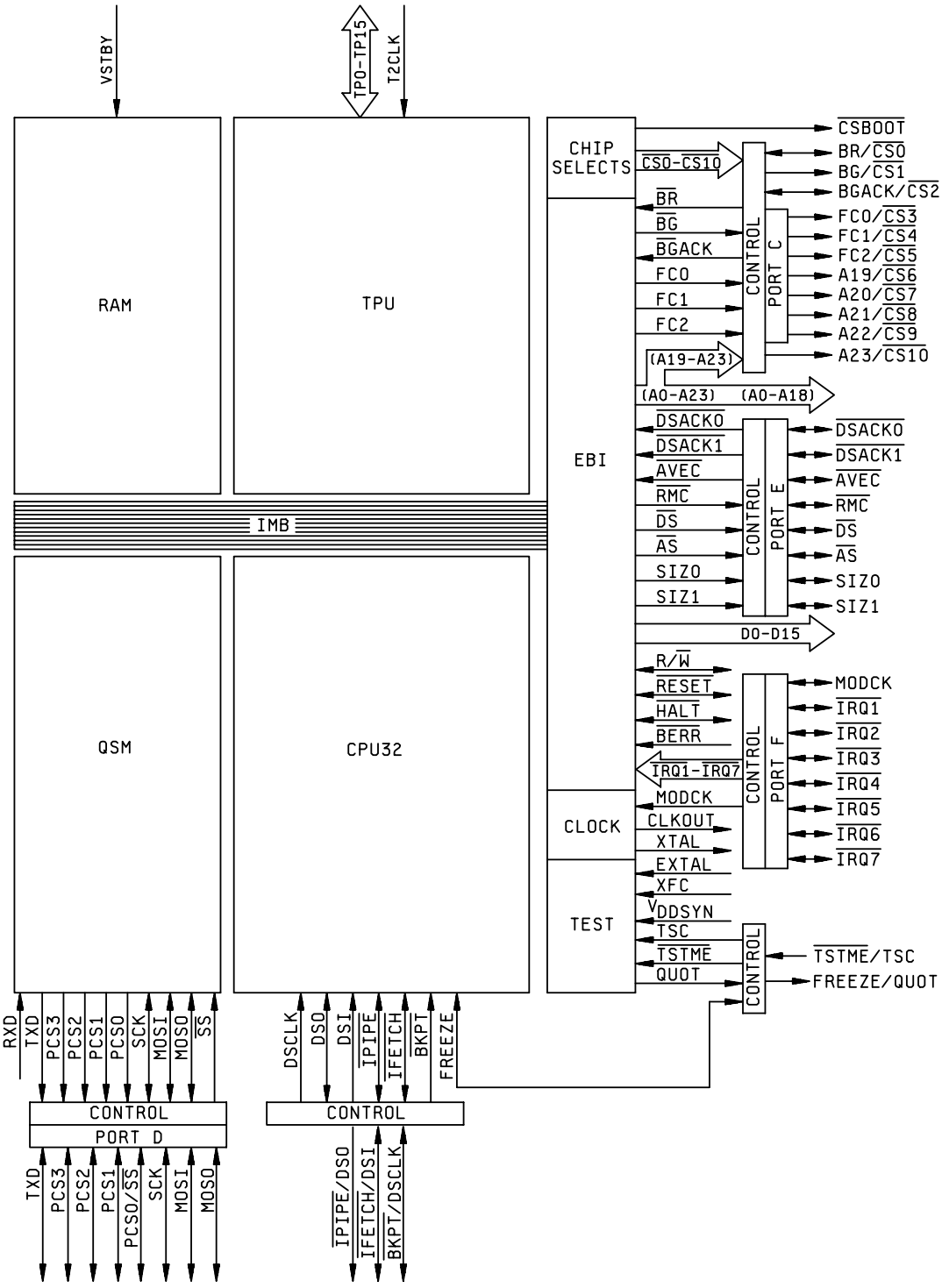
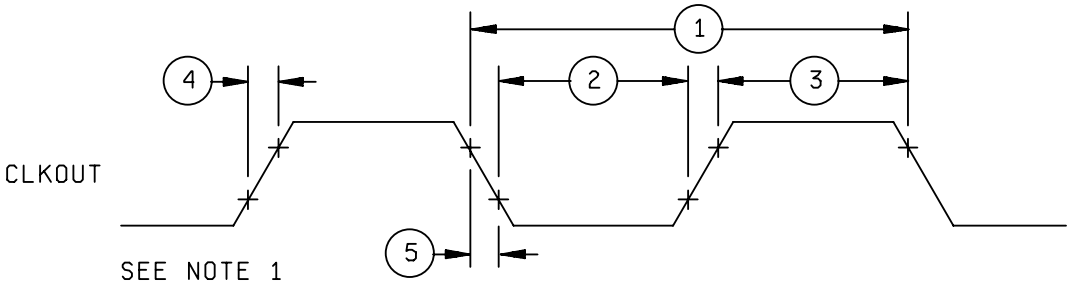
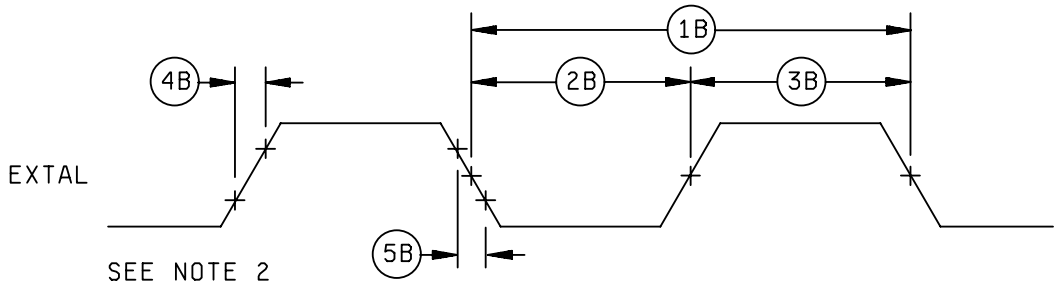


FIGURE 3. Block diagram.

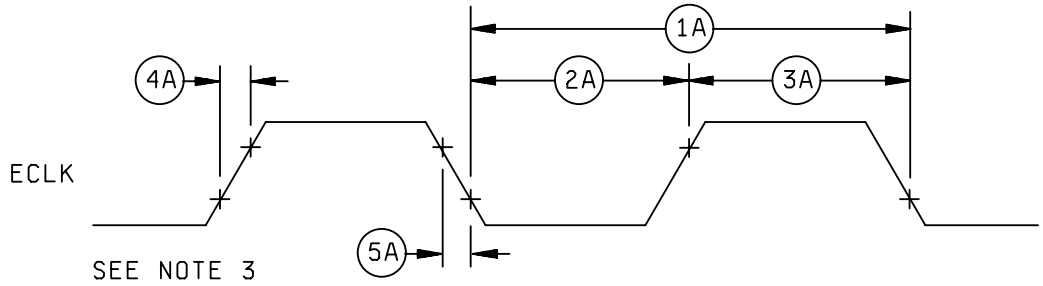
STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43218-3990	SIZE A		5962-91501
		REVISION LEVEL D	SHEET 23



CLKOUT OUTPUT TIMING DIAGRAM



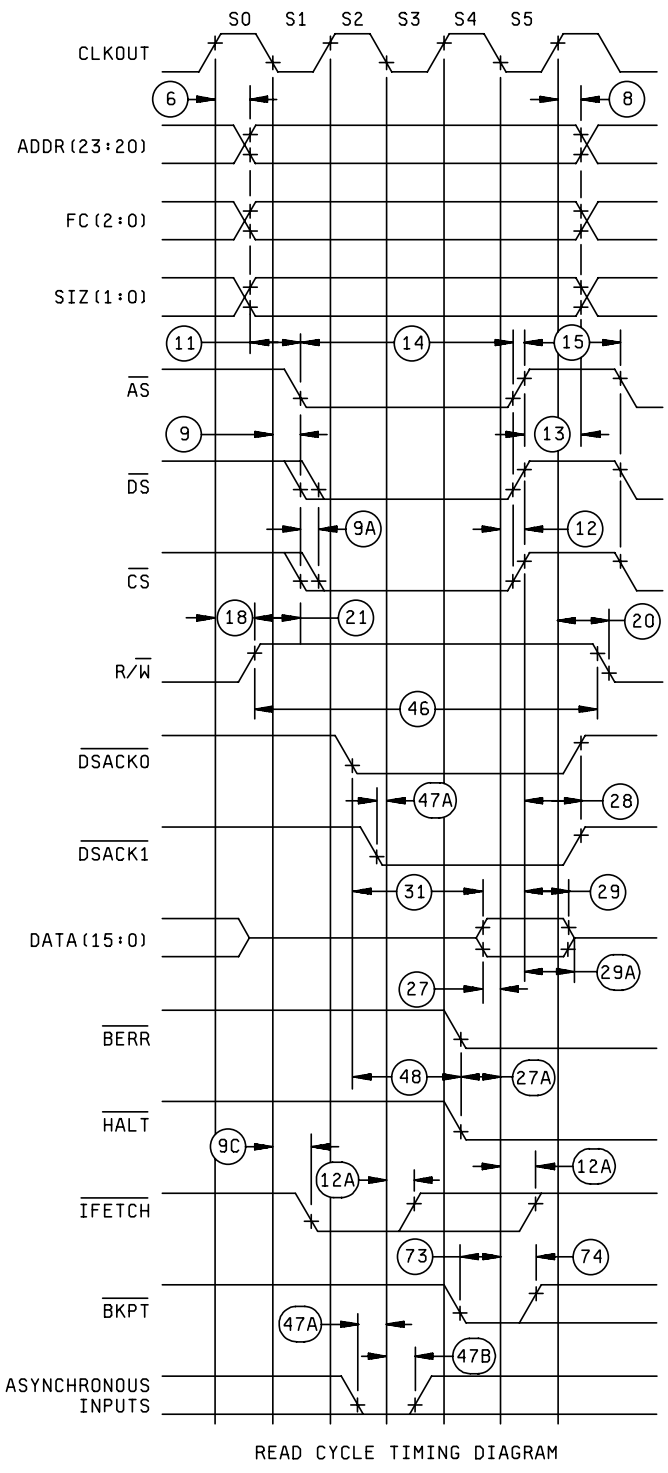
EXTERNAL CLOCK INPUT TIMING DIAGRAM



ECLK OUTPUT TIMING DIAGRAM

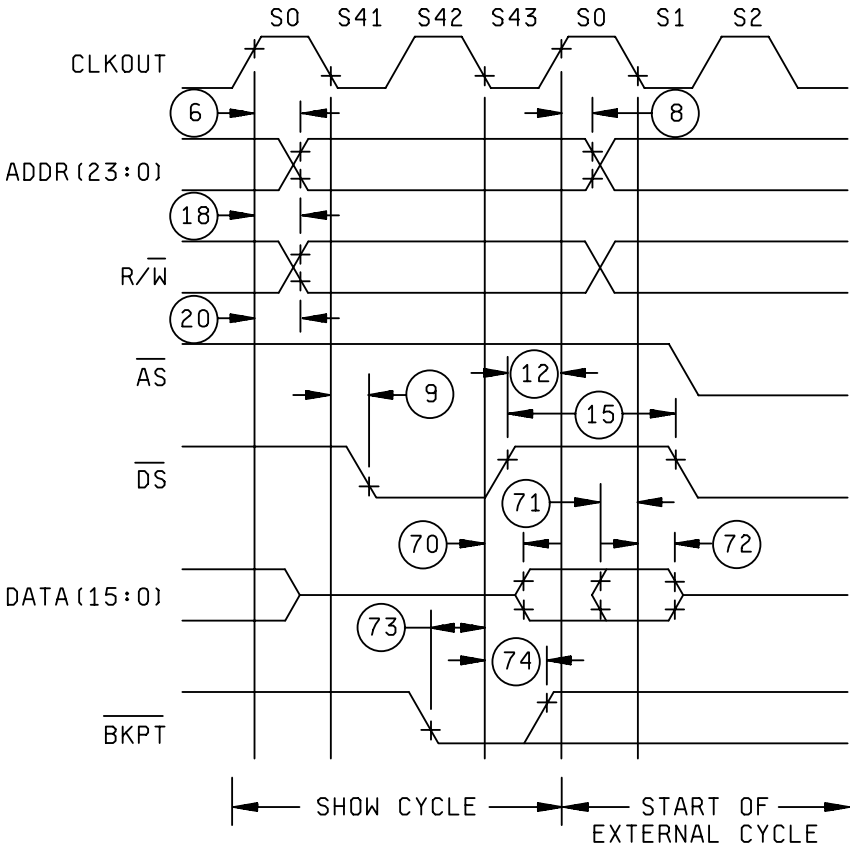
Notes:
1/ Timing shown with respect to 20% and 70% V_{DD}.
2/ Timing shown with respect to 20% and 70% V_{DD}. Pulse width shown with respect to 50% V_{DD}.
3/ Timing shown with respect to 20% and 70% V_{DD}

FIGURE 4. Timing waveforms.

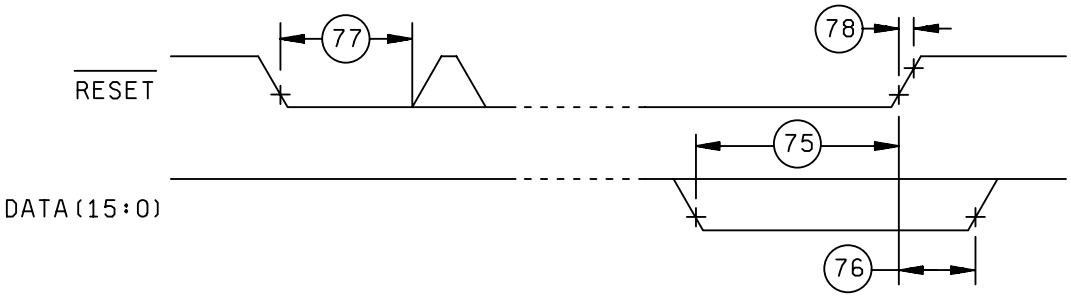


READ CYCLE TIMING DIAGRAM

FIGURE 4. Timing waveforms - Continued.



SHOW CYCLE TIMING DIAGRAM



RESET AND MODE SELECT TIMING DIAGRAM

FIGURE 4. Timing waveforms - Continued.

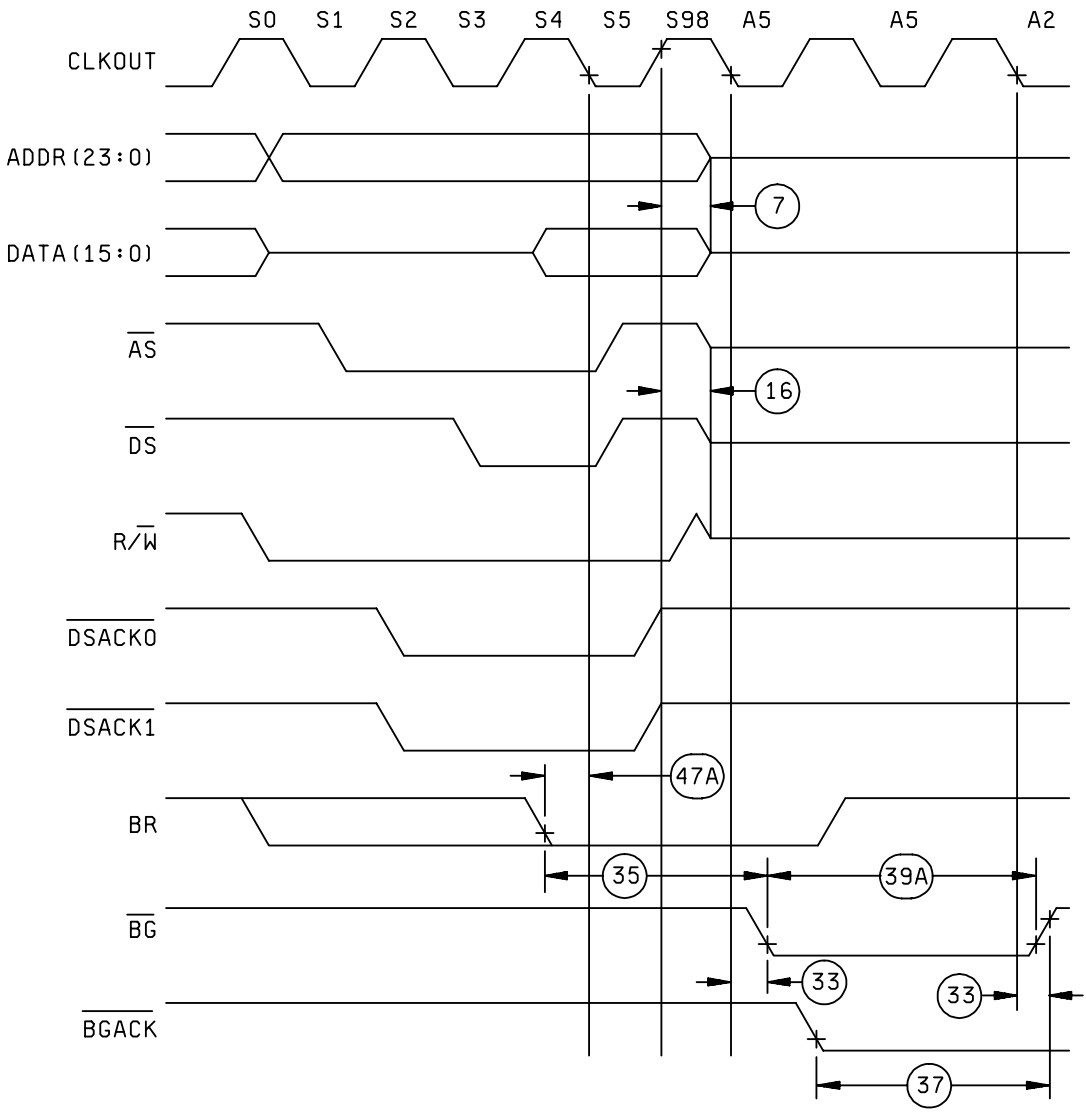
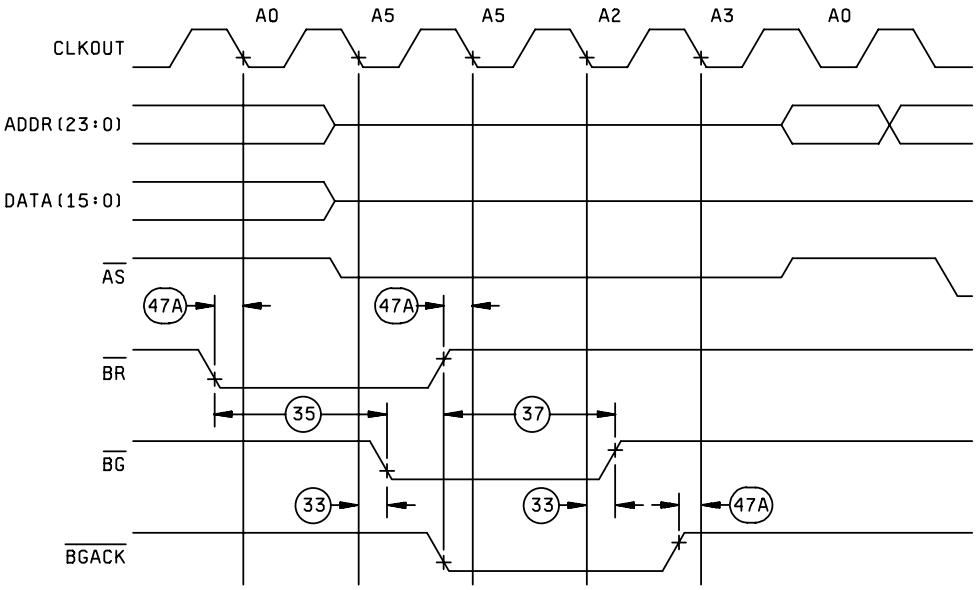
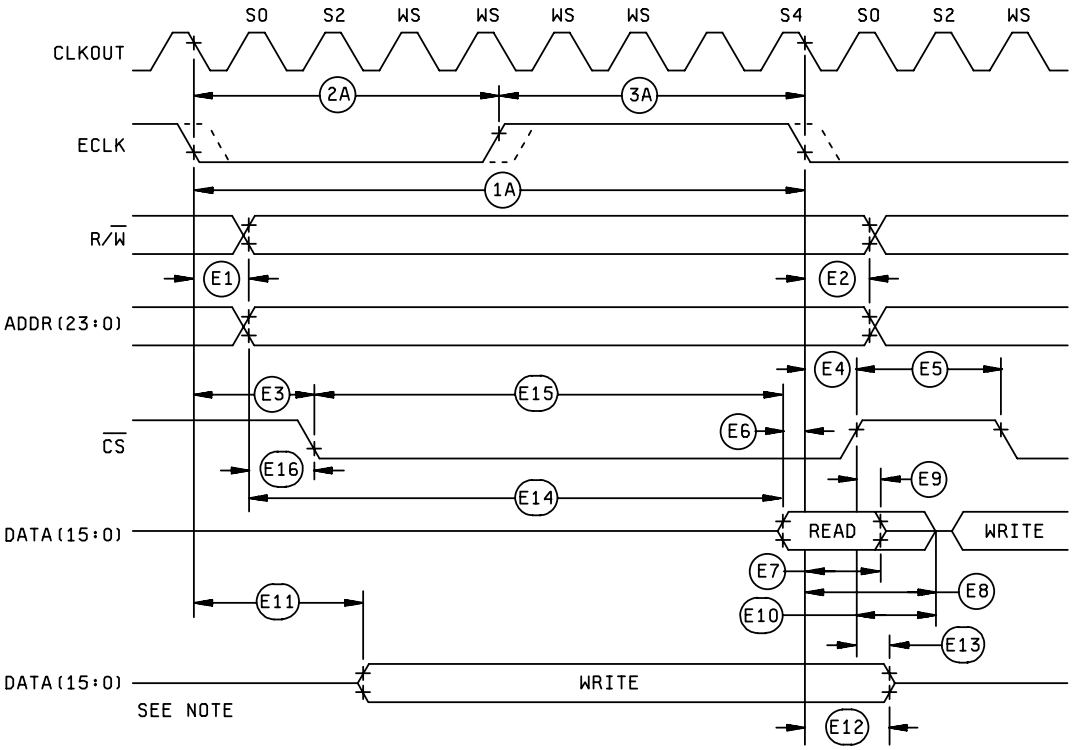


FIGURE 4. Timing waveforms - Continued.

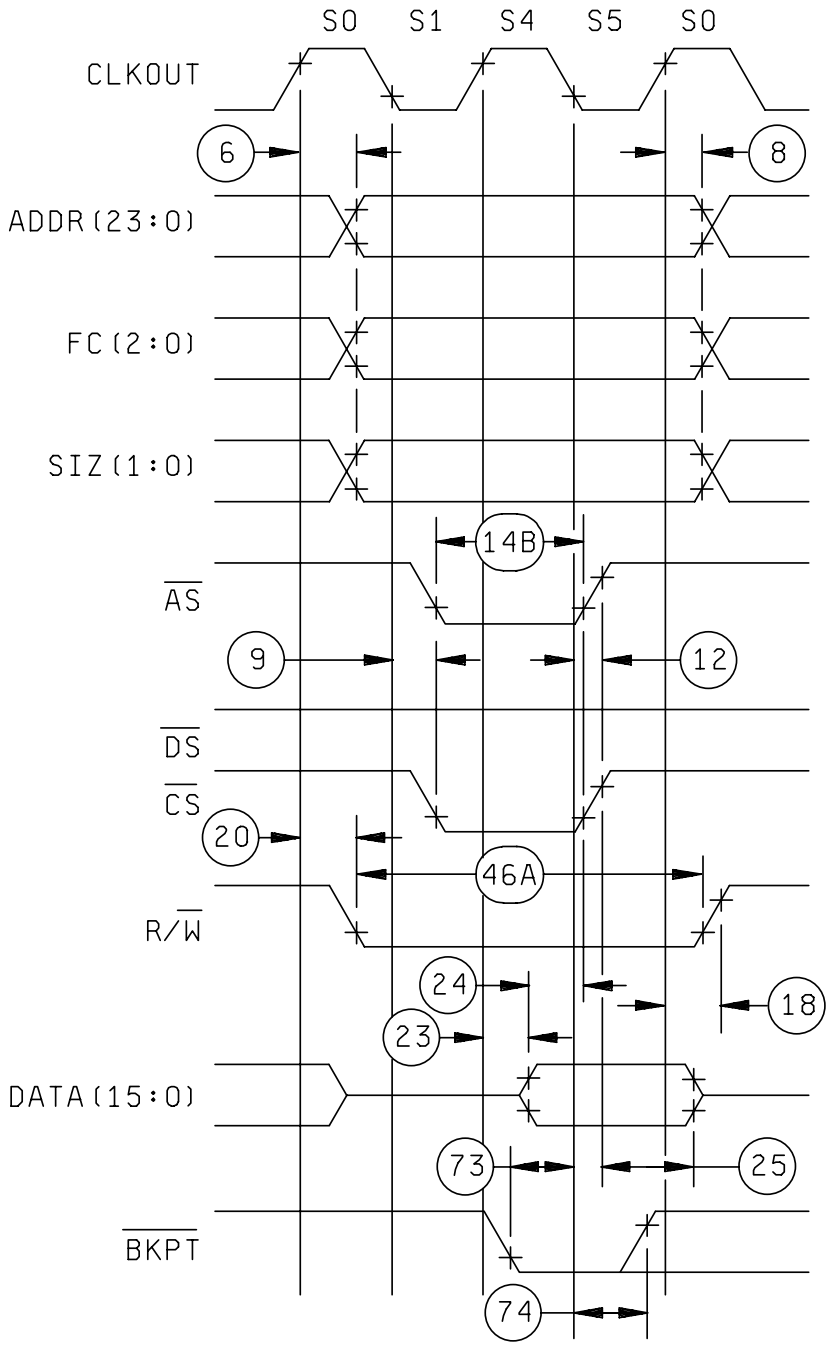


BUS ARBITRATION TIMING DIAGRAM - IDLE BUS CASE



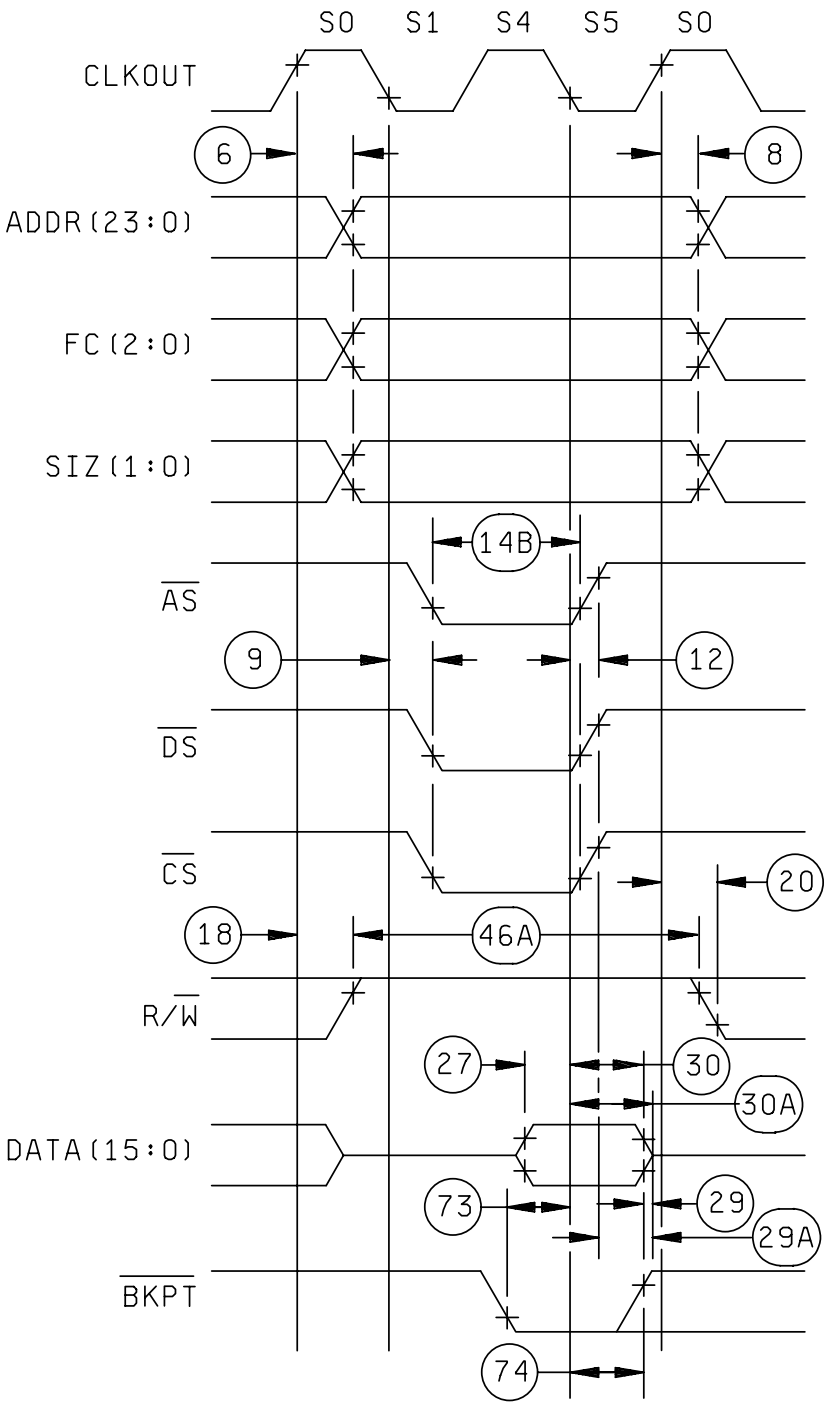
ECLK TIMING DIAGRAM

FIGURE 4. Timing waveforms - Continued.



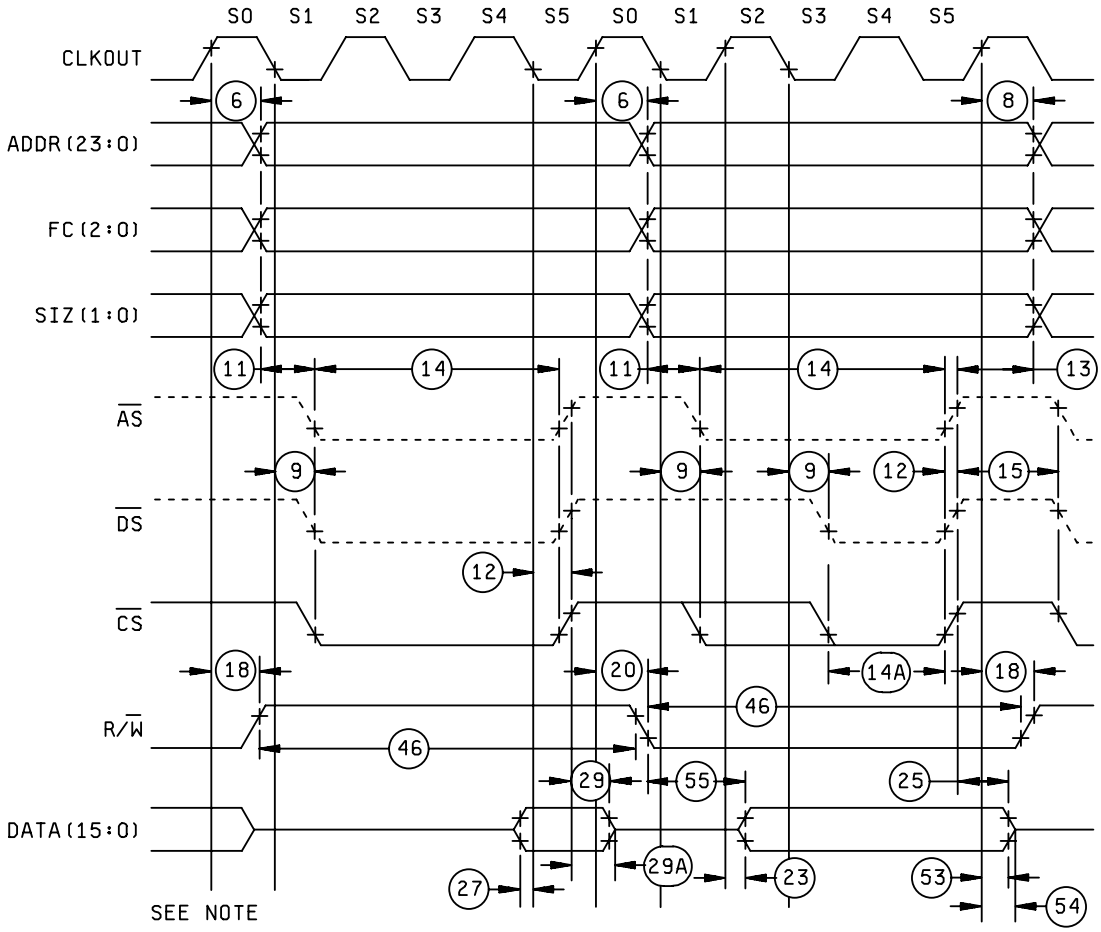
FAST TERMINATION WRITE CYCLE TIMING DIAGRAM

FIGURE 4. Timing waveforms - Continued.



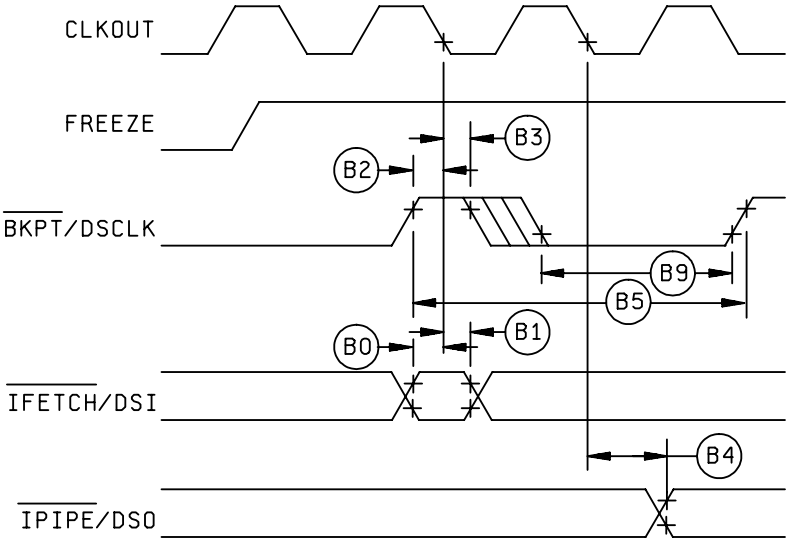
FAST TERMINATION READ CYCLE TIMING DIAGRAM

FIGURE 4. Timing waveforms - Continued.

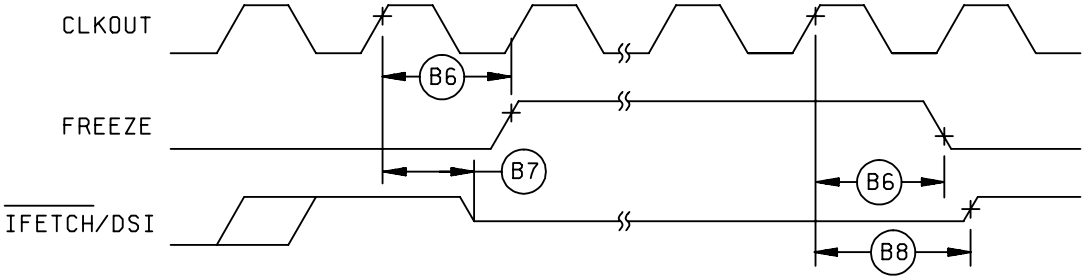


CHIP SELECT TIMING DIAGRAM

FIGURE 4. Timing waveforms - Continued.

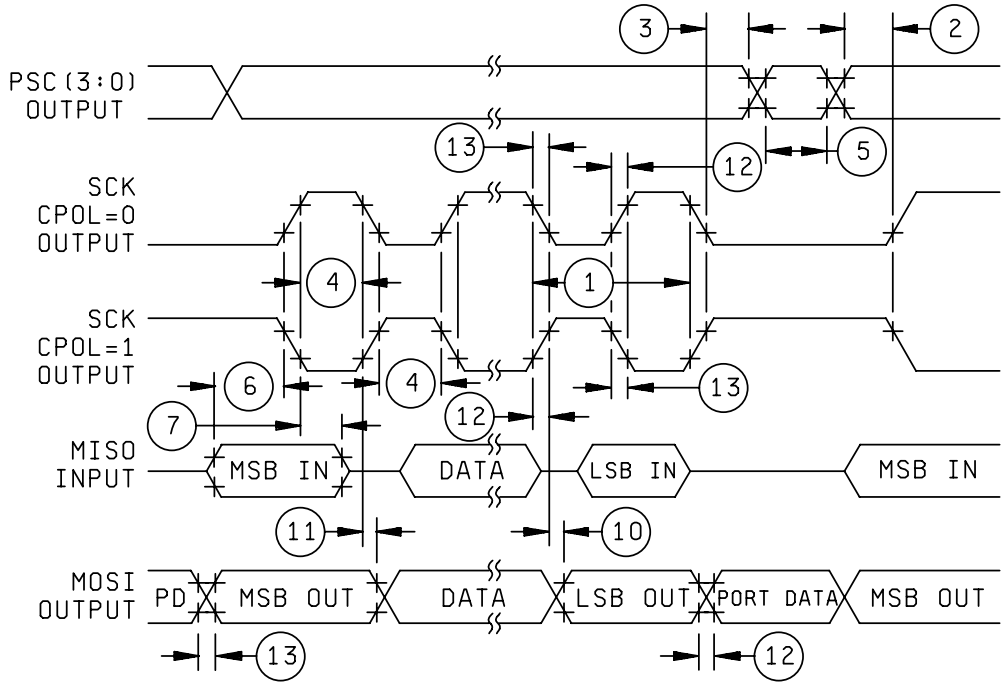


BACKGROUND DEBUGGING MODE TIMING DIAGRAM-
SERIAL COMMUNICATION

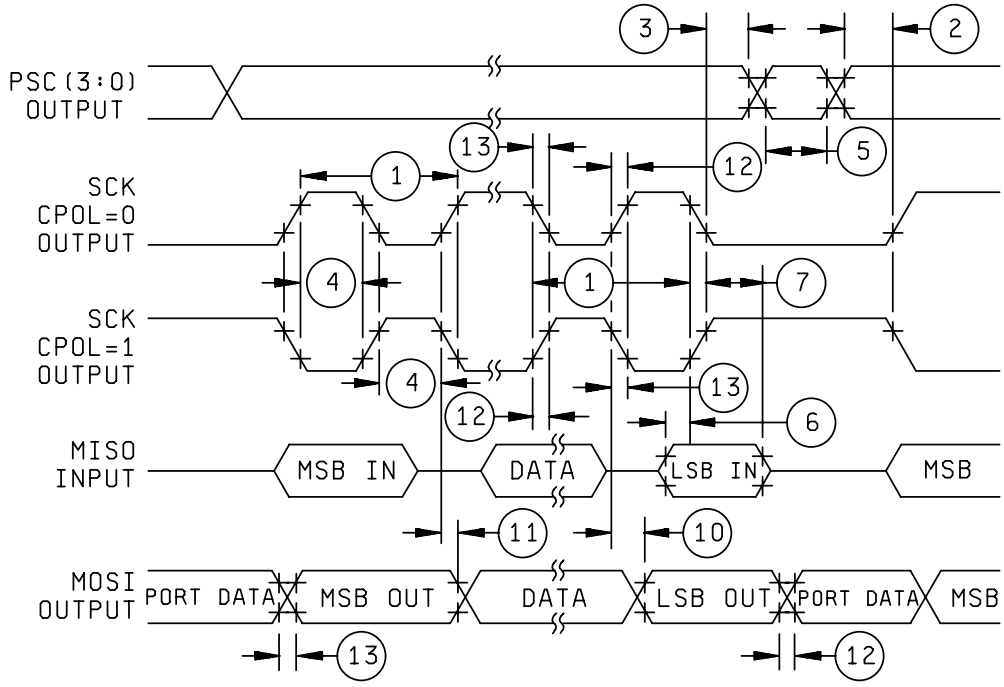


BACKGROUND DEBUGGING MODE TIMING DIAGRAM-
FREEZE ASSERTION

FIGURE 4. Timing waveforms - Continued.

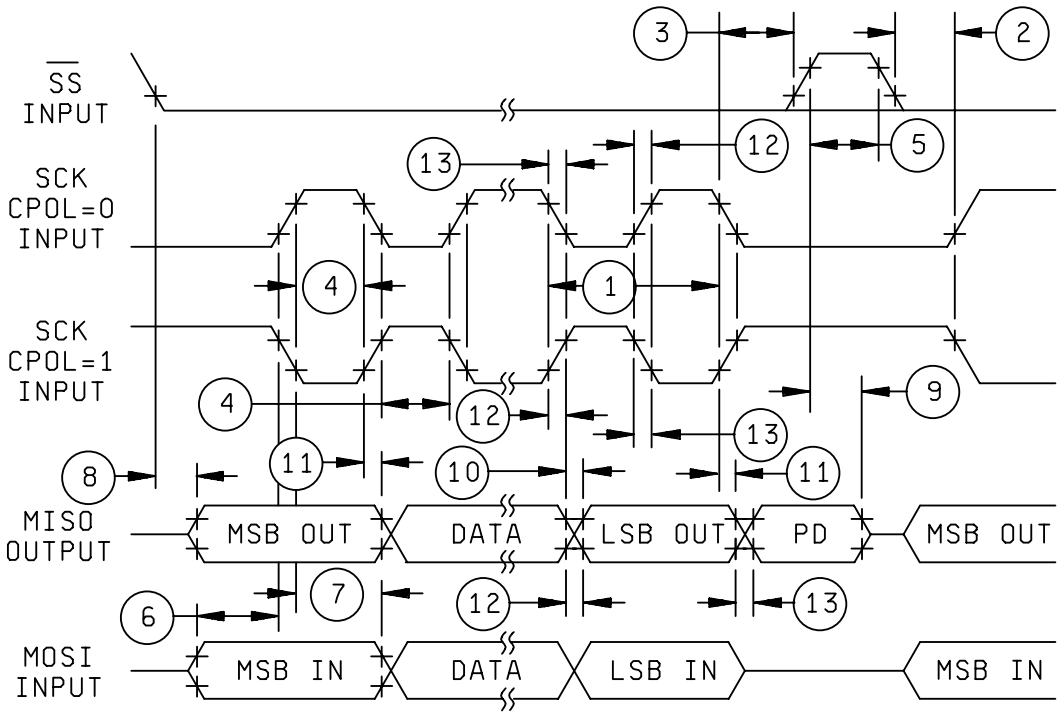


QSPI TIMING - MASTER, CPHA = 0



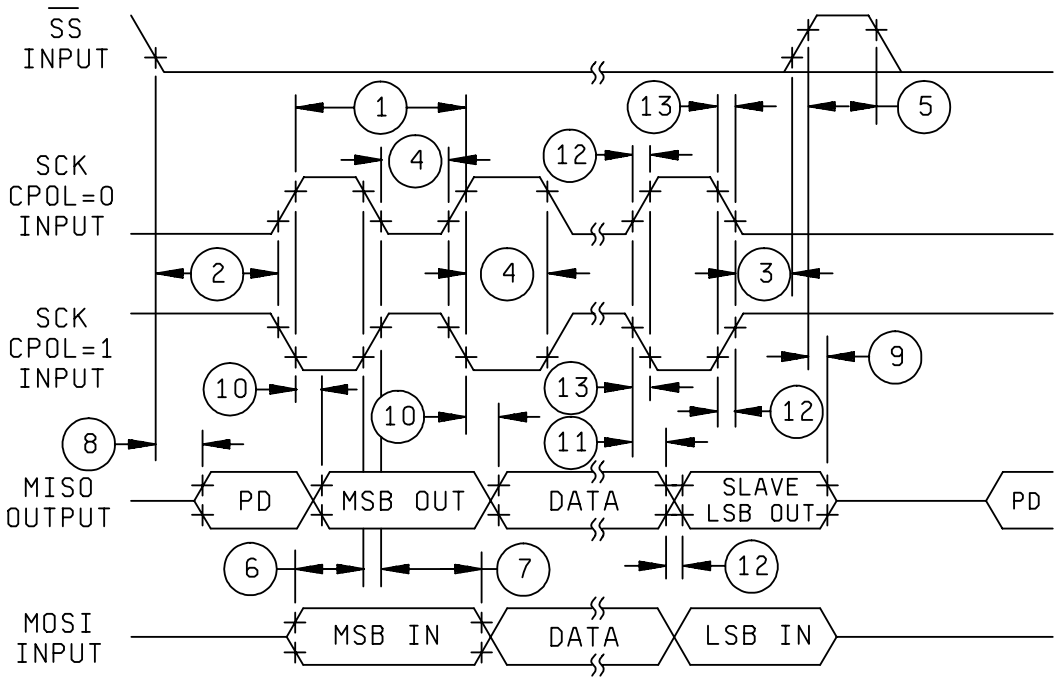
QSPI TIMING - MASTER, CPHA = 1

FIGURE 4. Timing waveforms - Continued.



QSPI TIMING - SLAVE,CPHA = 0

FIGURE 4. Timing waveforms - Continued.



QSPI TIMING - SLAVE,CPHA = 1

FIGURE 4. Timing waveforms - Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)		1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 05-10-04

Approved sources of supply for SMD 5962-91501 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9150101MXA	F8385	TS68332MAB/C16A
5962-9150101MYA	3/	68332-16
5962-9150101MZA	F8385	TS68332MR1B/C16A
5962-9150101MZC	F8385	TS68332MRB/C16A
5962-9150101QYC	3/	68332-16
5962-9150101QZA	3/	68332-16
5962-9150102MXA	F8385	TS68332MAB/C20A
5962-9150102MZA	F8385	TS68332MR1B/C20A
5962-9150102MZC	F8385	TS68332MRB/C20A

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
F8385	Atmel Grenoble Avenue De Rochepleine BP123 Saint Egreve CEDEX 38521, France