NOTICE OF REVISION (NOR)

This revision described below has been authorized for the document listed.

1. DATE: 93/11/04

Form Approved OMB No. 0704-0188

2. PROCURING ACTIVITY NO.

3. DODAAC

4. ORIGINATOR

a. TYPED NAME (First, Middle Initial, Last)

b. ADDRESS (Street, City, State, Zip Code)
Defense Electronics Supply Center
1507 Wilmington Pike
Dayton, OH 45444-5270

5. CAGE CODE: 67268

6. NOR NO.: 5962-R023-94

7. CAGE CODE: 67268

8. DOCUMENT NO.: 5962-90727

9. TITLE OF DOCUMENT
MICROCIRCUIT,DIGITAL CMOS GRAPHIC SYSTEM PROCESSOR, MONOLITHIC SILICON.

10. REVISION LETTER
a. CURRENT: initial
b. NEW: A

11. ECP NO.

12. CONFIGURATION ITEM (OR SYSTEM) TO WHICH ECP APPLIES
ALL

13. DESCRIPTION OF REVISION

Sheet 1: Revisions ltr column; add "A".
Revisions description column; add "Changes in accordance with NOR 5962-R023-94".
Revisions date column; add "93-11-04".
Revision level block; add "A".
Rev status of sheets; For sheets 1 and 29 add "A".

Sheet 29: Footnote 1/ change from: " All test to be performed at worst-case test conditions unless otherwise specified."

to: " All test to be performed at worst-case test conditions unless otherwise specified. At minimum frequency (t_Q period = 125 ns), both devices 01 and 02 are tested per the device 01 limits. At maximum frequency, devices are tested per their respective table I limits."

14. THIS SECTION FOR GOVERNMENT USE ONLY

a. (X one)		
	X	(1) Existing document supplemented by the NOR may be used in manufacture.
		(2) Revised document must be received before manufacturer may incorporate this change.
		(3) Custodian of master document shall make above revision and furnish revised document.

b. ACTIVITY AUTHORIZED TO APPROVE CHANGE FOR GOVERNMENT: DESC-ECC

c. TYPED NAME (First, Middle Initial, Last): Monica L. Poelking

d. TITLE: Chief, Custom Microelectronics

e. SIGNATURE: Monica L. Poelking

f. DATE SIGNED: 93/11/04

15a. ACTIVITY ACCOMPLISHING REVISION: DESC-ECC

b. REVISION COMPLETED (Signature): Jeffery Tunstall

c. DATE SIGNED: 93/11/04

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET	52	53	54	55	56	57	58	59	60	61									
REV																			
SHEET	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51
REV																			
SHEET	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32

REV STATUS OF SHEETS	REV													
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Jeffery Tunstall

CHECKED BY
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APPROVED BY
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DRAWING APPROVAL DATE
93-01-20

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, CMOS DIGITAL GRAPHIC SYSTEM PROCESSOR, MONOLITHIC SILICON

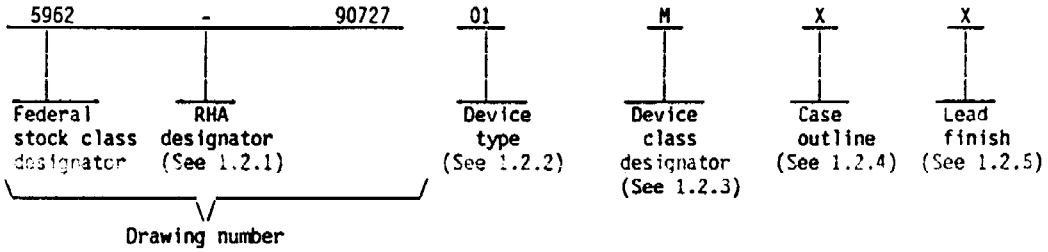
SIZE	CAGE CODE	5962-90727
A	67268	

SHEET 1 OF 61

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Cycle time	Circuit function
01	34010-40	200 ns	Graphic system processor
02	34010-50	160 ns	Graphic system processor

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Description designator	Terminals	Package style
X	CMGA15-P68	68	pin grid array package 1/
Y	CQCC1-N68	68	square chip carrier

1.3 Absolute maximum ratings.

Supply voltage (V_{CC}) 2/	7 V dc
Input voltage range	-0.3 V dc to 7 V dc
Output voltage range	-2 V dc to 7 V dc
Power disipation (P_D)	825 mW
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835

1/ Inactive for new design.
2/ All voltages are with respect to V_{SS}.

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Supply voltage range (V_{SS}) 1/	0 V dc
High level output current (I_{OH})	-400 µA
Low level output current (I_{OL})	2 mA
Operating case temperature(T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

1/ Care should be taken by card designers to provide a minimum inductance path between the V_{SS} pins and system ground in order to minimize V_{SS} noise.
2/ Values will be added when they become available.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-ECC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le VCC \le 5.5\ V$		Group A subgroups	Limits		Unit
					Min	Max	
High level input voltage	V_{IH}	V_{CC} = 4.5 to 5.5 V dc INCLK = 16 MHz	INCLK	1,2,3	3.2	V_{CC} + 0.3	V
			VCLK		2.4	V_{CC} + 0.3	
			All other pins		2.2	V_{CC} + 0.3	
Low level input voltage	V_{IL}	V_{CC} = 4.5 to 5.5 V dc INCLK = 16 MHz	LAD0-LAD15, HD0-HD15, HSNYC, VSYNC	1,2,3	-0.3	0.8	V
			All other pins		-0.3	0.6	
High level output voltage	V_{OH}	V_{CC} = 4.5 V dc	I_{OH} = -400 µA	1,2,3	2.6		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V dc I_{OL} = 2.0 mA	LCLK1, LCLK2, HRDY, HLDA/EMUA, HINT, BLANK	1,2,3		0.7	V
			All other pins			0.6	
High impedance leakage current, bidirectional pins	I_O	V_{CC} = 5.5 V dc	V_O = 2.8 V dc	1,2,3		20	µA
			V_O = 0.4 V dc			-20	
Input current 2/	I_I	$V_I = V_{SS}$ to V_{CC}	All inputs except RUN/EMU	1,2,3		±20	µA
Supply current	I_{CC}	V_{CC} = 5.5 V dc, 40 MHz		1,2,3		125	mA
		V_{CC} = 5.5 V dc, 50 MHz				150	
Functional Test		See 4.4.1b		7,8			
I/O capacitance	$C_{I/O}$	See 4.4.1c		4		28	pf
Input capacitance	C_{IN}	Except address/data lines See 4.4.1c	V_{CC} = 5.0 V	4		15	pf
Output capacitance	C_O	Except address/data lines See 4.4.1c	V_{CC} = 5.0 V	4		23	pf

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device types	Group A subgroups	Limits		Unit
					Min	Max	
Setup time of $\overline{\text{HWRITE}}$/HREAD high or HFSO, HFS1 valid to read or write strobe ↓	1 See figs. 3,4,5,8	V_{CC} = 4.5 V	All	9,10,11	10		ns
Delay from write strobe ↓ to data in valid, write cycle	2 See fig. 3,5		All	9,10,11		$2t_Q$	ns
Delay from read or write strobe low to next read or write strobe ↓	3 See figs. 3,4,5,8		All	9,10,11	$7t_Q$+10		ns
Duration of read or write strobe low	4 See figs. 3,4,5,8		All	9,10,11	80		ns
Delay from read or write strobe high to next read or write strobe ↓	5 See figs. 3,4,5,8		All	9,10,11	60		ns
Hold time of data in valid after write strobe high, write cycle	6 See fig. 3,5		All	9,10,11	10		ns
Hold time of $\overline{\text{HWRITE}}$/$\overline{\text{HREAD}}$ high or HFSO, HFS1 valid after read or write strobe high	7 See figs. 3,4,5,8		All	9,10,11	10		ns
Hold time of data high 4/ impedance after read strobe ↓, read cycle	8 See figs. 4,8		All	9,10,11	0		ns
Delay time from read strobe low to data out valid, read cycle with no wait	9 See fig. 4		All	9,10,11		90	ns
Hold time of data out valid after read strobe ↑ read cycle	10 See figs. 4,8		All	9,10,11	0		ns
Delay from read strobe 4/ high to data out high impedance, read cycle	11 See figs. 4,8		All	9,10,11		30	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Hold time of HRDY high after $\overline{HCS}$ ↓, cycle with wait	12 See figs. 5,8	V_{CC} = 4.5 V	All	9,10,11	0		ns
Delay from $\overline{HCS}$ low to HRDY low, cycle with wait	13 See figs. 5,8		All	9,10,11		40	ns
Hold time of write strobe low after HRDY ↑, write cycle with wait	16 See fig. 5		All	9,10,11	40		ns
Delay from HRDY ↑ to data out valid, read cycle with wait	17 See fig. 8		All	9,10,11		40	ns
Hold time of read strobe low after HRDY ↑, read cycle with wait	18 See fig. 8		All	9,10,11	40		ns
Duration of $\overline{HCS}$ low to configure GSP to run in self-bootstrap mode	19 See fig. 7		All	9,10,11	$4t_Q+55$		ns
Setup time of $\overline{HCS}$ low to $\overline{RESET}$ ↑ to configure the GSP to run in self-bootstrap mode	20 See fig. 7		All	9,10,11	$8t_Q+55$		ns
Duration of $\overline{RESET}$ low to ensure that GSP is properly reset	21 See fig. 7		All	9,10,11	$160t_Q$ - 40		ns
Delay from $\overline{HCS}$ ↑ to 5/ $\overline{RESET}$ high, end of reset, to configure GSP to run in self-bootstrap mode	22 See fig. 7		All	9,10,11		$4t_Q-50$	ns
Setup time of $\overline{RESET}$ 6/ valid to LCLK1 ↓ to guarantee recognition at a particular clock edge	23 See fig. 9		All	9,10,11	40		ns
Hold time of $\overline{RESET}$ 6/ valid after LCLK1 low to guarantee recognition at a particular clock edge	24 See fig. 9		All	9,10,11	10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device types	Group A subgroups	Limits Min	Limits Max	Unit
6/ Setup time of $\overline{HCS}$ valid to LCLK1 ↓ to guarantee recognition at a particular clock edge	25 See fig. 9	V_{CC} = 4.5 V	All	9,10,11	40		ns
Hold time of $\overline{HCS}$ valid 6/ after LCLK1 low to guarantee recognition at a particular clock edge	26 See fig. 9		All	9,10,11	10		ns
Period of INCLK	27 See fig. 6		01	9,10,11	25	62.5	ns
			02	9,10,11	20	62.5	ns
Pulse duration of INCLK high	28 See fig. 6	V_{IN} = 1.4 V dc	All	9,10,11	8		ns
Pulse duration of INCLK low	29 See fig. 6	V_{CC} = 4.5 V	All	9,10,11	8		ns
Pulse duration of local clock high	32 See fig. 10	V_{CC} = 4.5 V	All	9,10,11	$2t_Q$-10		ns
Pulse duration of local clock low	33 See fig. 10		All	9,10,11	$2t_Q$-10		ns
Hold time of LCLK2 low after LCLK1 high	34 See fig. 10		All	9,10,11	t_Q-10		ns
Hold time of LCLK2 high after LCLK1 low	35 See fig. 10		All	9,10,11	t_Q-10		ns
Hold time of LCLK1 high after LCLK2 high	36 See fig. 10		All	9,10,11	t_Q-10		ns
Hold time of LCLK1 low after LCLK2 low	37 See fig. 10		All	9,10,11	t_Q-10		ns
Hold time of LCLK2 high after LCLK1 high	38 See fig. 10		All	9,10,11	$3t_Q$-10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Hold time of LCLK2 low after LCLK1 low	39 See fig. 10	V_{CC} = 4.5 V	All	9,10,11	$3t_Q$-10		ns
Hold time of LCLK1 low after LCLK2 high	40 See fig. 10		All	9,10,11	$3t_Q$-10		ns
Hold time of LCLK1 high after LCLK2 low	41 See fig. 10		All	9,10,11	$3t_Q$-10		ns
Transition time (rise and fall) of LCLK1 or LCLK2	42 See fig. 10		All	9,10,11		10	ns
Setup time of row address valid to LCLK2 ↑	43 See fig. 10		01	9,10,11	$4t_Q$-25		ns
			02	9,10,11	$4t_Q$-15		ns
Setup time of column address valid to LCLK2 ↑	44 See fig. 10		01	9,10,11	$2t_Q$-25		ns
			02	9,10,11	$2t_Q$-15		ns
Setup time of LRDY 7/ valid to LCLK2 ↑	45 See fig. 10		All	9,10,11	30		ns
Hold time of LRDY valid 7/ LCLK2 high	46 See fig. 10		All	9,10,11	0		ns
Setup time of row address valid to LCLK1 ↓	47 See fig. 10		01	9,10,11	t_Q-25		ns
			02	9,10,11	t_Q-15		ns
Setup time of column address valid to LCLK1 ↑	48 See fig. 10		01	9,10,11	t_Q-25		ns
			02	9,10,11	t_Q-15		ns
Setup time of $\overline{LAL}$ high to LCLK1 ↓	49 See fig. 10		01	9,10,11	$2t_Q$-20		ns
			02	9,10,11	$2t_Q$-10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Setup time of row address valid to $\overline{RAS}$ ↓	51 See fig. 11	V_{CC} = 4.5 V	01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-15		ns
Hold time of row address valid after $\overline{RAS}$ low	52 See fig. 11		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Pulse duration, $\overline{RAS}$ high	53 See fig. 11		01	9,10,11	$3t_Q$-20		ns
			02	9,10,11	$3t_Q$-10		ns
Pulse duration, $\overline{RAS}$ low	54 See Fig 11		01	9,10,11	$5t_Q$-20		ns
			02	9,10,11	$5t_Q$-10		ns
Setup time of column address valid to $\overline{LAL}$ ↓	55 See fig. 11		01	9,10,11	$0.5t_Q$-20		ns
			02	9,10,11	$0.5t_Q$-10		ns
Hold time of column address valid after $\overline{LAL}$ low	56 See fig. 11		01	9,10,11	$0.5t_Q$-15		ns
			02	9,10,11	$0.5t_Q$-10		ns
Hold time of $\overline{RAS}$ high after $\overline{LAL}$ high	57 See fig. 11		01	9,10,11	$2t_Q$-20		ns
			02	9,10,11	$2t_Q$-10		ns
Hold time of $\overline{LAL}$ low after $\overline{RAS}$ low	58 See fig. 11		01	9,10,11	$6t_Q$-20		ns
			02	9,10,11	$6t_Q$-10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Hold time of $\overline{RAS}$ low after $\overline{CAS}$ low	59 See fig. 11	V_{CC} = 4.5 V	01	9,10,11	$3t_Q$-20		ns
			02	9,10,11	$3t_Q$-10		ns
Hold time of $\overline{W}$ high after $\overline{RAS}$ high, shift register transfer follows read	60 See fig. 11		01	9,10,11	$2t_Q$-20		ns
			02	9,10,11	$2t_Q$-10		ns
Setup time of column address valid to $\overline{CAS}$ ↓	61 See fig. 11		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{LAL}$ low after $\overline{CAS}$ low	62 See fig. 11		01	9,10,11	$4t_Q$-20		ns
			02	9,10,11	$4t_Q$-10		ns
Hold time of $\overline{LAL}$ low after $\overline{CAS}$ high, write cycle	63 See fig. 11,17		01	9,10,11	$0.5t_Q$-15		ns
			02	9,10,11	$0.5t_Q$-10		ns
Hold time of $\overline{CAS}$ high after $\overline{LAL}$ low	64 See fig. 11		01	9,10,11	$0.5t_Q$-15		ns
			02	9,10,11	$0.5t_Q$-10		ns
Hold time of $\overline{RAS}$ high after $\overline{CAS}$ high	65 See fig. 11		01	9,10,11	$2.5t_Q$-15		ns
			02	9,10,11	$2.5t_Q$-10		ns
Pulse duration, $\overline{CAS}$ low	66 See fig. 11		01	9,10,11	$3.5t_Q$-25		ns
			02	9,10,11	$3.5t_Q$-10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Hold time of $\overline{CAS}$ high after $\overline{RAS}$ low	67 See fig. 11	V_{CC} = 4.5 V	01	9,10,11	$2t_Q$-20		ns
			02	9,10,11	$2t_Q$-10		ns
Delay time from $\overline{RAS}$ low to $\overline{CAS}$ low	68 See fig. 11		01	9,10,11		$2t_Q$+20	ns
			02	9,10,11		$2t_Q$+10	ns
Hold time of $\overline{W}$ high after $\overline{CAS}$ high, shift register transfer follows read	69 See fig. 11		01	9,10,11	$1.5t_Q$-15		ns
			02	9,10,11	$1.5t_Q$-10		ns
Hold time of $\overline{CAS}$ low after $\overline{RAS}$ low	70 See fig. 11		01	9,10,11	$5.5t_Q$-25		ns
			02	9,10,11	$5.5t_Q$-10		ns
Pulse duration, $\overline{CAS}$ high	71 See fig. 11		01	9,10,11	$4.5t_Q$-15		ns
			02	9,10,11	$4.5t_Q$-10		ns
Hold time of $\overline{CAL}$ low after $\overline{W}$ high, write cycle	72 See fig. 11		01	9,10,11	$0.5t_Q$-15		ns
			02	9,10,11	$0.5t_Q$-10		ns
Setup time of $\overline{W}$ high to $\overline{CAS}$, end of write	73 See fig. 11		01	9,10,11	$4.5t_Q$-15		ns
			02	9,10,11	$4.5t_Q$-10		ns
Setup time of $\overline{W}$ low to $\overline{RAS}$, shift register transfer cycle	74 See fig. 12		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Hold time of $\overline{W}$ low after $\overline{RAS}$ low, shift register transfer cycle	75 See fig. 12	V_{CC} = 4.5 V	01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Setup time of $\overline{TR}/\overline{QE}$ low to $\overline{RAS}$ ↓, shift register transfer cycle	76 See fig. 12		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{TR}/\overline{QE}$ low after $\overline{RAS}$ low, shift register transfer cycle	77 See fig. 12		01	9,10,11	$4t_Q$-20		ns
			02	9,10,11	$4t_Q$-10		ns
Hold time of $\overline{TR}/\overline{QE}$ low after $\overline{CAS}$ low, shift register transfer cycle	78 See fig. 12		01	9,10,11	$2t_Q$-20		ns
			02	9,10,11	$2t_Q$-10		ns
Setup time of $\overline{TR}/\overline{QE}$ high to $\overline{RAS}$ ↑, shift register transfer cycle	79 See fig. 12		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Setup time of $\overline{TR}/\overline{QE}$ high to $\overline{CAS}$ ↑, shift register transfer cycle	80 See fig. 12		01	9,10,11	$1.5t_Q$-25		ns
			02	9,10,11	$1.5t_Q$-10		ns
Access time from $\overline{RAS}$ low to data in valid, read cycle 8/	83 See fig. 13		01	9,10,11		$5.5t_Q$-40	ns
			02	9,10,11		$5.5t_Q$-25	ns
Setup time of $\overline{CAS}$ high to $\overline{LAL}$ ↑	84 See fig. 13		01	9,10,11	$0.5t_Q$-15		ns
			02	9,10,11	$0.5t_Q$-10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Setup time of $\overline{DEN}$ high to $\overline{LAL}$	85 See fig. 13	V_{CC} = 4.5 V	01	9,10,11	$0.5t_Q$-15		ns
			02	9,10,11	$0.5t_Q$-10		ns
Access time from $\overline{CAS}$ low to data in valid, read cycle 6/	86 See fig. 13		01	9,10,11		$3.5t_Q$-40	ns
			02	9,10,11		$3.5t_Q$-25	ns
Hold time of data in valid after $\overline{CAS}$, read cycle	87 See fig. 13		01	9,10,11	0		ns
			02	9,10,11	0		ns
Hold time of row address high impedance after $\overline{CAS}$ high, end of read cycle 4/	88 See fig. 13		All	9,10,11	$1.5t_Q$-10		ns
Hold time of $\overline{TR/QE}$ low after $\overline{CAS}$ low, read cycle	89 See fig. 13		01	9,10,11	$3.5t_Q$-25		ns
			02	9,10,11	$3.5t_Q$-10		ns
Setup time of column address high impedance to $\overline{TR/QE}$, read cycle 4/	90 See fig. 13		All	9,10,11	t_Q-10		ns
Hold time of data in valid after $\overline{TR/QE}$, read cycle	91 See fig. 13		All	9,10,11	0		ns
Delay time from $\overline{CAS}$ to $\overline{TR/QE}$ low, read cycle	92 See fig. 13		01	9,10,11		t_Q+20	ns
			02	9,10,11		t_Q+10	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Access time from $\overline{TR}/\overline{QE}$ low to data in valid, read cycle 8/	93 See fig. 13	V_{CC} = 4.5 V	01	9,10,11		$2.5t_Q$-40	ns
			02	9,10,11		$2.5t_Q$-25	ns
Hold time of row address high impedance after $\overline{TR}/\overline{QE}$ high, end of read cycle 4/	94 See figs. 13		All	9,10,11	$1.5t_Q$-10		ns
Pulse duration, $\overline{TR}/\overline{QE}$ low read cycle	95 See figs. 13		01	9,10,11	$2.5t_Q$-25		ns
			02	9,10,11	$2.5t_Q$-10		ns
Delay time from $\overline{CAS}$ low to $\overline{DEN}$ low, read cycle	96 See figs. 13		01	9,10,11		t_Q+20	ns
			02	9,10,11		t_Q+10	ns
Hold time of data in valid after $\overline{DEN}$ ↑, read cycle	97 See fig. 13		All	9,10,11	0		ns
Setup time of column address high impedance to $\overline{DEN}$ ↓, read cycle 4/	98 See figs. 13		All	9,10,11	t_Q-10		ns
Hold time of next row address high impedance after $\overline{DEN}$ high, end of read cycle 4/	99 See fig. 13		All	9,10,11	$1.5t_Q$-10		ns
Access time from $\overline{DEN}$ low 8/ to data valid, read cycle	100 See fig. 13		01	9,10,11		$2.5t_Q$-40	ns
			02	9,10,11		$2.5t_Q$-25	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Hold time of DDOUT high after DEN high, read follows write cycle	101 See fig. 13	V_{CC} = 4.5 V	01	9,10,11	$3t_Q$-20		ns
			02	9,10,11	$3t_Q$-10		ns
Setup time of DDOUT low to DEN ↓, read cycle	102 See fig. 13		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of DDOUT low after DEN high, read cycle	103 See fig. 13		01	9,10,11	$1.5t_Q$-15		ns
			02	9,10,11	$1.5t_Q$-10		ns
Setup time of data out valid to W ↓, write cycle	104 See fig. 14		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-15		ns
Hold time of data out valid after W low, write cycle	105 See fig. 14		01	9,10,11	$4t_Q$-20		ns
			02	9,10,11	$4t_Q$-10		ns
Setup time of W low to RAS ↑, write cycle	106 See fig. 14		01	9,10,11	$2t_Q$-20		ns
			02	9,10,11	$2t_Q$-10		ns
Hold time of data out valid after RAS low, write cycle	107 See fig. 14		01	9,10,11	$7t_Q$-20		ns
			02	9,10,11	$7t_Q$-10		ns
Hold time of data out valid after CAS high, write cycle	108 See fig. 14		01	9,10,11	$1.5t_Q$-15		ns
			02	9,10,11	$1.5t_Q$-10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Setup time of $\overline{W}$ low to CAS ↑, write cycle	109 See fig. 14	V_{CC} = 4.5 V	01	9,10,11	$2.5t_Q$-25		ns
			02	9,10,11	$2.5t_Q$-10		ns
Hold time of data out valid after CAS low, write cycle	110 See fig. 14		01	9,10,11	$5t_Q$-20		ns
			02	9,10,11	$5t_Q$-10		ns
Hold time of data out valid after $\overline{W}$ high, write cycle	111 See fig. 14		01	9,10,11	$1.5t_Q$-15		ns
			02	9,10,11	$1.5t_Q$-10		ns
Pulse duration, $\overline{W}$ low	112 See fig. 14		01	9,10,11	$2.5\ t_Q$-25		ns
			02	9,10,11	$2.5t_Q$-10		ns
Hold time of $\overline{W}$ low after CAS low, write cycle	113 See fig. 14		01	9,10,11	$3.5t_Q$-25		ns
			02	9,10,11	$3.5t_Q$-10		ns
Setup time of column address valid to $\overline{W}$ ↑, write cycle	114 See fig. 14		01	9,10,11	$4.5t_Q$-30		ns
			02	9,10,11	$4.5t_Q$-15		ns
Hold time of $\overline{W}$ low after RAS low, write cycle	115 See fig. 14		01	9,10,11	$5.5t_Q$-25		ns
			02	9,10,11	$5.5t_Q$-10		ns
Setup time of row address valid to $\overline{W}$ ↑, write cycle	116 See fig. 14		01	9,10,11	$6.5t_Q$-35		ns
			02	9,10,11	$6.5t_Q$-15		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Setup time of $\overline{DEN}$ low to W ↓, write cycle	117 See fig. 14	V_{CC} = 4.5 V	01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{DEN}$ low after W high, write cycle	118 See fig. 14		01	9,10,11	$1.5t_Q$-15		ns
			02	9,10,11	$1.5t_Q$-10		ns
Setup time of DDOUT high to $\overline{DEN}$ ↓, write follows read	119 See fig. 14		01	9,10,11	$3t_Q$-20		ns
			02	9,10,11	$3t_Q$-10		ns
Setup time of $\overline{HOLD}$ valid to LCLK2 ↑ 9/	120 See figs. 15, 16		01	9,10,11	50		ns
			02	9,10,11	40		ns
Hold time of $\overline{HOLD}$ valid 9/ after LCLK2 high	121 See figs. 15, 16		All	9,10,11	0		ns
Setup time of $\overline{HLDA}$/$\overline{EMUA}$ output valid before LCLK2 ↓	122 See figs. 15, 16		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{HLDA}$/$\overline{EMUA}$ low, after LCLK2 low	123 See figs. 15, 16		All	9,10,11	t_Q-15		ns
Setup time of $\overline{RAS}$ high to LCLK1 ↑	125 See fig. 15		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Hold time of $\overline{RAS}$ driven 4/ high after LCLK1 high, bus release	126 See fig. 15	V_{CC} = 4.5	All	9,10,11	t_Q-10		ns
Delay from LCLK2 high to $\overline{RAS}$ high impedance, 4/ bus release	127 See fig. 15		All	9,10,11		30	ns
Setup time of $\overline{LAL}$ high to LCLK2 ↑	128 See fig. 15		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{LAL}$ driven 4/ high after LCLK1 ↓, bus release	129 See fig. 15		All	9,10,11	-5		ns
Delay from LCLK1 low to 4/ $\overline{LAL}$ high impedance, bus release	130 See fig. 15		All	9,10,11		30	ns
Setup time of $\overline{CAS}$, $\overline{W}$, and TR/$\overline{QE}$ high to LCLK1 ↓	131 See fig. 15		01	9,10,11	$0.5t_Q$-15		ns
			02	9,10,11	$0.5t_Q$-10		ns
Hold time of $\overline{CAS}$, $\overline{W}$, and TR/$\overline{QE}$ high after LCLK1 high, bus release 4/	132 See fig. 15		All	9,10,11	t_Q-10		ns
Delay from LCLK2 high to 4/ $\overline{CAS}$, $\overline{W}$, and TR/$\overline{QE}$ high impedance, bus release	133 See fig. 15		All	9,10,11		30	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ 3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Setup time of $\overline{DEN}$ or DDOUT high to LCLK1 ↓	134 See fig. 15	V_{CC} = 4.5 V	01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{DEN}$ and DDOUT high after LCLK1 ↓ 4/ bus release	135 See fig. 15		All	9,10,11	t_Q-10		ns
Delay from LCLK1 low to $\overline{DEN}$ and DDOUT high impedance, bus release	136 See fig. 15		All	9,10,11		30	ns
Hold time of LAD bus high impedance after LCLK2 ↑ 4/	137 See fig. 16		All	9,10,11	-5		ns
Hold time of $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{LAL}$, and $\overline{TR/QE}$ high impedance after LCLK1 ↑ 4/	138 See fig. 16		All	9,10,11	-5		ns
Delay from LCLK1 high to $\overline{RAS}$, $\overline{CAS}$, $\overline{W}$, $\overline{LAL}$, and $\overline{TR/QE}$ driven high, resume bus control	139 See fig. 16		All	9,10,11		30	ns
Hold time of $\overline{RAS}$ high after LCLK2 high, resumes bus control	140 See fig. 16		01	9,10,11	t_Q-15		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{DEN}$, DDOUT high impedance after LCLK2 high, resumes bus control 4/	142 See fig. 16		All	9,10,11	-5		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Delay from LCLK2 high to DEN, and DDOUT driven high, resumes bus control	See fig. 16	V_{CC} = 4.5 V	All	9,10,11		30	ns
Setup time of row address valid to RAS ↓, CAS-before-RAS refresh	See fig. 17		01	9,10,11	$2t_Q$-25		ns
			02	9,10,11	$2t_Q$-15		ns
Hold time of row address valid after RAS low CAS-before-RAS refresh	See fig. 17		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Pulse duration, RAS high, start of CAS-before-RAS refresh	See fig. 17		01	9,10,11	$4t_Q$-20		ns
			02	9,10,11	$4t_Q$-10		ns
Pulse duration, RAS low, CAS-before-RAS refresh	See fig. 17		01	9,10,11	$4t_Q$-20		ns
			02	9,10,11	$4t_Q$-10		ns
Setup time of row address valid to LAL ↓, CAS-before-RAS refresh	See fig. 17		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-15		ns
Hold time of row address valid after LAL low, CAS-before-RAS refresh	See fig. 17		01	9,10,11	$2t_Q$-20		ns
			02	9,10,11	$2t_Q$-10		ns
Hold time of RAS high after LAL low, CAS-before RAS refresh	See fig. 17		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Setup time of $\overline{RAS}$ high to $\overline{LAL}$ ↑, $\overline{CAS}$-before-$\overline{RAS}$ refresh	151 See fig. 17	V_{CC} = 4.5 V	01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Setup time of $\overline{LAL}$ high to $\overline{CAS}$ ↓, $\overline{CAS}$-before-$\overline{RAS}$ refresh	152 See fig. 17		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Setup time of $\overline{CAS}$ low to $\overline{LAL}$ ↓, $\overline{CAS}$-before-$\overline{RAS}$ refresh	153 See fig. 17		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Setup time of $\overline{RAS}$ high to $\overline{CAS}$ ↓, $\overline{CAS}$-before-$\overline{RAS}$ refresh	154 See fig. 17		01	9,10,11	$2t_Q$-20		ns
			02	9,10,11	$2t_Q$-10		ns
Setup time of $\overline{CAS}$ low to $\overline{RAS}$ ↑, $\overline{CAS}$-before-$\overline{RAS}$ refresh	155 See fig. 17		01	9,10,11	$2t_Q$-20		ns
			02	9,10,11	$2t_Q$-10		ns
Hold time of $\overline{CAS}$ low after $\overline{RAS}$ low, $\overline{CAS}$-before $\overline{RAS}$ refresh	156 See fig. 17		01	9,10,11	$4.5t_Q$-25		ns
			02	9,10,11	$4.5t_Q$-10		ns
Pulse duration, $\overline{CAS}$ low, $\overline{CAS}$-before-$\overline{RAS}$ refresh	157 See fig. 17		01	9,10,11	$6.5t_Q$-25		ns
			02	9,10,11	$6.5t_Q$-10		ns
Setup time of $\overline{CAS}$ high to $\overline{RAS}$ ↓, $\overline{CAS}$-before-$\overline{RAS}$ refresh	158 See fig. 17		01	9,10,11	$3.5t_Q$-15		ns
			02	9,10,11	$3.5t_Q$-10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$		Group A subgroups	Limits		Unit
					Min	Max	
Hold time of $\overline{RAS}$ high after LCLK2 high, all cycles except internal and CAS-before-RAS refresh	159 See fig. 18	V_{CC} = 4.5 V	Device types 01	9,10,11	t_Q-15		ns
			02	9,10,11	t_Q-10		ns
Setup time of $\overline{RAS}$ low to LCLK2 ↓, all cycles except internal and CAS-before-RAS refresh	160 See fig. 18		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{RAS}$ high after LCLK1 low, CAS-before-RAS refresh	161 See fig. 18		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Setup time of $\overline{RAS}$ low to LCLK1 ↑, CAS-before-RAS refresh	162 See fig. 18		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{RAS}$ low after LCLK1 low, all cycles except internal	163 See fig. 18		01	9,10,11	t_Q-15		ns
			02	9,10,11	t_Q-10		ns
Setup time of $\overline{RAS}$ high to LCLK1 ↑, all cycles except internal	164 See fig. 18		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{LAL}$ high after LCLK2 low, all cycles except internal	165 See fig. 18		01	9,10,11	$0.5t_Q$-15		ns
			02	9,10,11	$0.5t_Q$-10		ns
Setup time of $\overline{LAL}$ low to LCLK1 ↑, all cycles except internal	166 See fig. 18		01	9,10,11	$0.5t_Q$-15		ns
			02	9,10,11	$0.5t_Q$-10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Hold time of $\overline{LAL}$ low after LCLK2 low, all cycles except internal	167 See fig. 18	V_{CC} = 4.5 V	01	9,10,11	t_Q-15		ns
			02	9,10,11	t_Q-10		ns
Setup time of $\overline{LAL}$ high after LCLK2 ↑, all cycles except internal	168 See fig. 18		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{CAS}$ high after LCLK2 ↑, $\overline{CAS}$-before $\overline{RAS}$ refresh	169 See fig. 18		01	9,10,11	t_Q-15		ns
			02	9,10,11	t_Q-10		ns
Setup time of $\overline{CAS}$ low to LCLK ↓, $\overline{CAS}$-before-$\overline{RAS}$ refresh	170 See fig. 18		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{CAS}$ high after LCLK2 low, all cycles except internal DRAM refresh and $\overline{CAS}$-before-$\overline{RAS}$ refresh	171 See fig. 18		01	9,10,11	t_Q-15		ns
			02	9,10,11	t_Q-10		ns
Setup time of $\overline{CAS}$ low to LCLK2 ↑, all cycles except internal DRAM refresh and $\overline{CAS}$-before-$\overline{RAS}$ refresh	172 See fig. 18		C1	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{CAS}$ low after LCLK2 low, all cycles except internal and DRAM refresh	173 See fig. 18		01	9,10,11	$0.5t_Q$-15		ns
			02	9,10,11	$0.5t_Q$-10		ns
Setup time of $\overline{CAS}$ high to LCLK1 ↑, all cycles except internal DRAM refresh	174 See fig. 18		01	9,10,11	$0.5t_Q$-15		ns
			02	9,10,11	$0.5t_Q$-10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5 \le V_{CC} \le 5.5$ V	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Hold time of $\overline{W}$ high after LCLK1 high, shift register transfer	175 See fig. 18	V_{cc} = 4.5 V	01	9,10,11	t_Q-15		ns
			02	9,10,11	t_Q-10		ns
Setup time of $\overline{W}$ low to LCLK1 ↓, shift register transfer	176 See fig. 18		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{W}$ low after LCLK1 low, shift register transfer	177 See fig. 18		01	9,10,11	t_Q-15		ns
			02	9,10,11	t_Q-10		ns
Setup time of $\overline{W}$ high to LCLK1 ↑, shift register transfer	178 See fig. 18		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{W}$ high after LCLK1 high, write	179 See fig. 18		01	9,10,11	t_Q-15		ns
			02	9,10,11	t_Q-10		ns
Setup time of $\overline{W}$ low to LCLK1 ↓, write	180 See fig. 18		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{W}$ low after LCLK2 low, write	181 See fig. 18		01	9,10,11	$0.5t_Q$-15		ns
			02	9,10,11	$0.5t_Q$-10		ns
Setup time of $\overline{W}$ high to LCLK1 ↑, write	182 See fig. 18		01	9,10,11	$0.5t_Q$-15		ns
			02	9,10,11	$0.5t_Q$-10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Hold time of $\overline{TR}/\overline{QE}$ high after LCLK1 high, shift register transfer	183 See fig. 18	V_{CC} = 4.5 V	01	9,10,11	t_Q-15		ns
			02	9,10,11	t_Q-10		ns
Setup time of $\overline{TR}/\overline{QE}$ low to LCLK1 ↓, shift register transfer	184 See fig. 18		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{TR}/\overline{QE}$ low after LCLK2 high, shift register transfer	185 See fig. 18		01	9,10,11	t_Q-15		ns
			02	9,10,11	t_Q-10		ns
Setup time of $\overline{TR}/\overline{QE}$ high to LCLK2 ↓, shift register transfer	186 See fig. 18		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{TR}/\overline{QE}$ high after LCLK1 high, read	187 See fig. 18		01	9,10,11	t_Q-15		ns
			02	9,10,11	t_Q-10		ns
Setup time of $\overline{TR}/\overline{QE}$ low to LCLK1 ↓, read	188 See fig. 18		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{TR}/\overline{QE}$ low after LCLK2 low, read	189 See fig. 18		01	9,10,11	$0.5t_Q$-15		ns
			02	9,10,11	$0.5t_Q$-10		ns
Setup time of $\overline{TR}/\overline{QE}$ high to LCLK1 ↑, read	190 See fig. 18		01	9,10,11	$0.5t_Q$-15		ns
			02	9,10,11	$0.5t_Q$-10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device types	Group A subgroups	Limits Min	Limits Max	Unit
Hold time of $\overline{DEN}$ high after LCLK2 low, write	191 See fig. 18	V_{CC} = 4.5 V	01	9,10,11	t_Q-15		ns
			02	9,10,11	t_Q-10		ns
Setup time of $\overline{DEN}$ low to LCLK2 ↑, read	192 See fig. 18		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{DEN}$ low after LCLK1 high, write	193 See fig. 18		01	9,10,11	t_Q-15		ns
			02	9,10,11	t_Q-10		ns
Setup time of $\overline{DEN}$ high to LCLK1 ↓, write	194 See fig. 18		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{DEN}$ high after LCLK1 high, read	195 See fig. 18		01	9,10,11	t_Q-15		ns
			02	9,10,11	t_Q-10		ns
Setup time of $\overline{DEN}$ low to LCLK1 ↓, read	196 See fig. 18		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{DEN}$ low after LCLK2 low, read	197 See fig. 18		C1	9,10,11	$0.5t_Q$-15		ns
			02	9,10,11	$0.5t_Q$-10		ns
Setup time of $\overline{DEN}$ high to LCLK1 ↑, read	198 See fig. 18		01	9,10,11	$0.5t_Q$-15		ns
			02	9,10,11	$0.5t_Q$-10		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Device	Group A subgroups	Limits Min	Limits Max	Unit
Hold time of DDOUT high after LCLK2 low, read	199 See fig. 18	V_{CC} = 4.5 V dc	01	9,10,11	t_Q-15		ns
			02	9,10,11	t_Q-10		ns
Setup time of DDOUT low to LCLK2 ↑, read	200 See fig. 18		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of DDOUT low after LCLK1 high, read	201 See fig. 18		01	9,10,11	t_Q-15		ns
			02	9,10,11	t_Q-10		ns
Setup time of DDOUT high after LCLK1 ↓, read	202 See fig. 18		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Hold time of $\overline{LAL}$ high after LCLK2 high, CAS-before-RAS refresh	203 See fig. 18		01	9,10,11	t_Q-15		ns
			02	9,10,11	t_Q-10		ns
Setup time of $\overline{LAL}$ low to LCLK2 ↓, CAS-before-RAS refresh	204 See fig. 18		01	9,10,11	t_Q-20		ns
			02	9,10,11	t_Q-10		ns
Period of video input clock VCLK	205 See fig. 19		01	9,10,11	100		ns
			02	9,10,11	80		ns
Pulse duration of VCLK high	206 See fig. 19		01	9,10,11	40		ns
			02	9,10,11	30		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/3/ $-55°C \le T_C \le +125°C$ unless otherwise specified $4.5\ V \le V_{CC} \le 5.5\ V$	Group A subgroups	Limits		Unit
				Min	Max	
Pulse duration of VCLK Low	207 See fig. 19	V_{CC} = 4.5 V	Device types 01 9,10,11	40		ns
			02 9,10,11	30		ns
Delay from VCLK low to HSYNC, VSYNC, or BLANK low	209 See fig. 20		All 9,10,11		30	ns
Delay from VCLK low to HSYNC, VSYNC or BLANK high	210 See fig. 20		All 9,10,11		30	ns
Hold time of HSYNC, VSYNC or BLANK high after VCLK ↓	211 See fig. 20		All 9,10,11	0		ns
Hold time of HSYNC, VSYNC or BLANK low after VCLK ↓	212 See fig. 20		All 9,10,11	0		ns
Setup time of HSYNC, VSYNC, valid after VCLK ↑ 10/	213 See fig. 21		All 9,10,11	20		ns
Hold time of HSYNC, VSYNC valid after VCLK high 10/	214 See fig. 21		All 9,10,11	20		ns
Setup time of HSYNC, VSYNC high to VCLK ↑	215 See fig. 21		All 9,10,11	20		ns

1/ All test to be performed at worst-case test conditions unless otherwise specified.

2/ RUN/EMU will be no-connection in a typical configuration. The nominal pull-up current will be 250 μA.

3/ tQ = One quarter of a local output clock period, or twice the input clock period.
↑ = No longer low.
↓ = No longer high.

4/ These values are derived from characterization and are guaranteed but not tested.

5/ Parameter 22 is the maximum amount by which the RESET low-to-high transition can be delayed after the HCS low-to-high transition and still guarantee that the GSP is configured to run in self-bootstrap mode (HLT bit = 0) following the end of reset. HCS may be held low for some time past the low-to-high RESET transition, and will be ignored by the GSP for 17 local clock periods following the clock edge at which the low-to-high RESET transition is detected. Following completion of the eight RAS-only cycles that automatically follow reset, however, a low HCS level will be interpreted as a chip select.

6/ RESET and HCS are asynchronous inputs. The specified setup and hold times of these signals with respect to the high-to-low transition of LCLK1 need be met only to guarantee that a transition of RESET or HCS is detected by the device at a particular clock edge.

7/ LRDY is a synchronous input sampled during the low-to-high transition of LCLK2. The specified setup and hold times must be met for the device to operate properly.

8/ 4_{tQ} is added to these values for each wait state inserted.

9/ HOLD is a synchronous input sampled during the low-to-high transition of LCLK2. The specified setup and hold times must be met for the device to operate properly.

10/ Specified setup and hold times on asynchronous inputs are required only to guarantee recognition at indicated clock edge.

Case			Case			Case		
X	Y	Function	X	Y	Function	X	Y	Function
A6	1	VSS	J1	24	LAD13	J10	47	HD12
B6	2	RUN/EMU	J2	25	LAD14	H11	48	HD11
A5	3	RESET	K1	26	LAD15	H10	49	HD10
B5	4	VCLK	L2	27	VCC	G11	50	HD9
A4	5	INCLK	K2	28	LCLK1	G10	51	HD8
B4	6	LINT1	L3	29	LCLK2	F11	52	VSS
A3	7	LINT2	K3	30	HSYNC	F10	53	HD7
B3	8	HOLD	L4	31	VSYNC	E11	54	HD6
A2	9	LRDY	K4	32	BLANK	E10	55	HD5
B1	10	LAD0	L5	33	HLDA/EMUA	D11	56	HD4
B2	11	LAD1	K5	34	LAL	D10	57	HD3
C1	12	LAD2	L6	35	VSS	C11	58	HD2
C2	13	LAD3	K6	36	DDOUT	C10	59	HD1
D1	14	LAD4	L7	37	DEN	B11	60	HD0
D2	15	LAD5	K7	38	RAS	A10	61	VCC
E1	16	LAD6	L8	39	CAS	B10	62	HUDS
E2	17	LAD7	K8	40	W	A9	63	HLDS
F1	18	VSS	L9	41	TR/DE	B9	64	HREAD
F2	19	LAD8	K9	42	HINT	A8	65	HWRITE
G1	20	LAD9	L10	43	HRDY	B8	66	HCS
G2	21	LAD10	K11	44	HD15	A7	67	HFS0
H1	22	LAD11	K10	45	HD14	B7	68	HFS1
H2	23	LAD12	J11	46	HD13			

FIGURE 1. Terminal connections.

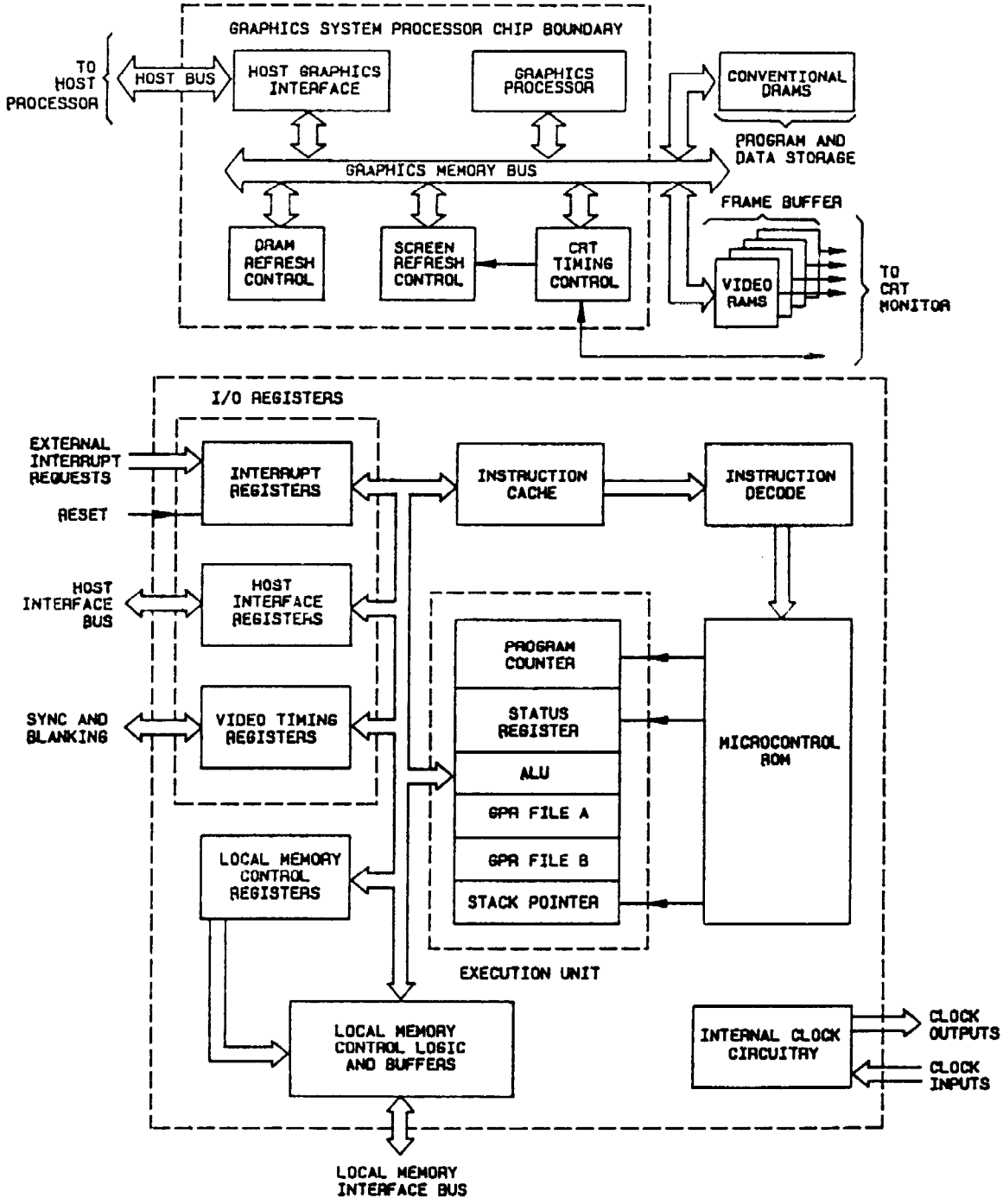
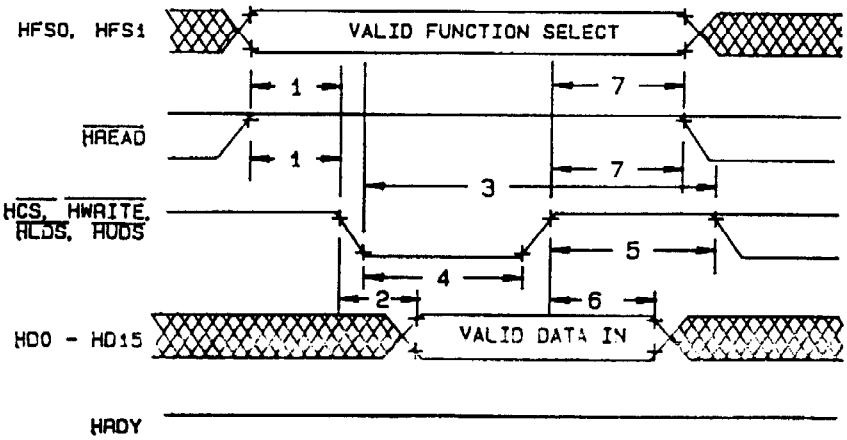
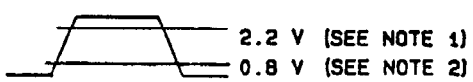
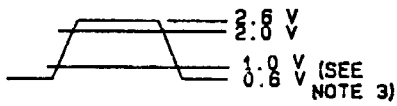


FIGURE 2. Block diagram.



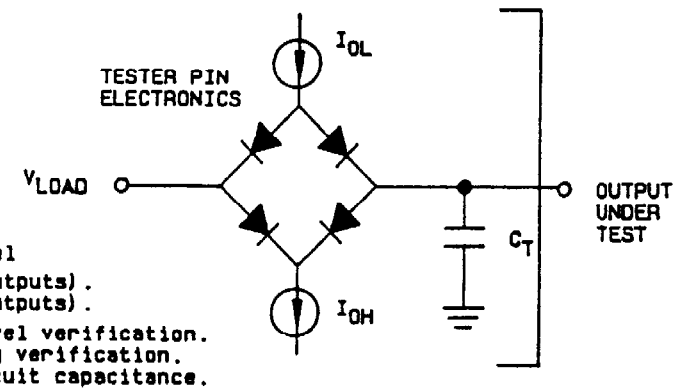


TTL-LEVEL INPUTS



TTL-LEVEL OUTPUTS

NOTES:
1. 3.2 volts for INCLK and 2.4 volts for VCLK.
2. LAD0-LAD15, HSYNC, VSYNC, and 0.6 V for all others.
3. 0.7 V for LCLK1, LCLK2, HLDA/EMUA, HINT, HRDY, and BLANK.



WHERE: I_{OL} = 2.0 mA dc level verification (all outputs).
I_{OH} = 400 µA (all outputs).
V_{LOAD} = 1.5 V dc level verification.
0.7 V timing verification.
C_T = 80 pF load circuit capacitance.

LOAD CIRCUIT

FIGURE 3. Waveform - host interface timing: write cycle with no wait timing diagram.

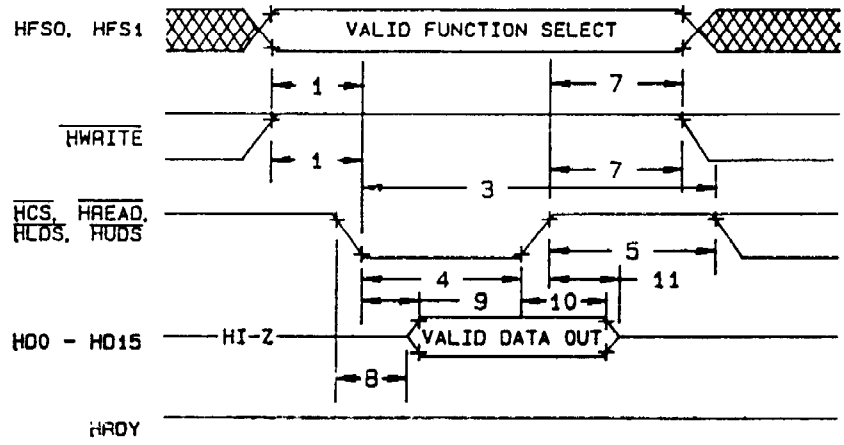
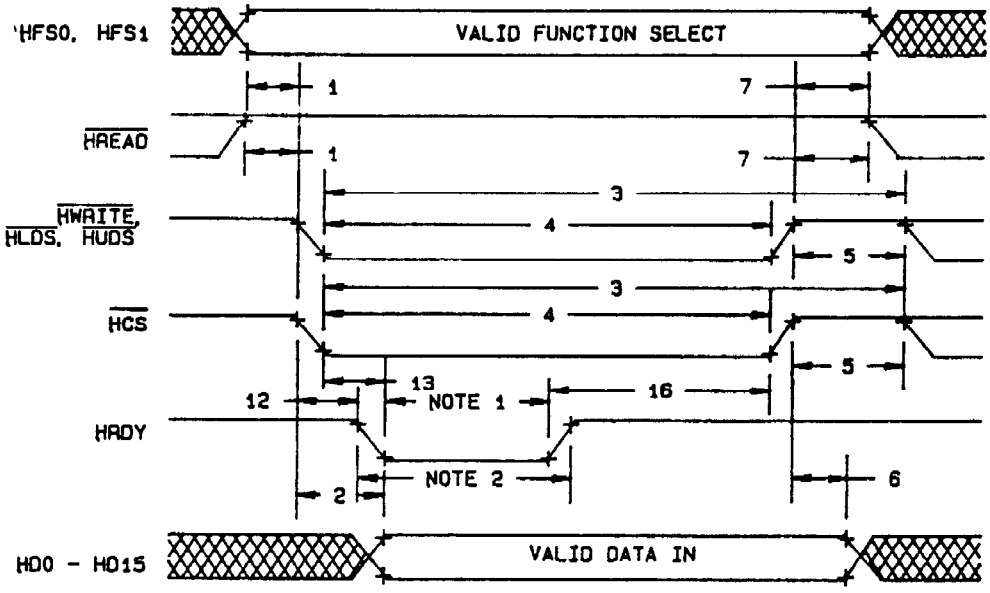


FIGURE 4. Waveform - host interface timing: Read cycle with no wait timing diagram.



NOTES:

1. Parameter 14 has been intentionally omitted but remains in the timing diagram for designer's reference. This parameter, $t_{w(RYL)}$, is a function of local bus memory contention and can be arbitrarily wide depending on when the Device completes its internal operations.
2. Parameter 15 has been intentionally omitted but remains in the timing diagram for designer's reference. This parameter, $t_{d(RYL-RYH)}$, indicates that a low-going pulse on HRDY can be arbitrarily narrow-the theoretical minimum would be 0 ns. This parameter is dependent on the internal synchronization of the falling edge of HCS with respect to local bus activity.

FIGURE 5. Waveform - host interface timing: write cycle with wait.

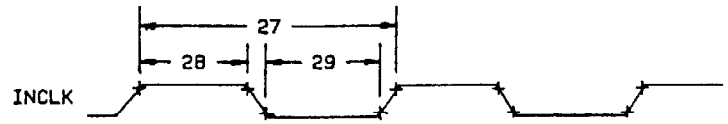


FIGURE 6. Waveform - Local bus timing diagram: Input timing diagram.

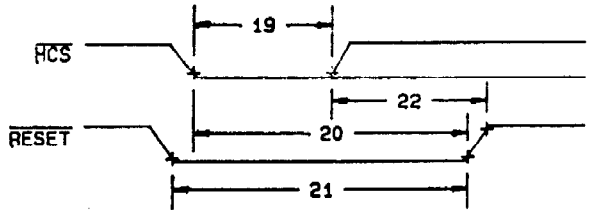


FIGURE 7. Waveform - Reset: asynchronous timing relationships timing diagram .

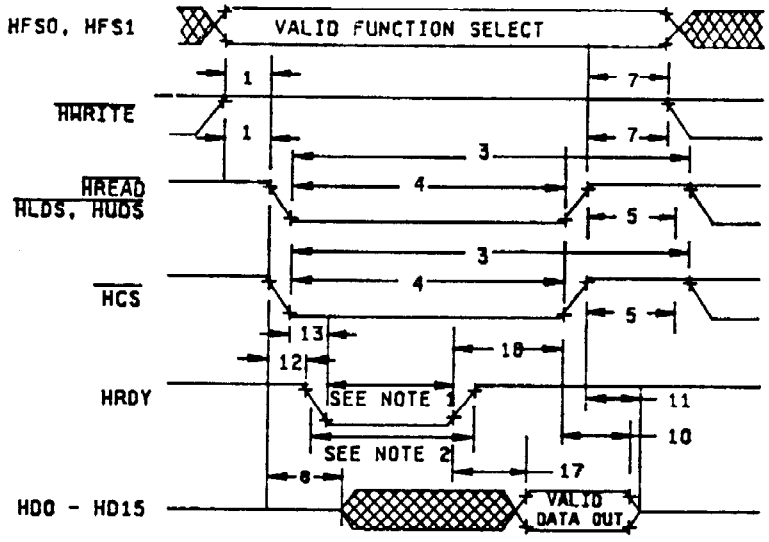
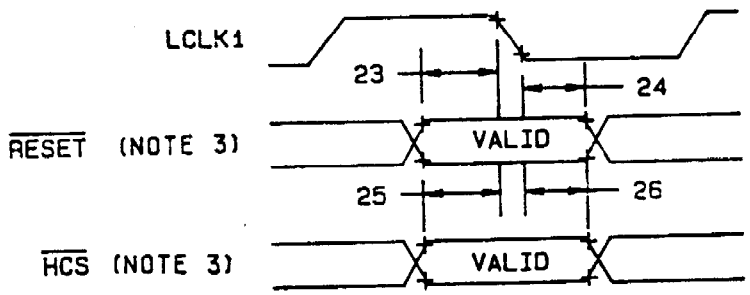


FIGURE 8. Waveform - Host interface timing read cycle with wait.

NOTES:

1. Parameter 14 has been intentionally omitted but remains in the diagram for designer's reference. this para, $t_{w(RYL)}$, is a function of local bus memory contention and an be arbitrarily wide depending on with the device completes its internal operations.

2. Parameter 15 has been intentionally omitted but remains in the timing diagram for designer's reference. This parameter, $t_{d(RYA-RYH)}$, indicates that a low going pulse on HRDY can be arbitrarily narrow-the theoretical minimum would be 0 ns. This parameter is dependent on the internal synchronization of the falling edge of HCS with respect to local bus activity



NOTE 3:

$\overline{\text{RESET}}$ and $\overline{\text{HCS}}$ are asynchronous inputs. The specified setup and hold times of these signals with respect to the high-to-low transition of LCLK1 need be met only to guarantee that transition of $\overline{\text{RESET}}$ of $\overline{\text{HCS}}$ is detected by the device at a particular clock edge.

FIGURE 9. Waveform - synchronous timing relationships timing diagram.

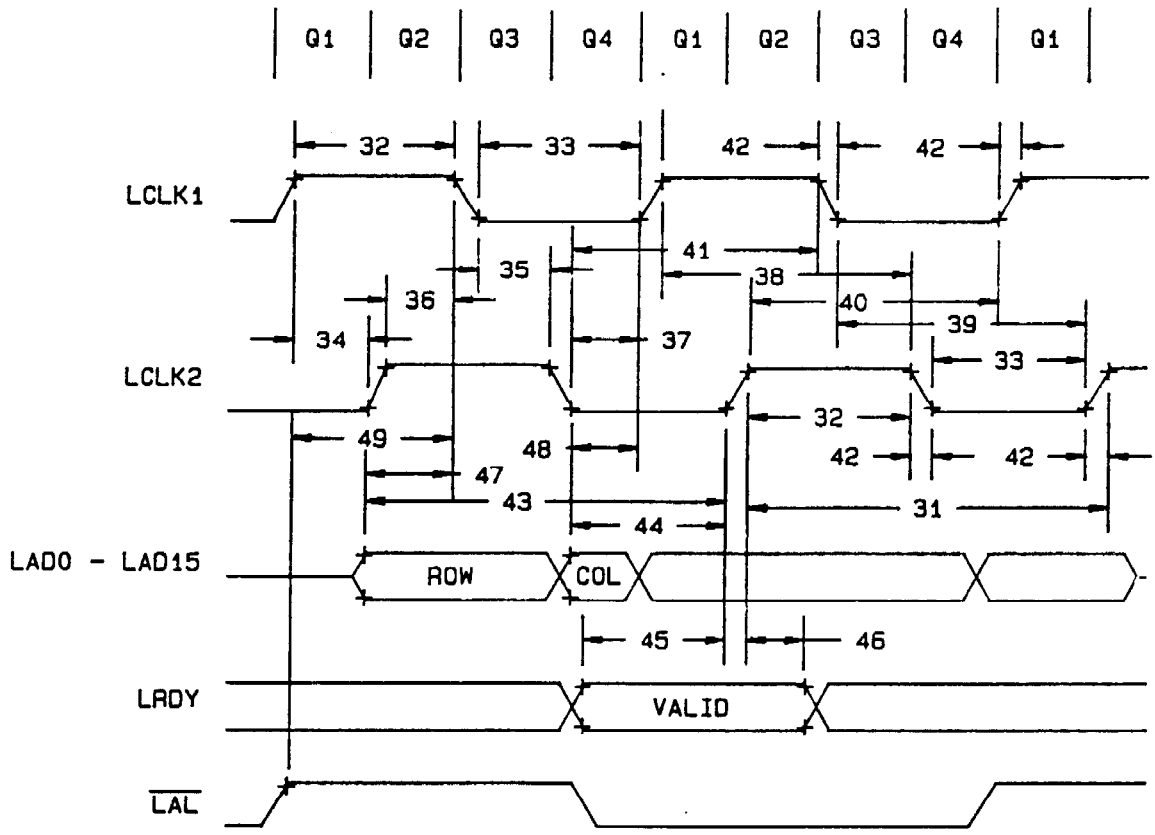


FIGURE 10. Waveform - local bus timing: Output clock and LRDY timing diagram.

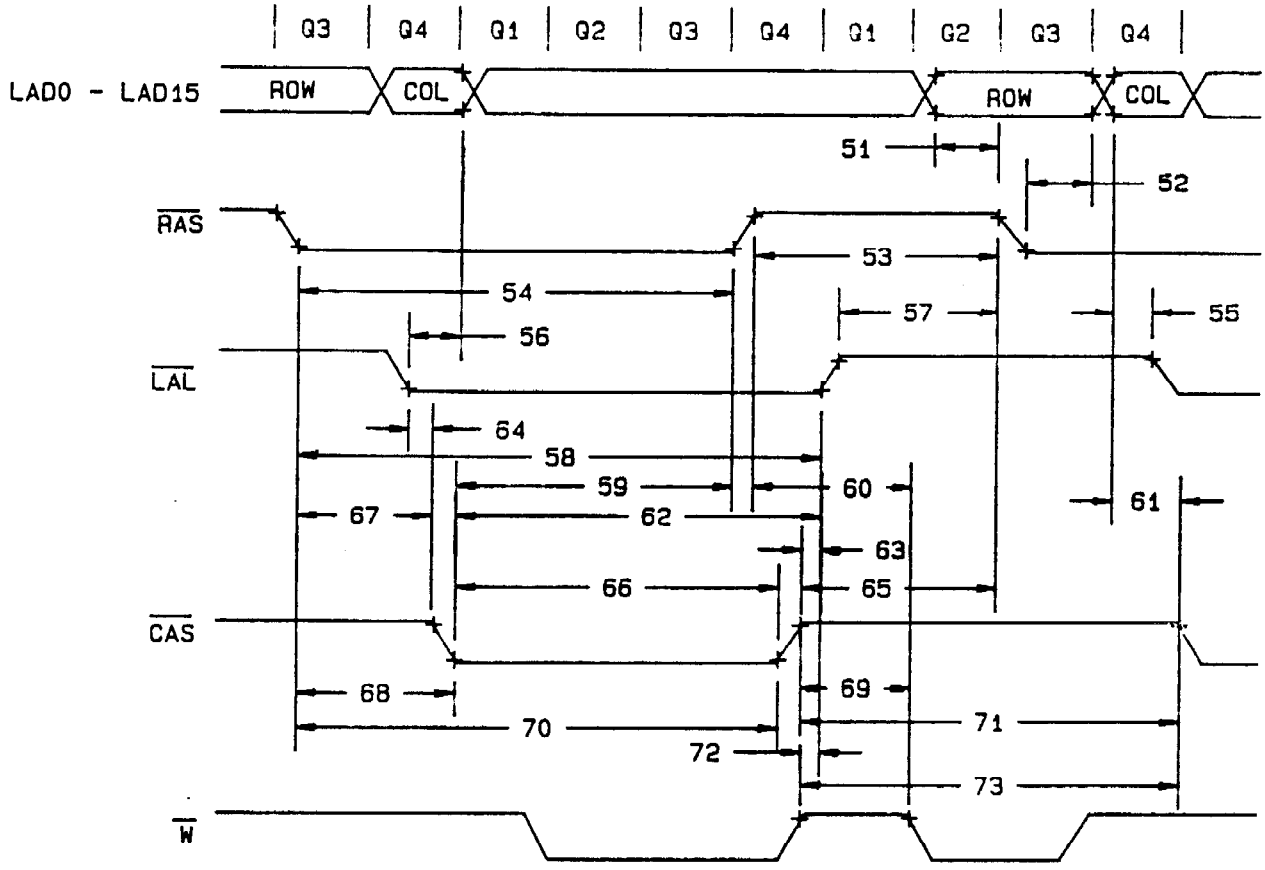


FIGURE 11. Waveform bus timing: The $\overline{RAS}$, $\overline{CAS}$, and $\overline{LAL}$ outputs timing diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90727
		REVISION LEVEL	SHEET 37

LOCAL BUS TIMING PARAMETERS: SHIFT REGISTER TRANSFER CYCLE

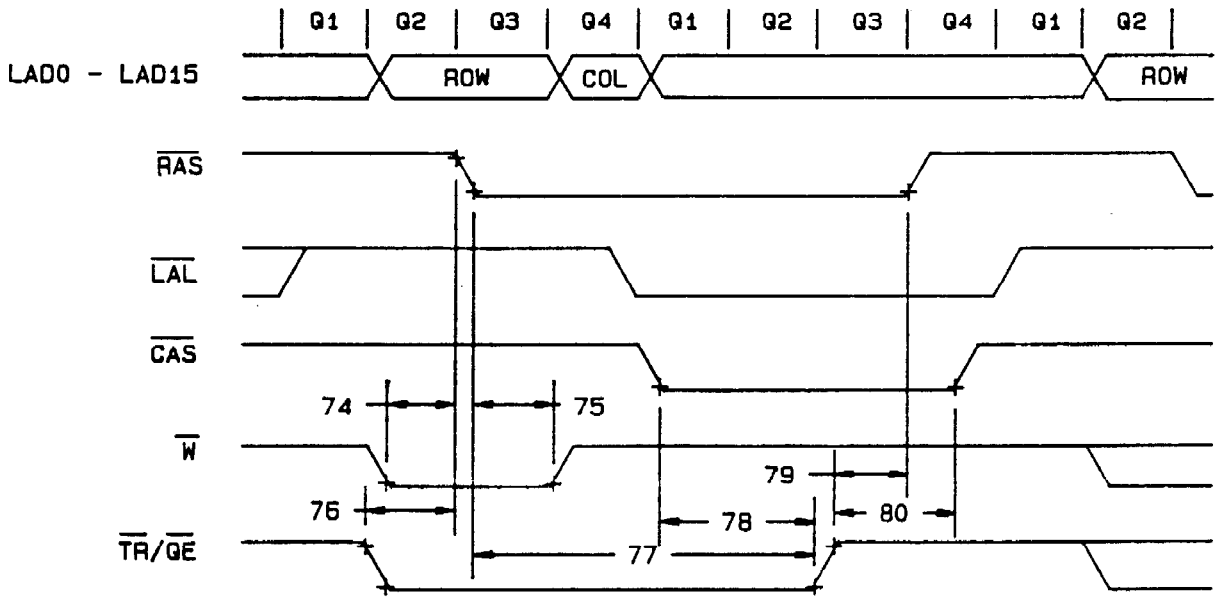


FIGURE 12. Waveform - local bus timing parameters: Shift resister transfer cycle timing diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90727
		REVISION LEVEL	SHEET 38

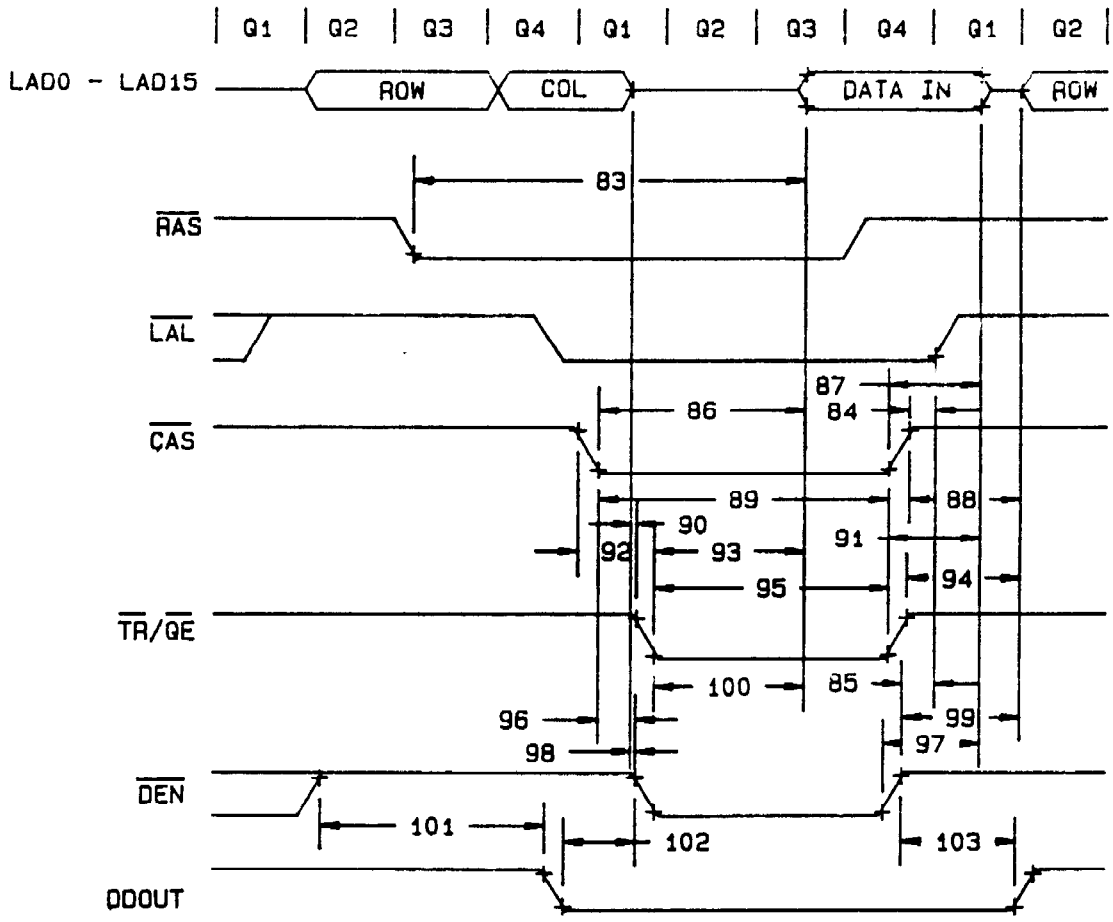


FIGURE 13. Waveform - local bus timing: Read cycle timing diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90727
		REVISION LEVEL	SHEET 39

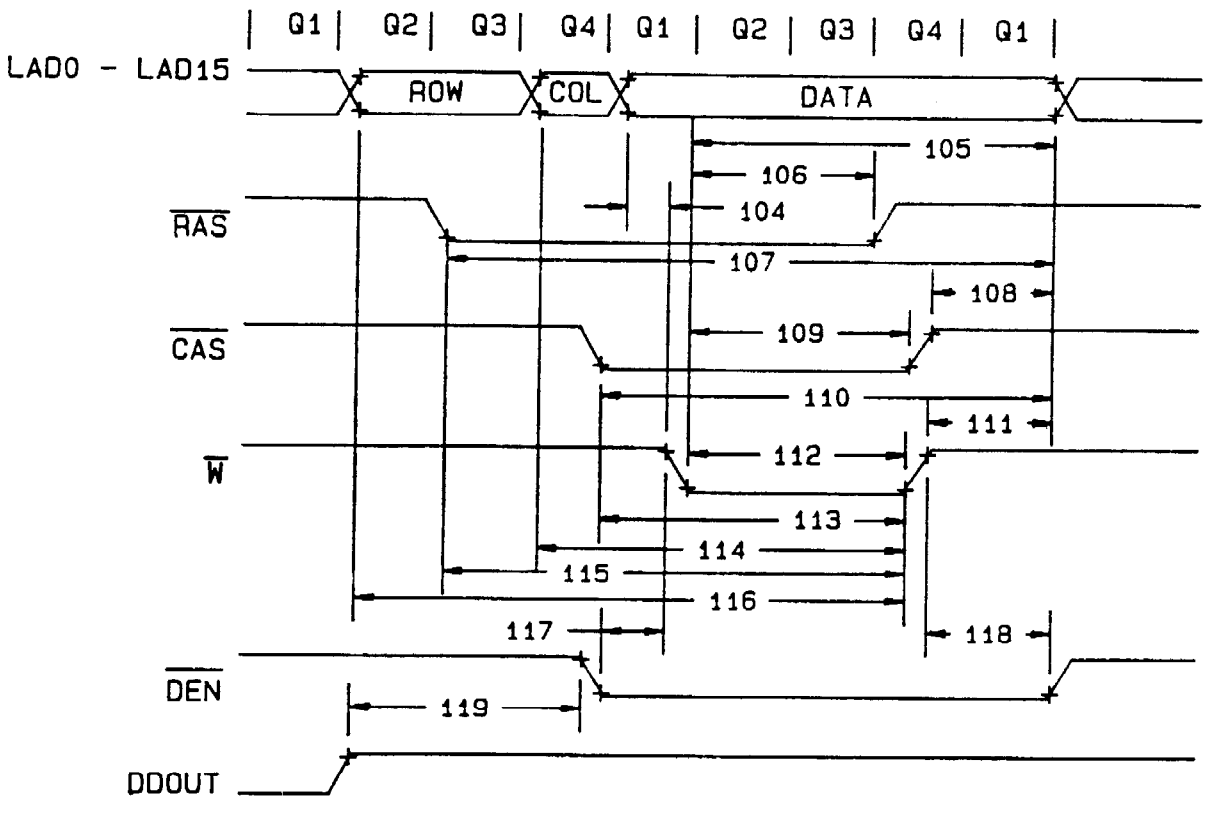


FIGURE 14. Waveform - local bus timing: Write cycle timing diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90727
		REVISION LEVEL	SHEET 40

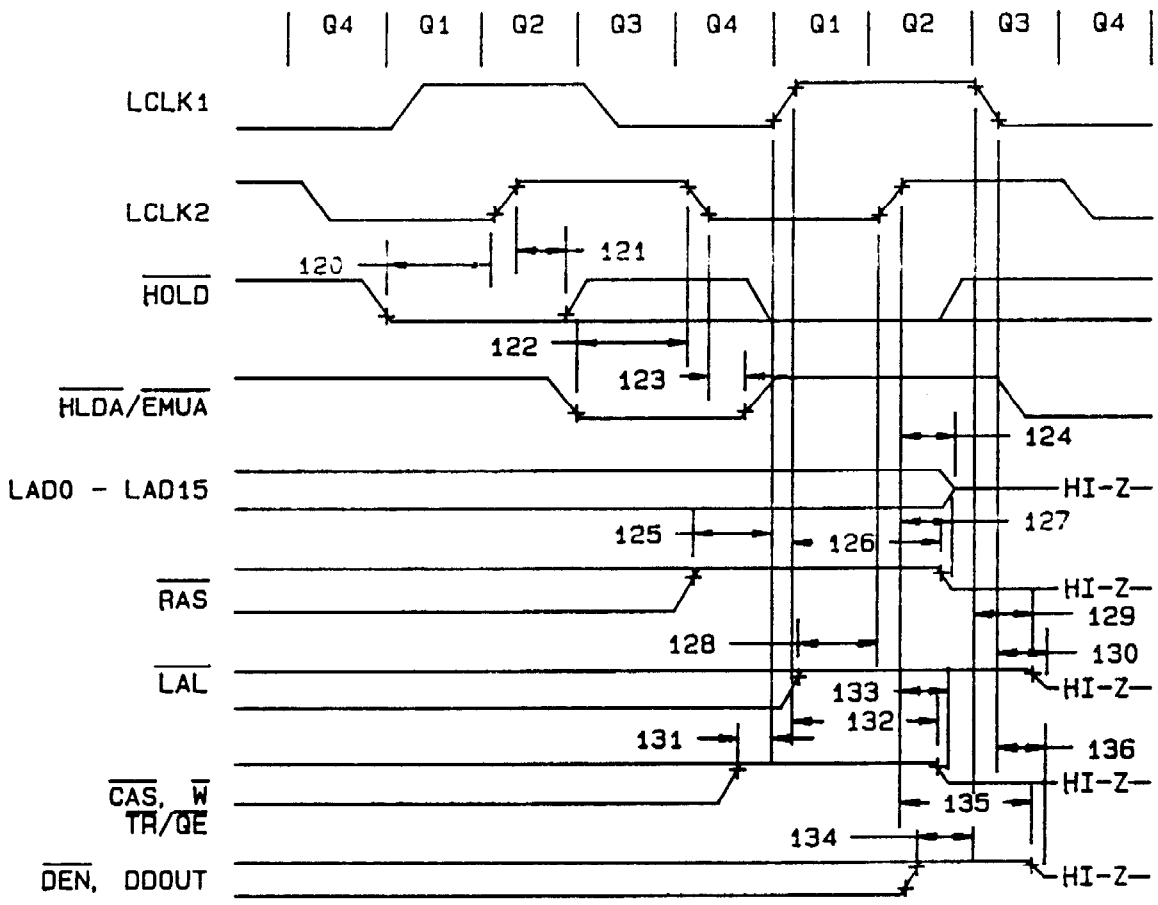


FIGURE 15. Waveform - GSP releases control of local bus timing diagram.

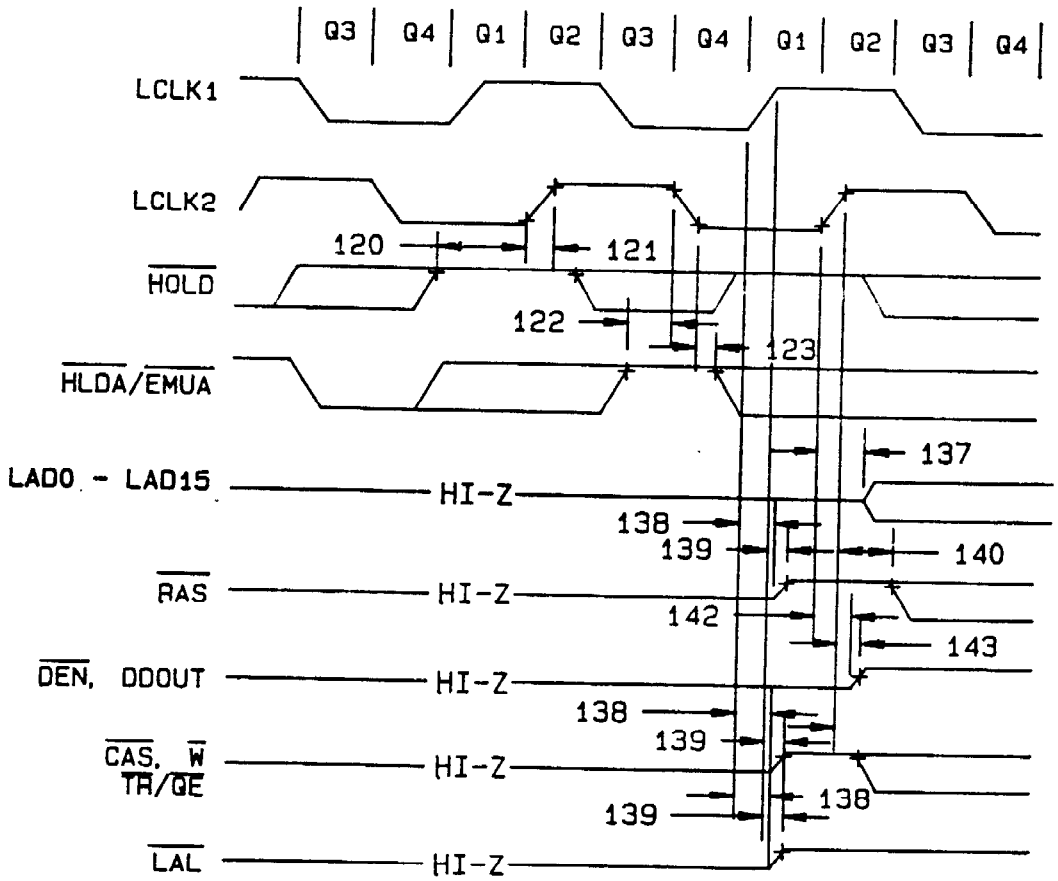


FIGURE 16. Waveform - GSP resumes control of local bus timing diagram.

$\overline{CAS}$ - BEFORE - $\overline{RAS}$ DRAM REFRESH CYCLE TIMING

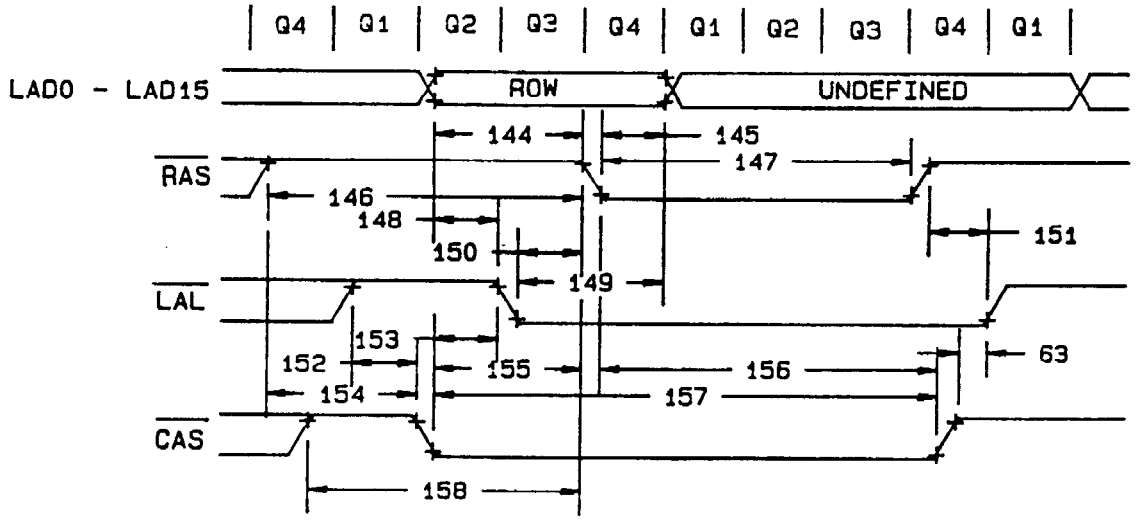


FIGURE 17. Waveform - $\overline{CAS}$-before-$\overline{RAS}$ DRAM refresh cycle timing diagram.

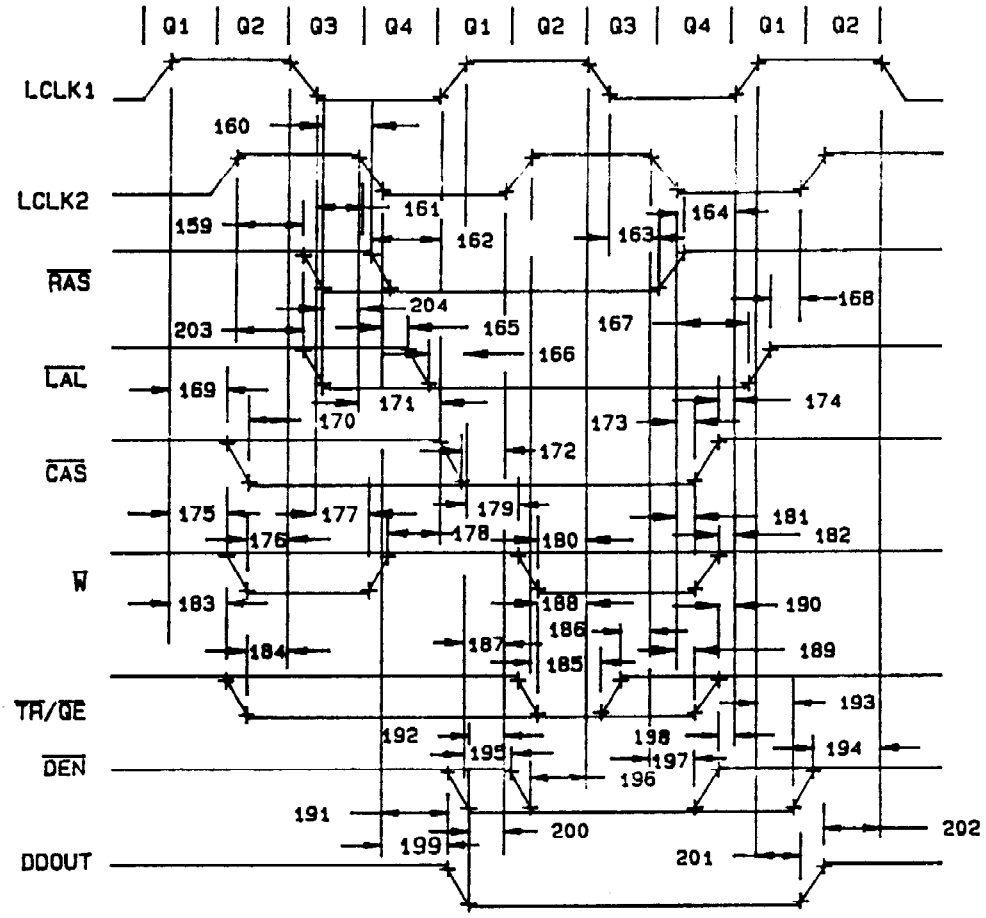


FIGURE 18. Waveform - local bus timing: Relationship of control signals to clocks timing diagram.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90727
		REVISION LEVEL	SHEET 44

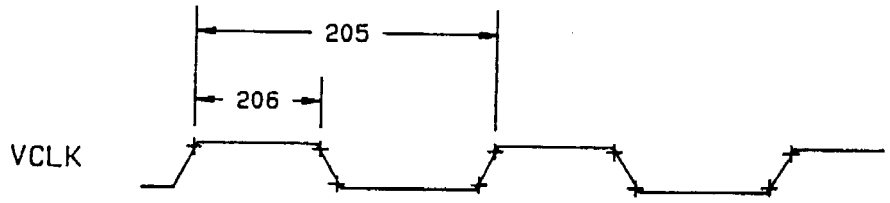


FIGURE 19. Waveform - video input clock timing diagram.

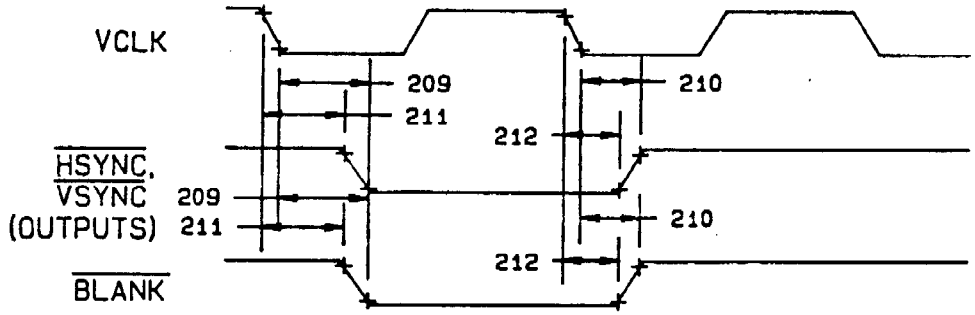
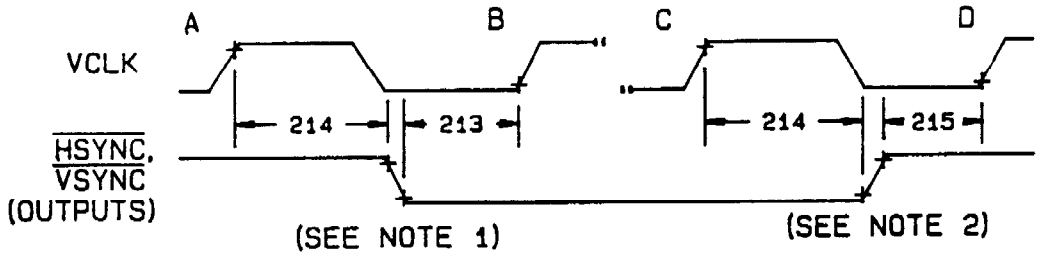


FIGURE 20. Waveform - video output timing diagram.



NOTES:
1. If the falling edge of the sync signal occurs more that $t_{h(SV-VCH)}$ past VCLK edge A, and at least $t_{su(SV-VCH)}$ before edge B, transition will be detected at edge B instead of edge A.
2. If the rising edge of the sync signal occurs more that $t_{h(SV-VCH)}$ past VCLK edge C, and at least $t_{su(SV-VCH)}$ before edge D, transition will be detected at edge D instead of edge C.

FIGURE 21. Waveform - VIDEO interface timing: External SYNC inputs timing diagram.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535 and as detailed in table IIB herein.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroups 4 (C_{IN}, C_O and $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design changes which may effect capacitance sample size is 5 devices with no failures, and all input and output terminal tested.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535 table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)		1,7,9			1,7,9
Final electrical parameters (see 4.2)	1,2,3,7,8, 1/ 9,10,11	1,2,3,7,8, 1/ 9,10,11	1,2,3,7,8, 2/9,10,11	1,2,3,7,8, 1/ 9,10,11	1,2,3,7,8, 2/9,10,11
Group A test requirements (see 4.4)	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11
Group B end-point electrical parameters (see 4.4)			1,7,9		
Group C end-point electrical parameters (see 4.4)	1,2,7,9	1,2,7,9		1,2,7,9	1,2,7,9
Group D end-point electrical parameters (see 4.4)	1,2,7,9	1,2,7,9	1,2,7,9	1,2,7,9	1,2,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.3.1 Additional criteria for device classes M, B, and S. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. For device class M, the test circuit shall be submitted to DESC-ECC for review with the certificate of compliance. For device classes B and S, the test circuit shall be submitted to the qualifying activity.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The steady-state life test circuit shall be submitted to DESC-ECC with the certificate of compliance and shall be under the control of the device manufacturer's TRB in accordance with MIL-I-38535.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

TABLE IIB. Additional screening for device class V.

Test	MIL-STD-883, test method	Lot requirement
Particle impact noise detection	2020	100%
Internal visual	2010, condition A or approved alternate	100%
Nondestructive bond pull	2023 or approved alternate	100%
Reverse bias burn-in	1015	100%
Burn-in	1015, total of 240 hours at +125°C	100%
Radiographic	2012	100%

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D. RHA quality conformance inspection sample tests shall be performed at the RHA level specified in the acquisition document.

a. RHA tests for device classes B and S for levels M, D, R, and H or for device class M for levels M and D shall be performed through each level to determine at what levels the devices meet the RHA requirements. These RHA tests shall be performed for initial qualification and after design or process changes which may affect the RHA performance of the device.

b. End-point electrical parameters shall be as specified in table IIA herein.

c. Prior to total dose irradiation, each selected sample shall be assembled in its qualified package. It shall pass the specified group A electrical parameters in table I for subgroups specified in table IIA herein.

d. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for RHA level being tested, and meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5 percent, after exposure.

e. Prior to and during total dose irradiation testing, the devices shall be biased to establish a worst case condition as specified in the radiation exposure circuit.

f. For device classes M, B, and S, subgroups 1 and 2 in table V, method 5005 of MIL-STD-883 shall be tested as appropriate for device construction.

g. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-ECC, telephone (513) 296-6022.

6.4 Comments. Comments on this drawing should be directed to DESC-ECC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.5 Symbols, definitions, and functional descriptions. The following types of memory cycles are supported: Read (see figure 22), write (see figure 23), VRAM memory-to-shift-register (see figure 24), VRAM shift-register-to-memory (see figure 25), RAS-only DRAM refresh (see figure 26) and CAS-before RAS DRAM refresh (see figure 27). The functional timing for these cycles is shown in the next six figures. The seventh figure indicates the timing signals output during an internal cycle (see figure 28), i.e., a cycle during which no memory access takes place. During a memory cycle, the row address, column address are output at the memory interface makes external multiplexing hardware unnecessary, while supporting a wide variety of memory configurations. For example, on figure 21, 16 consecutive address bits (5 through 20) are output on LAD1-LAD8 during the row and column address times. Output along with the address are bus status signals that indicates when DRAM refresh cycles, screen refresh (VRAM memory-to-shift-register) cycles, and instruction fetch cycles are occurring. The following remarks apply to memory timing in general. A row address is output on LAD0-LAD15 at the start of the cycle, and is valid before and after the fall of $\overline{RAS}$. Next a column address is outout on LAD0-LAD15. The column address is valid briefly before and after the falling edge of LAL, but is not valid at the falling edge of CAS. The column address is clocked into an external transparent latch (e.g., a M38510/346 octal latch) on the falling edge of LAL to provide the hold time on the column address required for dynamic RAMs and video RAMs. A transparent latch is required in order that the row address be available at the outputs of the latch during the start of the cycle. Very large memory configurations may require external buffering of data lines. The DEN signal serves as the drive-enable signal to external bidirectional buffers, e.g., M38510/348 octal buffers. The DDout signal serves as the direction control for the buffers. When an I/O register is addressed by the Device, a special memory read or write cycle is performed. During this cycle, the external $\overline{RAS}$ signal falls, but the external $\overline{CAS}$ remains inactive-high for the duration of the cycle. The timing shown in the first six functional timing diagrams assumes that the LRDY input remains high during the cycle. The LRDY pin is pulled low by slower memories requiring a longer cycle time. The Device samples the LRDY input at the end of Q1, as indicated on the figures. If LRDY is low, the Device inserts an additional state, called a "wait" state, into the cycle. Wait states continue to be inserted until LRDY is sampled at a high level. The cycle then completes in the manner indicated in the functional timing diagrams. A wait state is one local clock period in duration. Three additional timing diagrams provide examples of cycles extended by wait states (see figures 29, 30, and 31). The LRDY input ignored by the Device during internal cycles. A hold/hold acknowledge capability is also built into local memory interface to allow external devices to request control of the bus. After acknowledging a hold request, the Device releases the bus by driving its address/data bus and control outputs into the impedance state. See table III for the pin descriptions of case outline "X" and "Y".

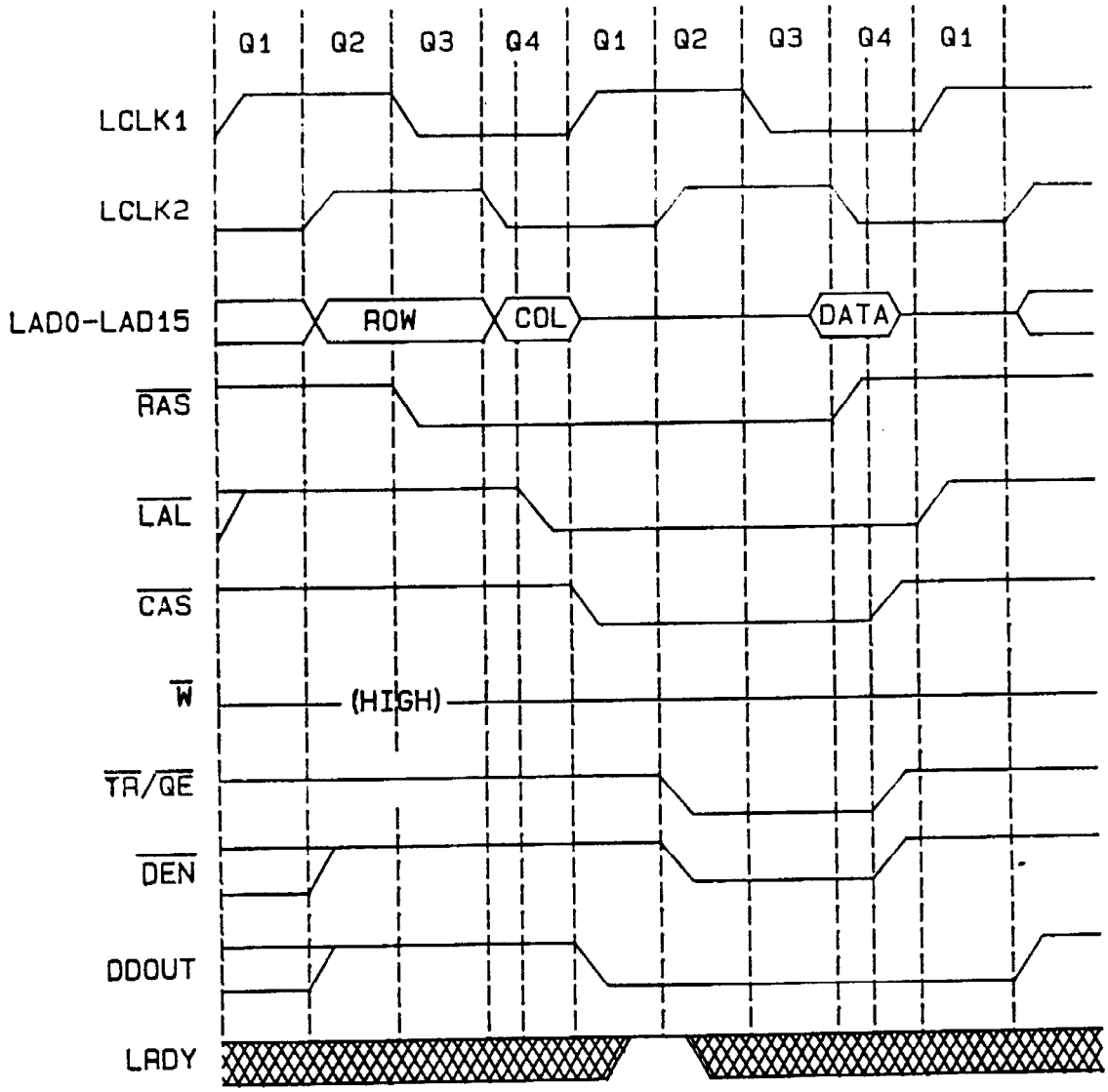


FIGURE 22. Waveform - read cycle timing diagram.

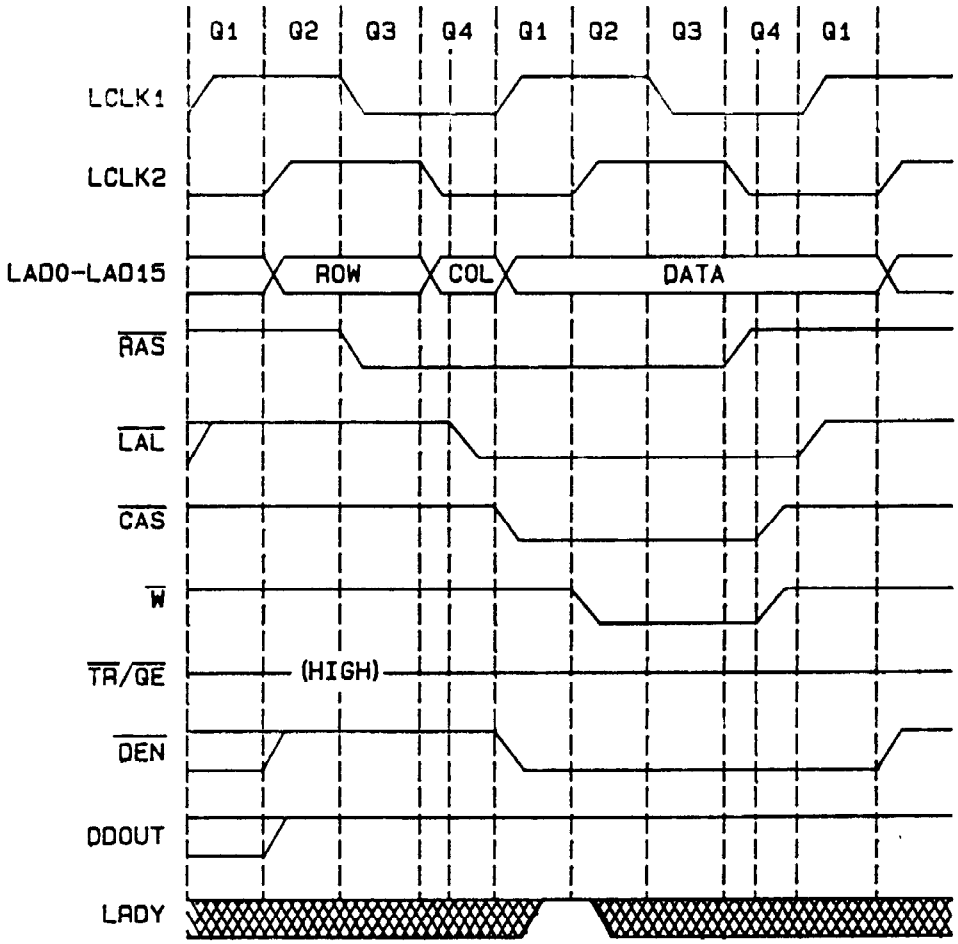


FIGURE 23. Waveform - write cycle timing diagram.

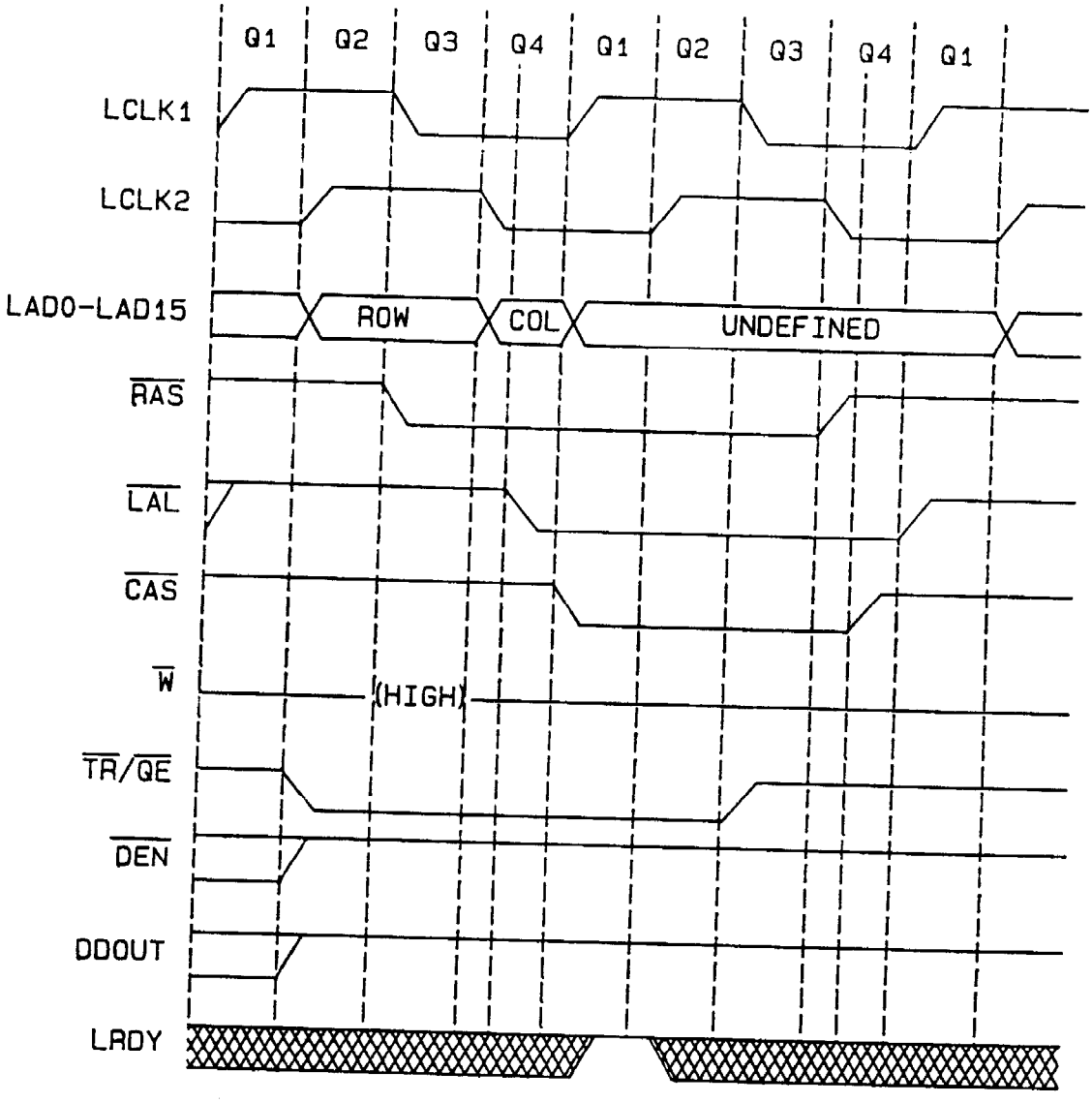


FIGURE 24. Waveform - memory-to-register cycle timing diagram.

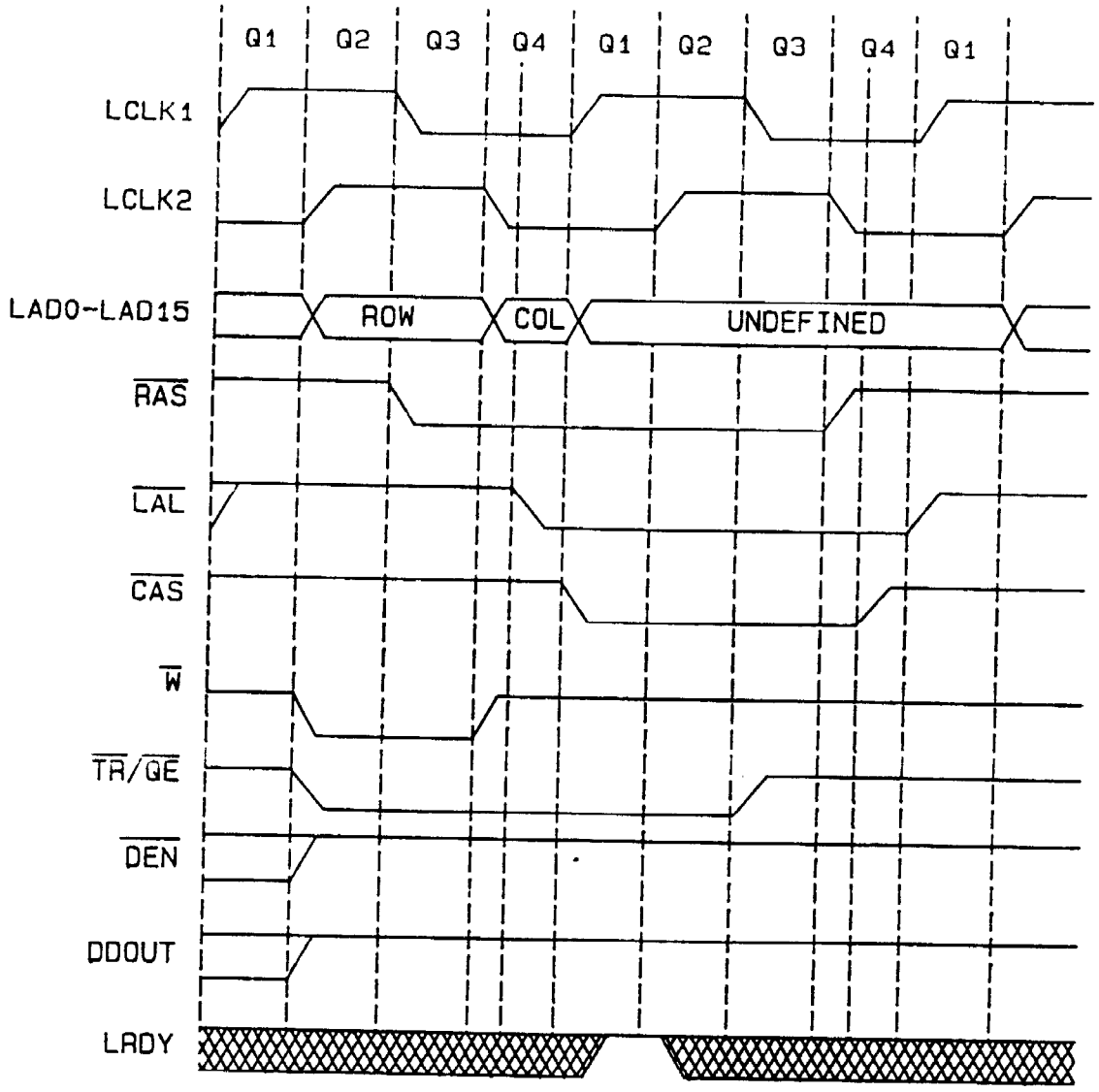


FIGURE 25. Waveform - register-to-memory cycle timing diagram.

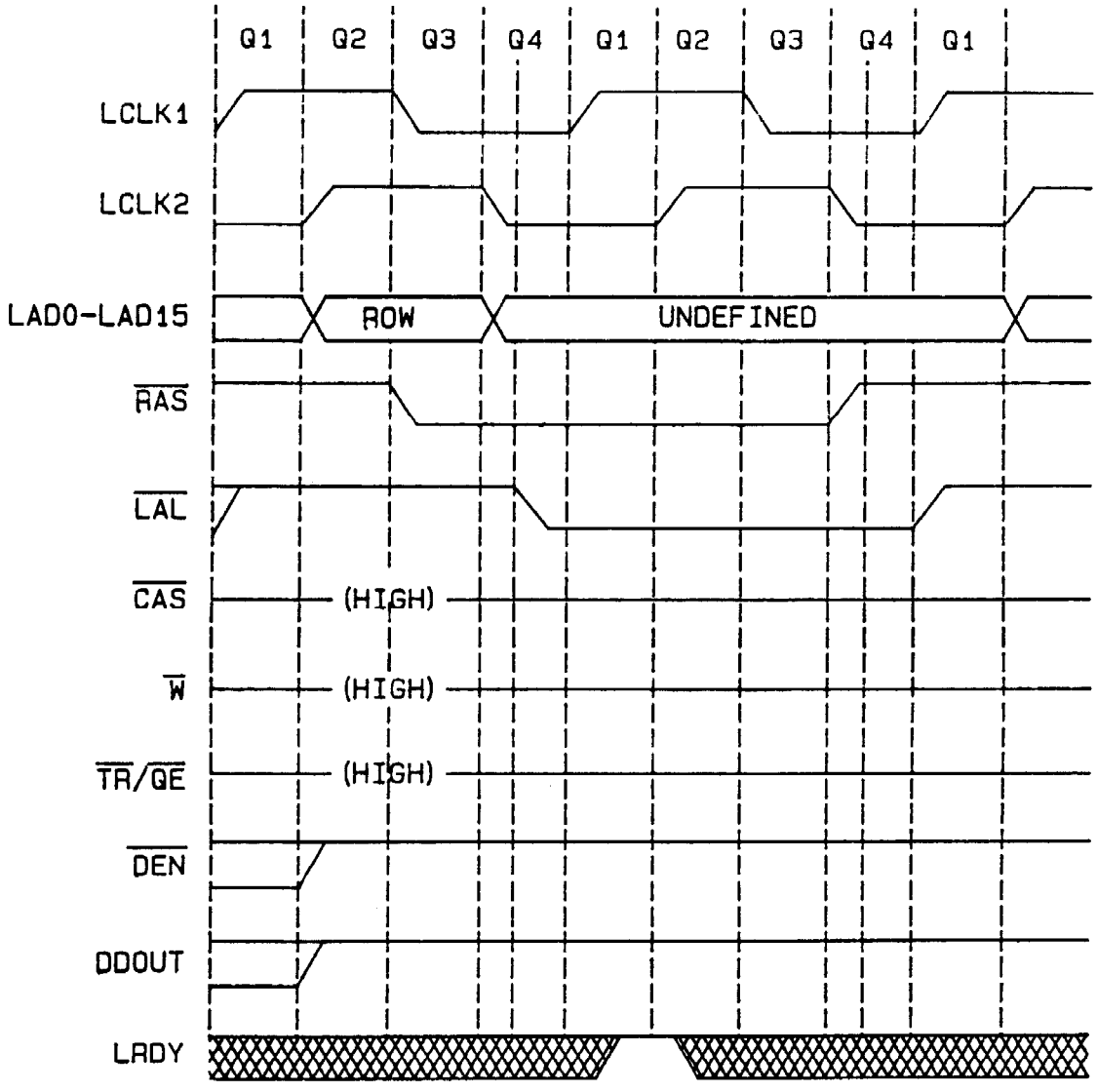


FIGURE 26. Waveform - $\overline{\text{RAS}}$-only DRAM refresh cycle timing diagram.

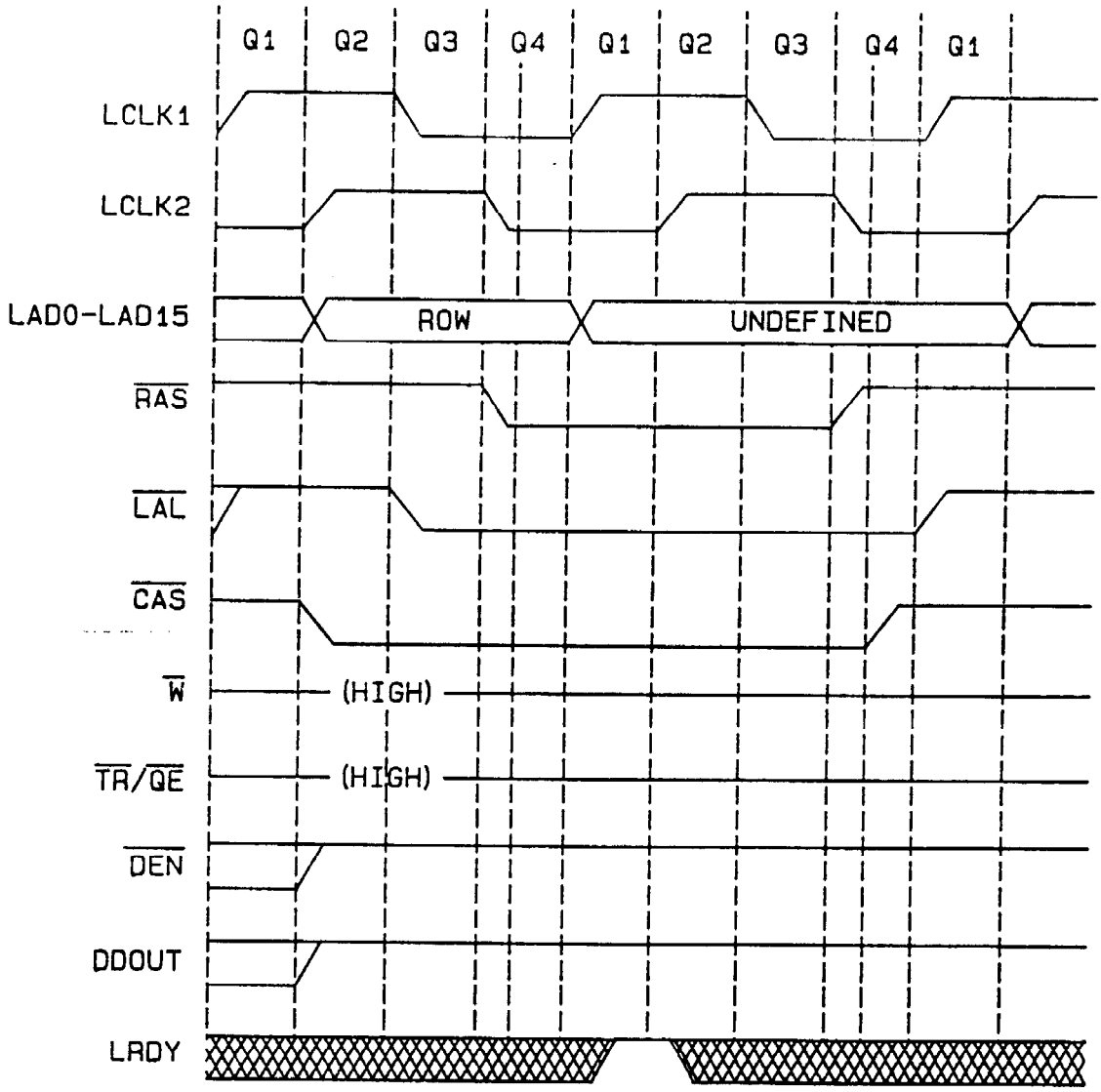


FIGURE 27. Waveform - $\overline{\text{CAS}}$-before $\overline{\text{RAS}}$ refresh cycle timing diagram.

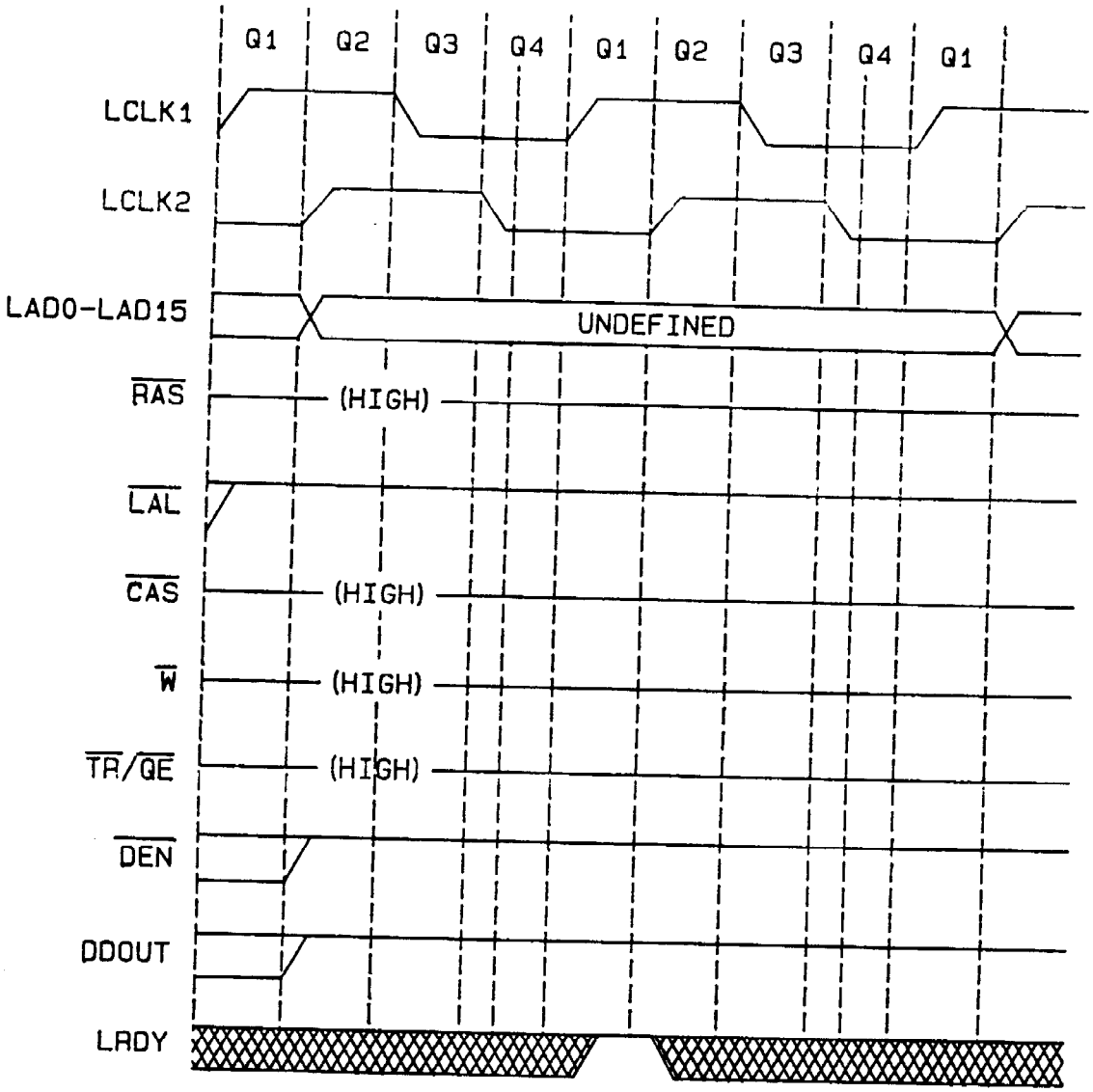


FIGURE 28. Waveform - internal cycles back to back timing diagram.

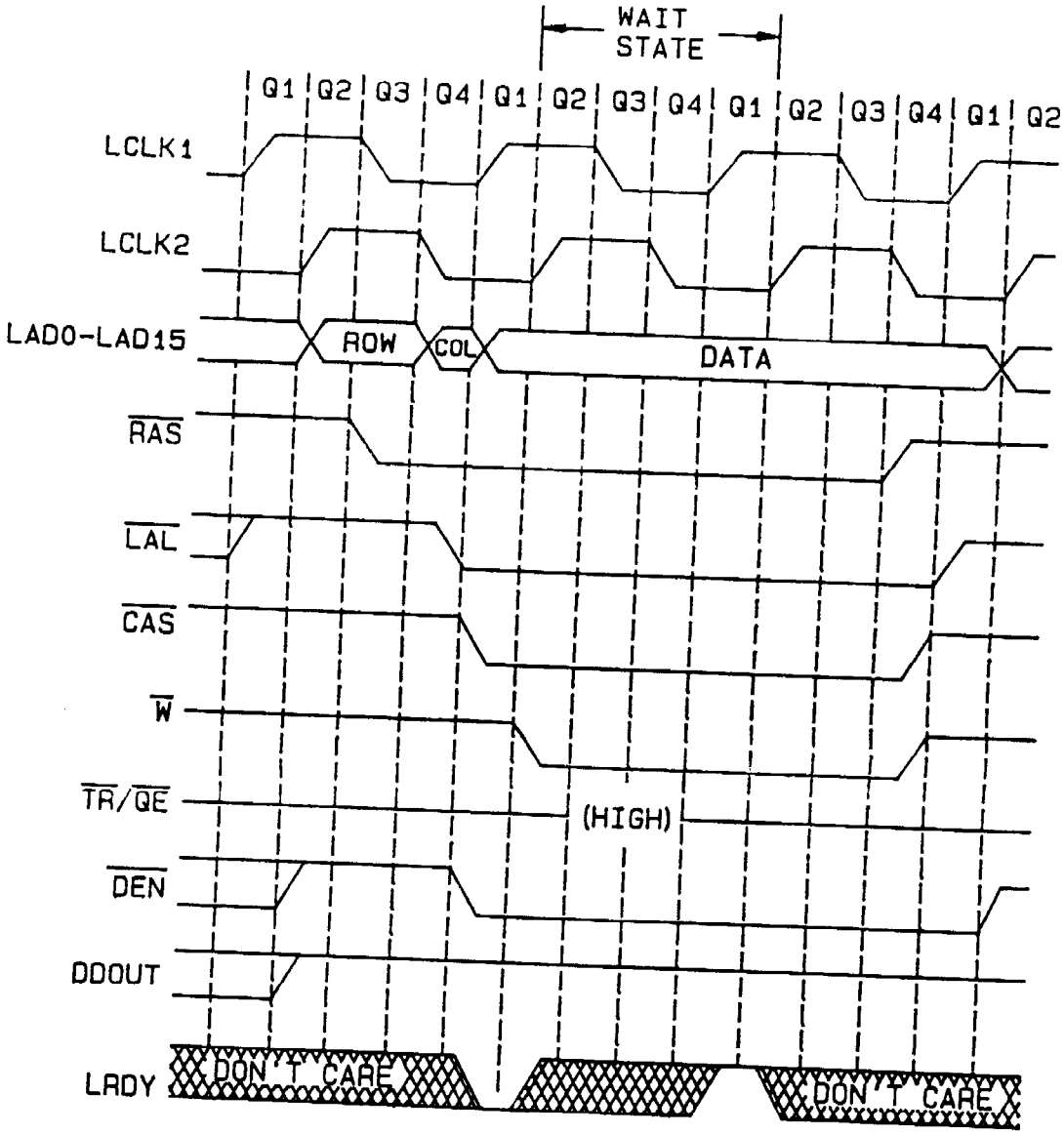


FIGURE 29. Waveform - write cycle with one wait state timing diagram

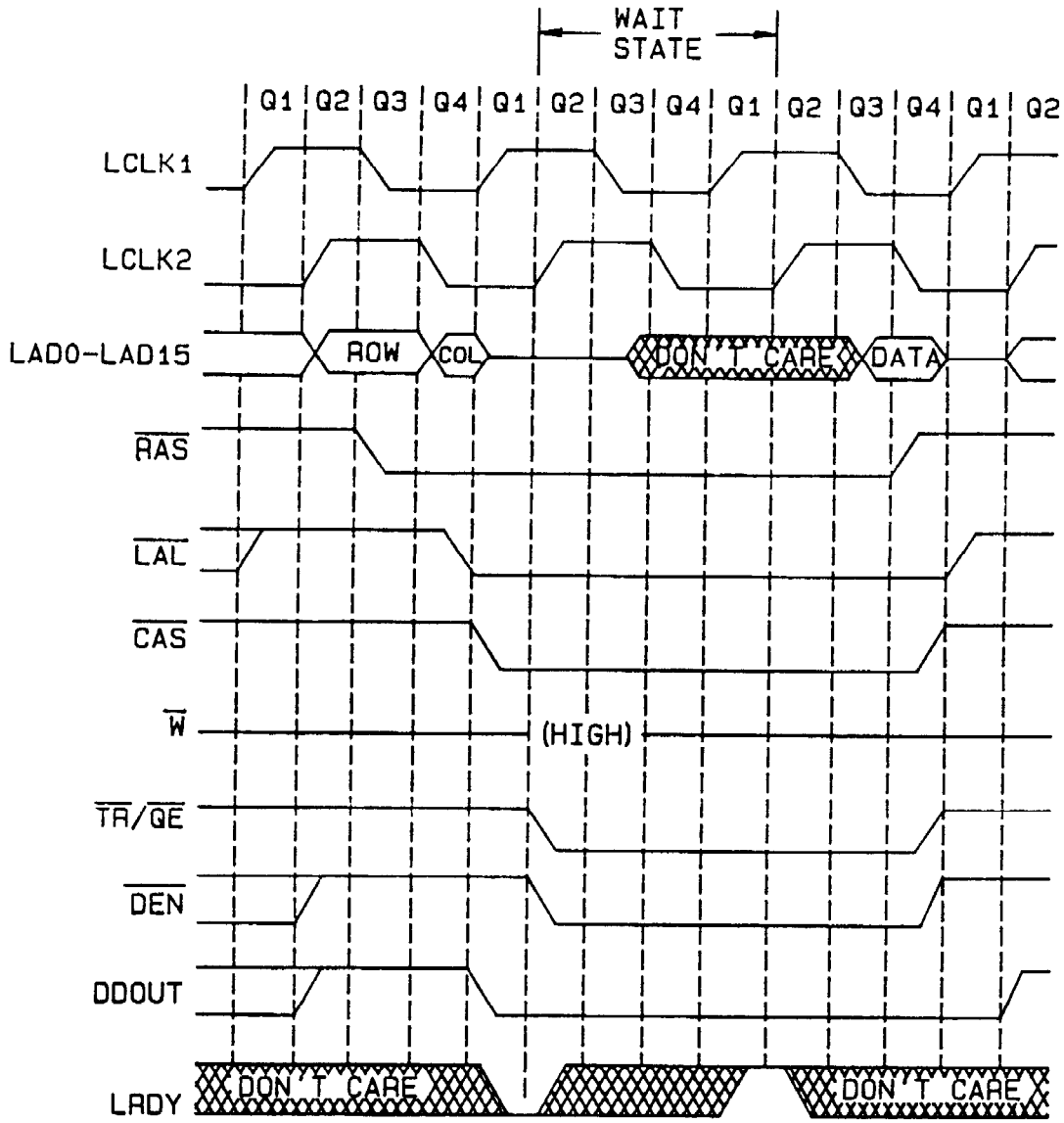


FIGURE 30. Waveform - read cycle with one wait state timing diagram.

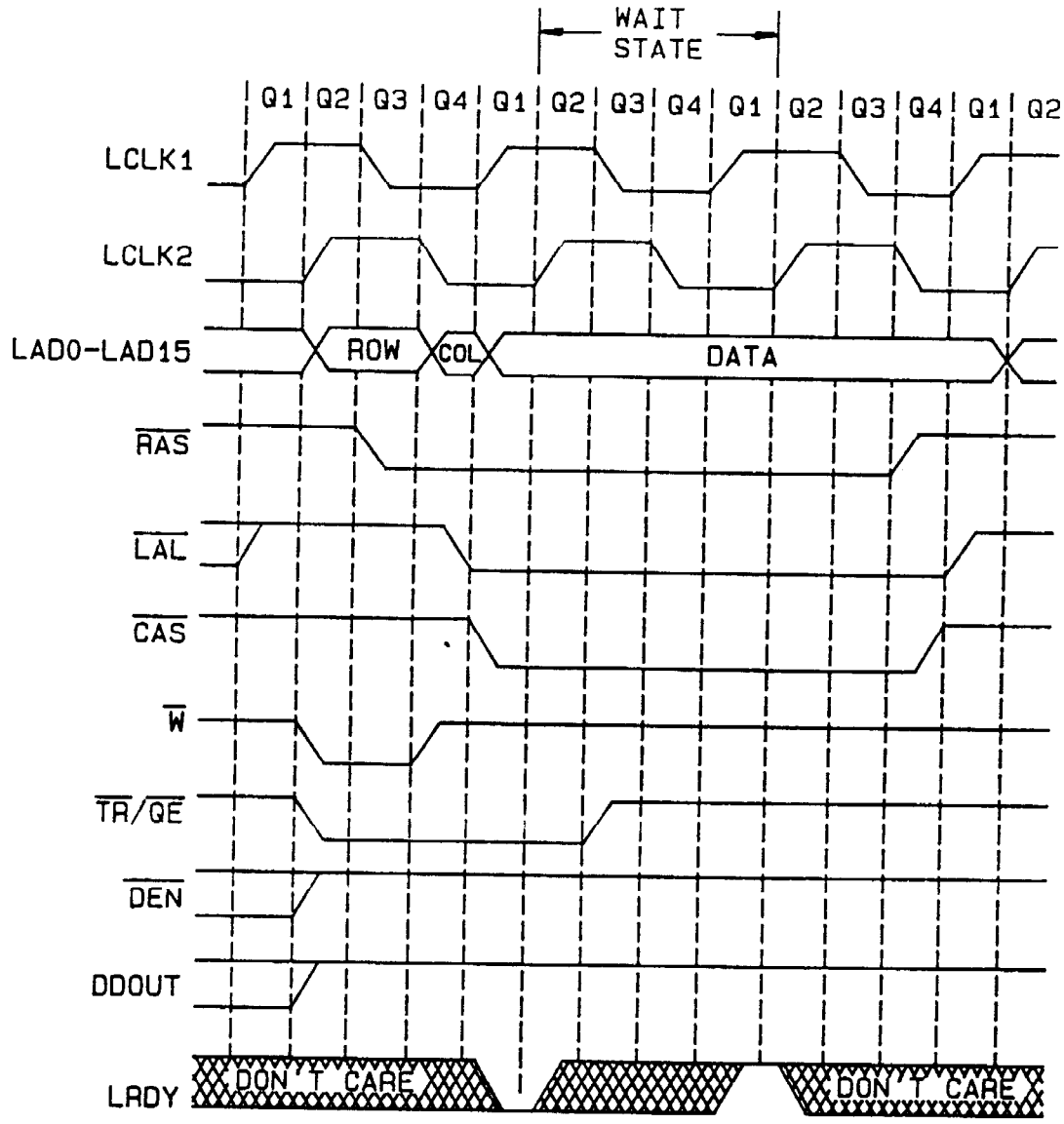


FIGURE 31. Waveform - shift-register-to-memory cycle with one wait state timing diagram.

Pin			I/O	Pin nomenclature
Name	Case X pin	Case Y pin		
VSS	A6,F1,L6,F11	1,18,35,52	I	Ground pins
VCC	L2,A10	27,61	I	Nominal 5-Volt power supply
$\overline{\text{RESET}}$	A5	3	I	
$\overline{\text{HCS}}$	B8	66	I	Host chip select
HD0-HD15	B11,C10,C11 D10,D11,E10 E11,F10,G10 G11,H10,H11 J10,J11,K10 K11	60-53 51-44	I/O	Host bidirectional data bus
HFS0,HFS1	A7,B7	67,68	I	Host function select
$\overline{\text{HINT}}$	K9	42	0	Host interrupt request
$\overline{\text{HLDS}}$	A9	63	I	Host lower data select
$\overline{\text{HUDS}}$	B10	62	I	Host upper data select
$\overline{\text{HRDY}}$	L10	43	0	Host ready
$\overline{\text{HREAD}}$	B9	64	I	Host read strobe
$\overline{\text{HWRITE}}$	A8	65	I	Host write strobe
$\overline{\text{RAS}}$	K7	38	0	Local row-address strobe
$\overline{\text{CAS}}$	L8	39	0	Local column-address strobe
DDOUT	K6	36	0	Local data direction out
$\overline{\text{DEN}}$	L7	37	0	Local data enable
LAD0-LAD15	B1,B2,C1,C2 D1,D2,E1,E2 F2,G1,G2,H1 H2,J1,J2,K1	10-17 19-26	I/O	Local address/data bus
LAL	K5	34	0	Local address latched
LCLK1,	K2	28	0	
$\overline{\text{LCLK2}}$	L3	29		
$\overline{\text{LINT1}}$,	B4	6	0	Local interrupt request
$\overline{\text{LINT2}}$	A3	7		
LRDY	A2	9	I	Local ready
$\overline{\text{TR/QE}}$	L9	41	0	Local shift register transfer/Output enable
$\overline{\text{W}}$	K8	40	0	Local write strobe
INCLK	A4	5	I	Input clock
HOLD	B3	8	I	Hold and emulation
$\overline{\text{RUN/EMU}}$	B6	2	I	
$\overline{\text{HLDA/EMUA}}$	L5	33	0	
$\overline{\text{BLANK}}$	K4	32	0	Blanking
HSYNC	K3	30	I/O	Horizontal sync
VCLK	B5	4	I	Video clock
$\overline{\text{VSYNC}}$	L4	31	I/O	Vertical sync

Table III. Pin Description.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-90727ZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-90727ZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-90727ZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-90727ZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-ECC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECC.

STANDARDIZED MILITARY DRAWING SOURCE APPROVAL BULLETIN

DATE: 93-01-20

Approved sources of supply for SMD 5962-90727 are listed below for immediate acquisition only and shall be added to MIL-BUL-103 during the next revision. MIL-BUL-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DESC-ECS. This bulletin is superseded by the next dated revision of MIL-BUL-103.

Military drawing PIN	Vendor CAGE number	Vendor 1/ similar PIN
5962-9072701MXX 2/	01295	SMJ34010-40GBM
5962-9072701MYX	01295	SMJ34010-40FDM
5962-9072702MXX 2/	01295	SMJ34010-50GBM
5962-9072702MYX	01295	SMJ34010-50FDM

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

2/ Inactive for new design. In accordance with MIL-STD-1835.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporated 13500 N. Central Expressway P.O. Box 655303 Midland, TX 79711-0448